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ZN428E8/ZN428J8/ZN428D

8-BIT LATCHED INPUT D-A CONVERTER

The ZN428 is a monolithic 8-bit D-A converter with input latches to facilitate updating from a data bus. The latch is transparent when enable is LOW and the data is held when enable is taken HIGH. The ZN428 also contains a 2.5V reference the use of which is pin optional to retain flexibility. An external fixed or varying reference may therefore be substituted.

FEATURES

- Contains DAC with Data Latch and On-Chip Reference
- Guaranteed Monotonic over the Full Operating Temperature Range
- Single +5V Supply
- Microprocessor Compatible
- TTL and 5V CMOS Compatible
- 800ns Settling Time
- Complementary to ZN427 A to D Series
- Commercial or Military Temperature Range

ORDERING INFORMATION

Device Type	Operating temperature	Package
ZN428D	0°C to +70°C	MP16W
ZN428E8	0°C to +70°C	DP16
ZN428J8	-55°C to +125°C	DC16

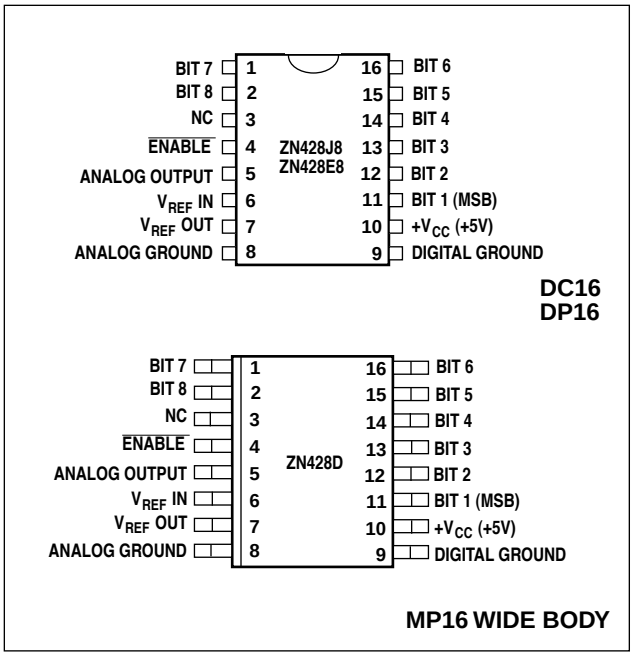
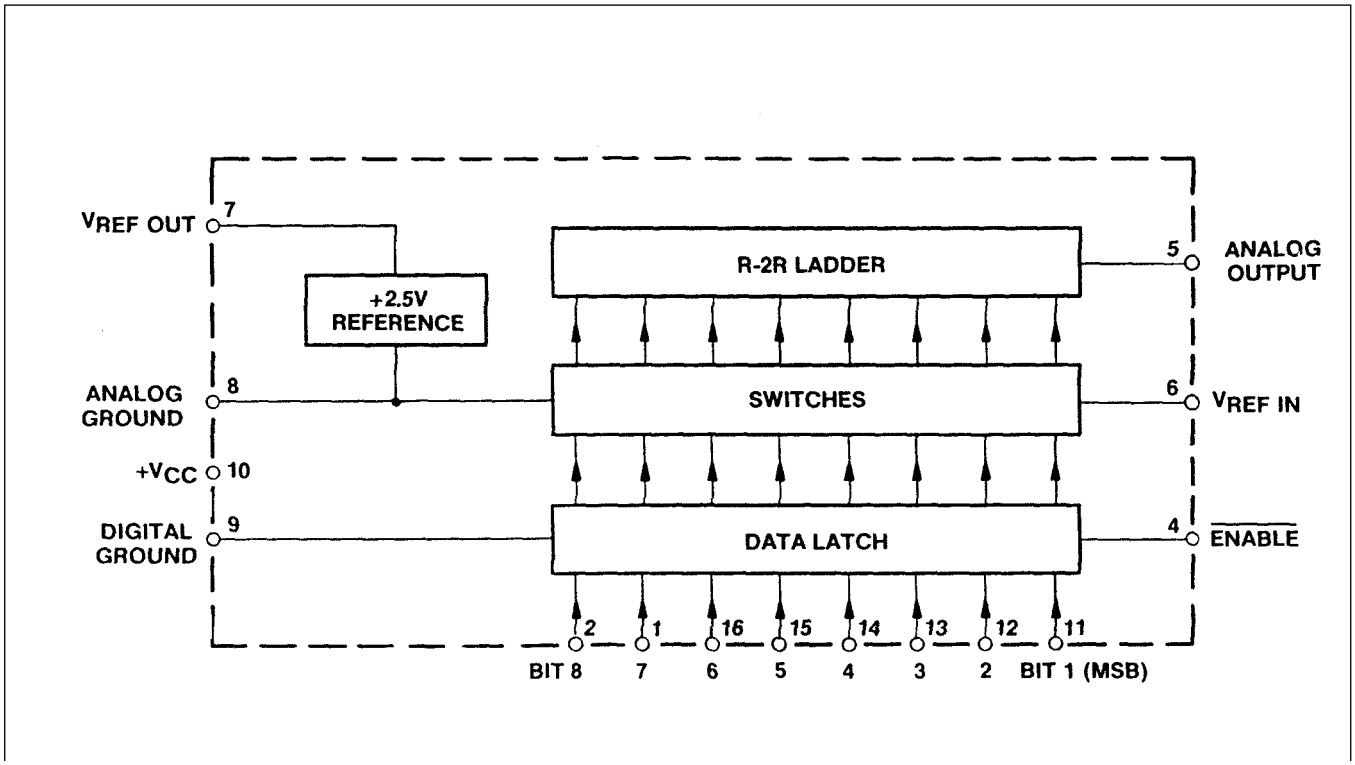


Fig.1 Pin connections (not to scale) - top view



ABSOLUTE MAXIMUM RATINGS

Supply voltage V_{CC}	+7.0V
Max.voltage, logic and V_{REF} inputs	$+V_{CC}$
Operating temperature range	0°C to +70°C (ZN428E8, ZN428D) -55°C to +125°C (ZN428J8)
Storage temperature range	-55°C to +125°C
Analog ground to digital ground	±200mV

ELECTRICAL CHARACTERISTICS

(V_{CC} = +5V, T_{amb} = 25°C unless otherwise specified)

Parameter	Min.	Typ.	Max.	Units	Conditions
Internal Voltage Reference					
Output voltage	2.475	2.550	2.625	V	R_{REF} = 390Ω 123 C_{REF} = 1μF
Slope resistance	-	0.5	2	Ω	
$V_{REF\ OUT}$ T.C.	-	50	-	ppm/°C	
Reference current	4	-	15	mA	Note 1
D-A Converter					
Linearity error	-	-	±0.5	LSB	2.0V ≤$V_{REF\ IN}$ ≤3.0V
Differential non-linearity	-	±0.5	-	LSB	
Linearity error T.C.	-	±3	-	ppm/°C	
Differential non-linearity T.C.	-	±6	-	ppm/°C	
Offset voltage	-	2	5	mV	All bits off
Offset voltage T.C.	-	±6	-	μV/°C	
Full-scale output	2.545	2.550	2.555		External reference
Full-scale output T.C.	-	2	-	ppm/°C	123 $V_{REF\ IN}$ = 2.560V, all bits ON
Analog output resistance	-	4	-	kΩ	
External reference voltage	0	-	3.0	V	
Settling time to 0.5 LSB	-	800	-	ns	1 LSB major transition (Note 2)
	-	1.25	-	μs	All bits ON to OFF or OFF to ON (Note 2)
Operating temperature range:					
ZN428D and ZN428 E8	0	-	70	°C	
ZN428J8	-55	-	125	°C	
Supply voltage (V_{CC})	4.5	5.0	5.5	V	
Supply current	-	20	30	mA	Note 3
Power consumption	-	100	-	mW	

Note 1: See REFERENCE
Note 2: R_L = 10MΩ, C_L = 10pF
Note 3: All inputs HIGH (V_{IH} = 3.5V)

ELECTRICAL CHARACTERISTICS (cont.)

Parameter	Min.	Typ.	Max.	Units	Conditions
Logic (over specified operating temperature range)					
High level input voltage	2.0	-	-	V	
Low level input voltage	-	-	0.8	V	
High level input current	- -	- -	60 20	µA µA	V_{IN} = 5.5V, V_{CC} = Max. V_{IN} = 2.4V, V_{CC} = Max.
Low level input current	-	-	-5	µA	V_{IN} = 0.4V, V_{CC} = Max.
Input clamp diode voltage	-	-1.5	-	V	I_{IN} = -8mA
Enable pulse width	100	-	-	ns	
Data set-up time	150	-	-	ns	Note 4
Data hold time	10	-	-	ns	Note 5

Note 4: Set up time before $\overline{\text{ENABLE}}$ goes high
Note 5: Hold time after $\overline{\text{ENABLE}}$ goes high

D-A CONVERTER

The converter is of the voltage switching type and uses an R-2R ladder network as shown in Fig.3. Each 2R element is connected to 0V or $V_{REF\ IN}$ by transistor voltage switches specially designed for low offset voltage (<1mV). A binary weighted voltage is produced at the output of the R-2R ladder.

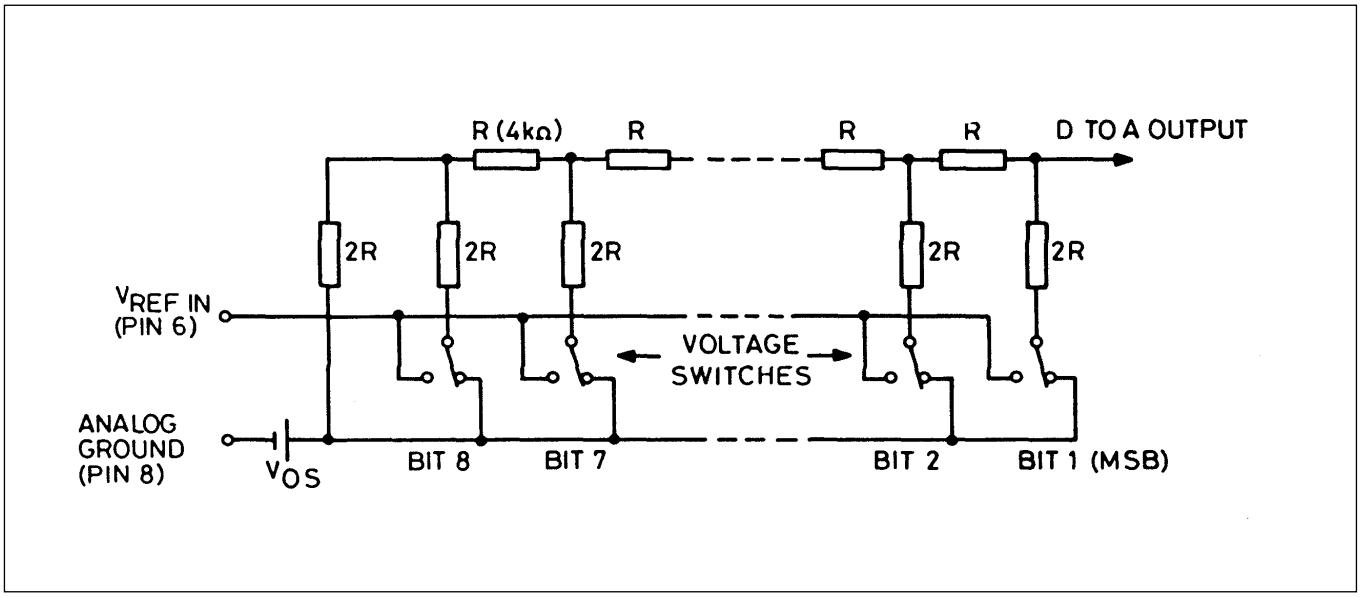


Fig.3 The R-2R ladder network

Analog output = $\frac{n}{256}$ ($V_{REF\ IN}$ - V_{OS}) + V_{OS}

where n is the digital input to the D-A from the data latch.

V_{OS} is a small offset voltage produced by the D-A switch currents flowing through the package lead resistance. The value of V_{OS} is typically 1mV. This offset will normally be removed by the setting up procedure (see Operating Notes) and because the offset temperature coefficient is low (±6µV/°C)the effect on accuracy is negligible.

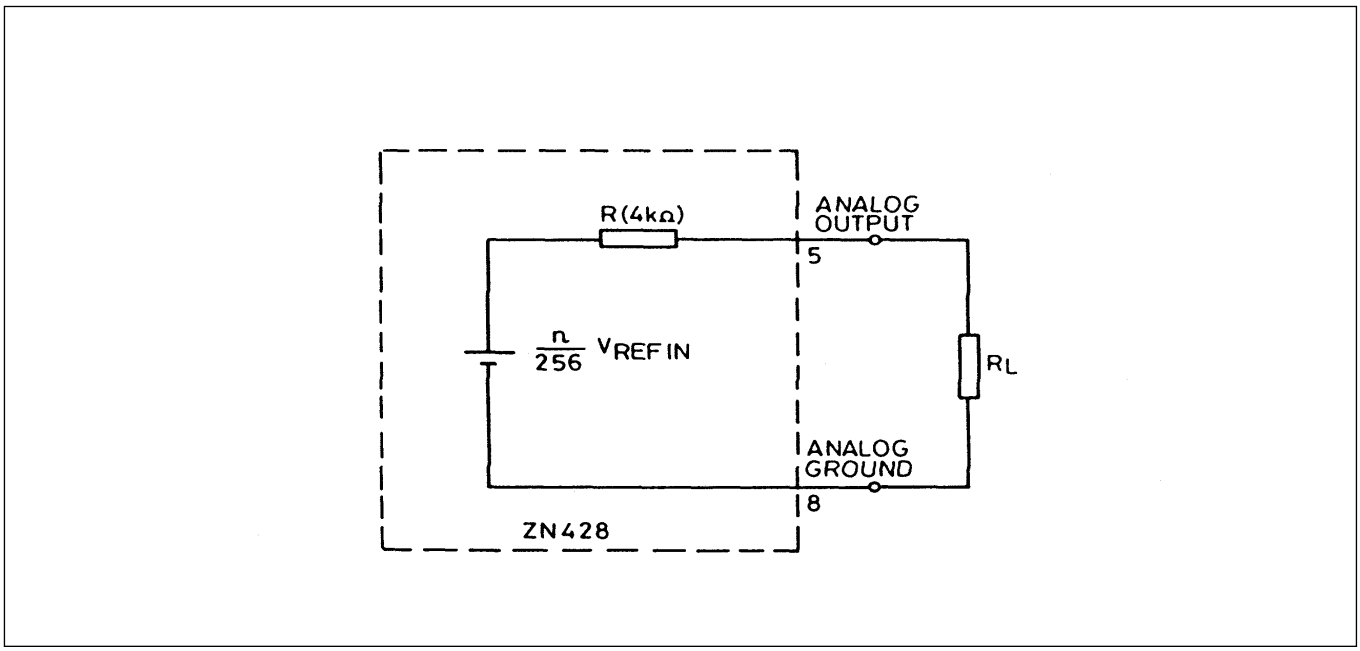


Fig.4 Analog output equivalent circuit

Fig.4 shows equivalent circuit of the output (ignoring V_{OS}). The output resistance R has a temperature coefficient of +0.2% per °C.

The gain drift due to this is $\frac{0.2R}{R+R_L}$ % per °C.

R_L should be chosen as large as possible to make the gain drift small. As an example if R_L = 400kΩ then the gain drift due to the T.C. of R for a 100°C change in ambient temperature will be less than 0.2%. Alternatively the ZN428 can be buffered by an amplifier (see Operating Notes).

REFERENCE

(a) Internal Reference

The internal reference is an active bandgap circuit which is equivalent to a 2.5V Zener diode with very low slope impedance (Fig.5). A resistor (R_{REF}), should be connected between $+V_{CC}$ (pin 10) and pin 7. The recommended value of 390Ω will supply a nominal reference current of (5.0-2.5)/0.39 = 6.4mA. A stabilising/decoupling capacitor C_{REF} = 1μF is required between pins 7 and 8 for internal reference option, $V_{REF\ OUT}$ (pin 7) being connected to $V_{REF\ IN}$ (pin 6).

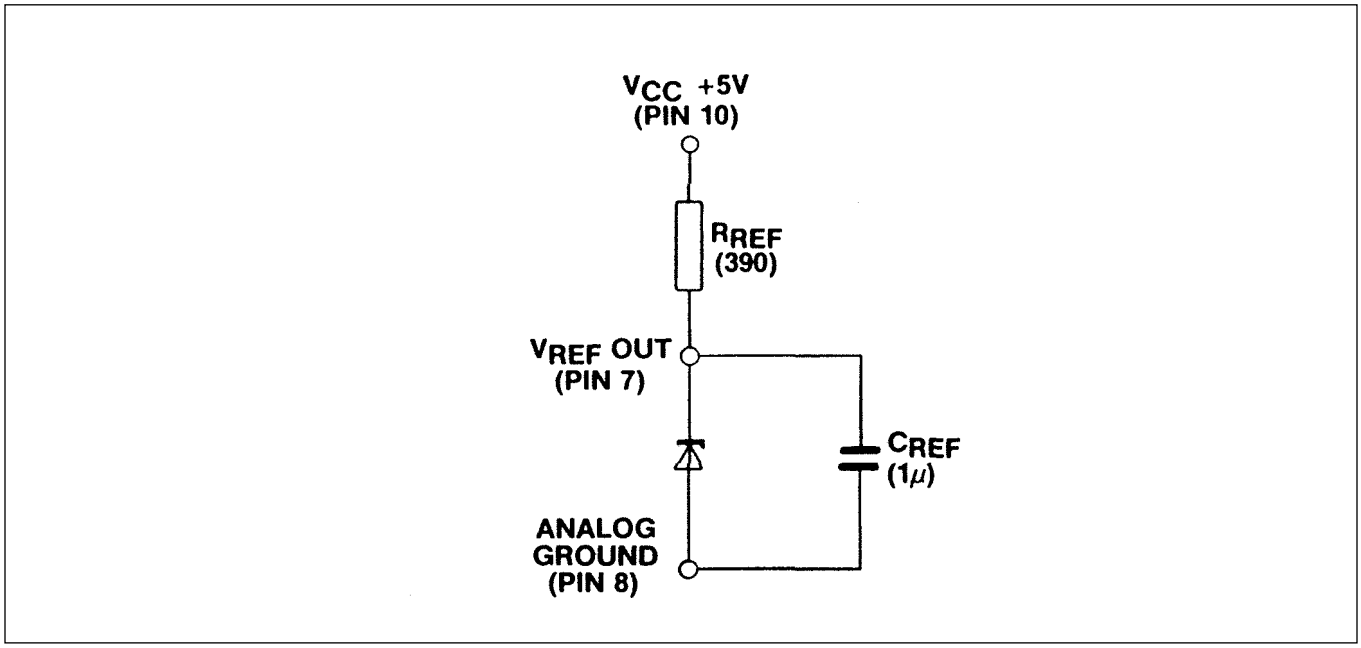


Fig.5 Internal voltage reference

Up to five ZN428s may be driven from one internal reference (there is no need to reduce R_{REF}). This useful feature saves power and gives excellent gain tracking between the converters.

(b) External Reference

If required an external reference voltage may be connected to $V_{REF\ IN}$. The slope resistance of such a reference should be less than $\frac{2.5}{n}\ \Omega$, where n is the number of converters supplied.

$V_{REF\ IN}$ can be varied from 0 to +3V for ratiometric operation. The ZN428 is guaranteed monotonic for $V_{REF\ IN}$ above 2V.

LOGIC

Input coding is binary for unipolar operation and offset binary for bipolar operation. When the $\overline{\text{ENABLE}}$ input is low the data inputs drive the D to A directly. When $\overline{\text{ENABLE}}$ goes high the input data word is held in the data latch.

The equivalent circuit for the data and clock inputs is shown in Fig.6.

The ZN428 is provided with separate analog and digital ground connections. The circuit will operate correctly with as much as ±200mV between the two grounds.

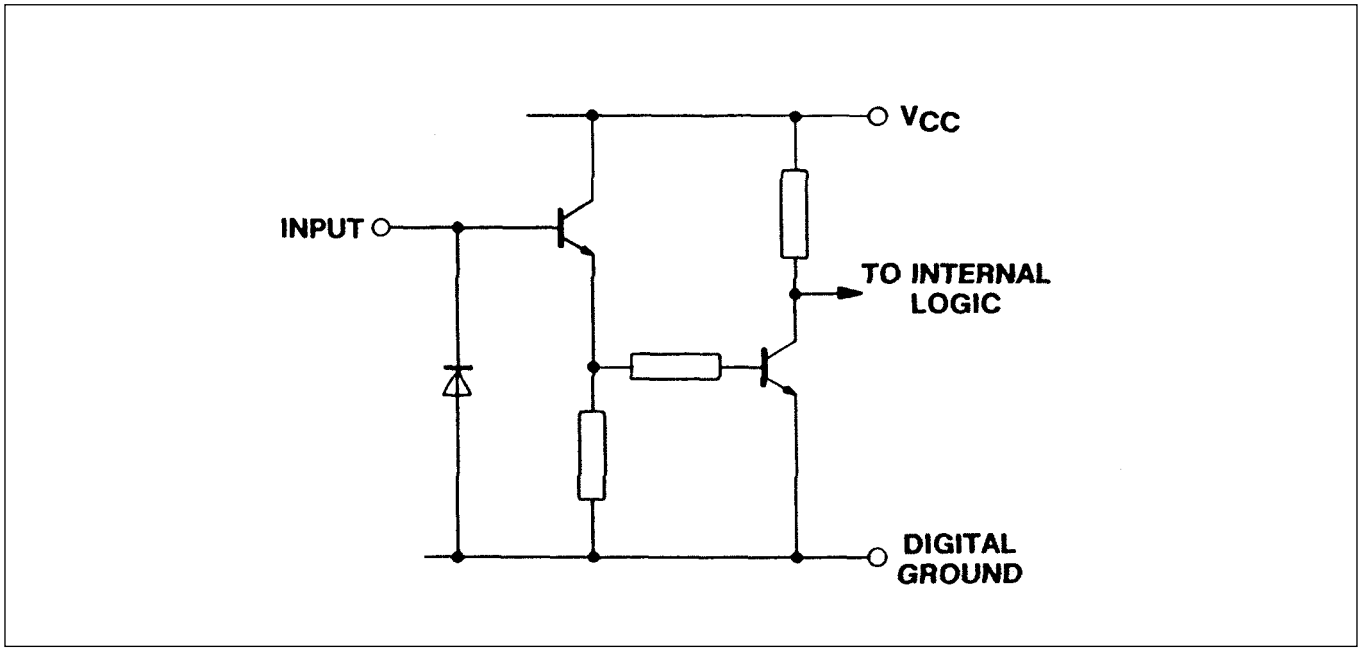


Fig.6 Equivalent circuit of all inputs

OPERATING NOTES

(1) Unipolar D-A Converter

The nominal output range of the ZN428 is 0 to $V_{REF\ IN}$ through a 4Ω resistance. Other output ranges can readily be obtained by using an external amplifier.

The general scheme (Fig.7) is suitable for amplifiers with input bias currents less than 1.5μA.

The resulting full-scale range is given by:

$$V_{OUT}\ FS = \left(1 + \frac{R1}{R2}\right) V_{REF\ IN} = G.V_{REF\ IN}$$

The impedance at the inverting input is R1//R2 and for low drift with temperature this parallel combination should be equal to the ladder resistance (4kΩ). The required nominal values of R1 and R2 are given by R1 = 4GkΩ and R_2 = 4G/(G-1)kΩ.

Using these relationships a table of nominal resistance values for R_1 and R_2 can be constructed for $V_{REF\ IN}$ = 2.5V.

Output Range	G	R_1	R_2
+5V	2	8kΩ	8kΩ
+10V	4	16kΩ	5.33kΩ

For gain setting R_1 is adjusted about its nominal value. Practical circuit realisations (including amplifier stabilising components) for +5 and +10V output ranges are given in Fig.8. Settling time for a major transition is 1.5μs typical.

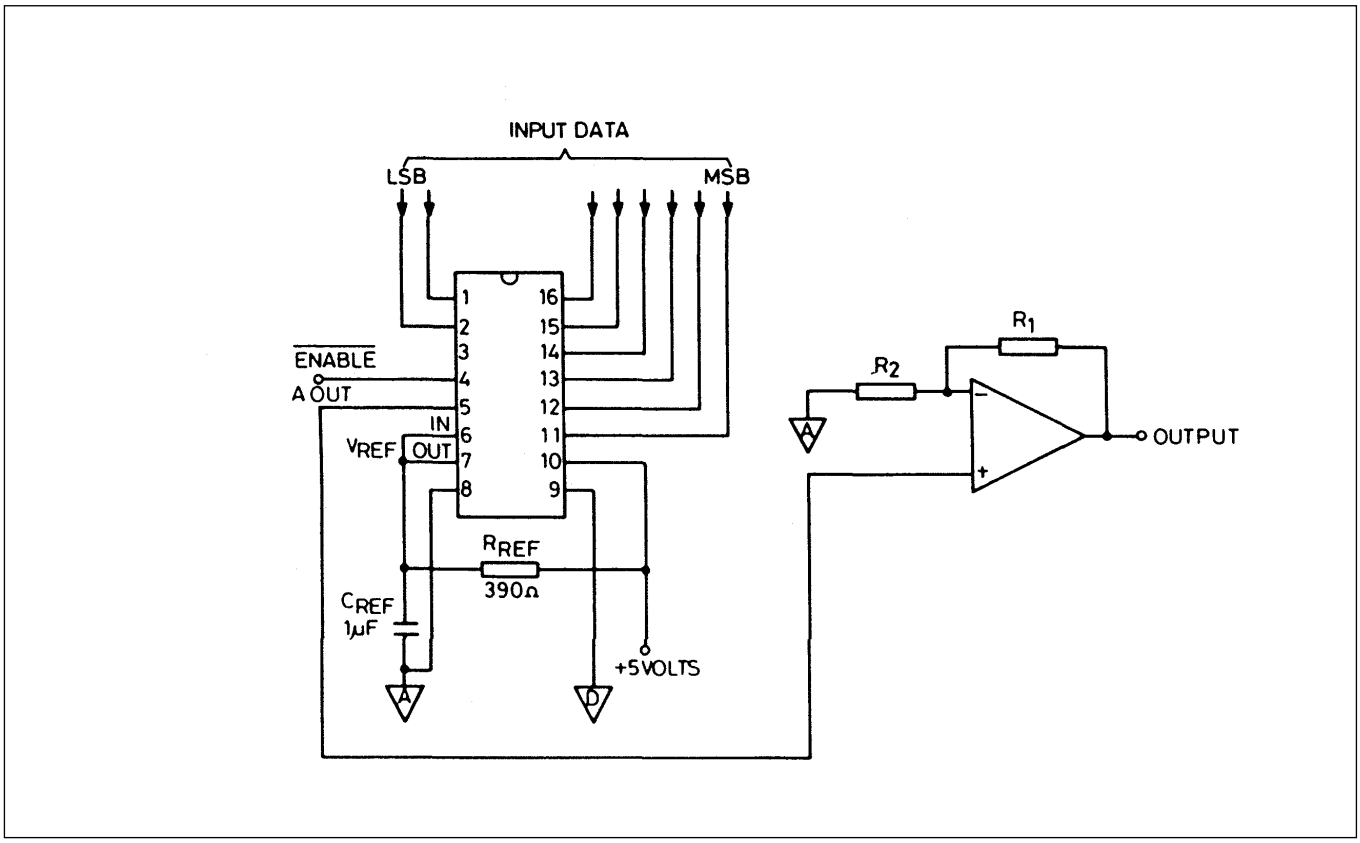


Fig.7 Unipolar operation - basic circuit

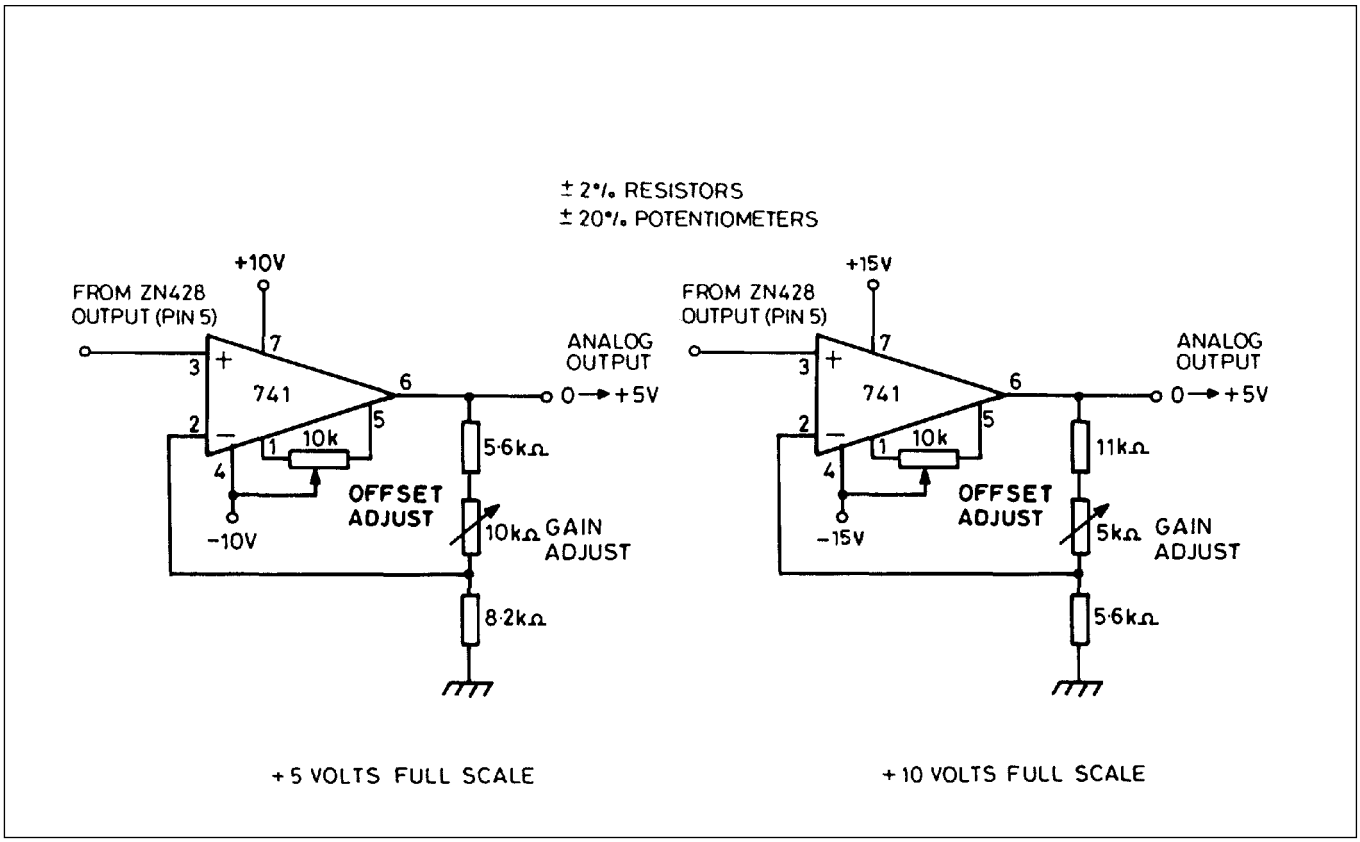


Fig.8 Unipolar operation - component values

UNIPOLAR ADJUSTMENT PROCEDURE

(i) Set all bits to OFF (low) with $\overline{\text{ENABLE}}$ low and adjust zero until V_{OUT} = 0.0000V.

(ii) Set all bits ON (high) and adjust gain until V_{OUT} = FS - 1LSB.

UNIPOLAR SETTING UP POINTS

Output Range, +FS	LSB	FS - 1LSB
+5V	19.5 mV	4.9805V
+10V	39.1mV	9.9609V

$$1LSB = \frac{FS}{256}$$

UNIPOLAR LOGIC CODING

Input Code (Binary)	Analog Output (Nominal Value)
11111111	FS - 1LSB
11111110	FS - 2 LSB
11000000	$^3/_4$ FS
10000001	$^1/_2$ FS + 1LSB
10000000	$^1/_2$ FS
01111111	$^1/_2$ FS - 1LSB
01000000	$^1/_4$ FS
00000001	1LSB
00000000	0

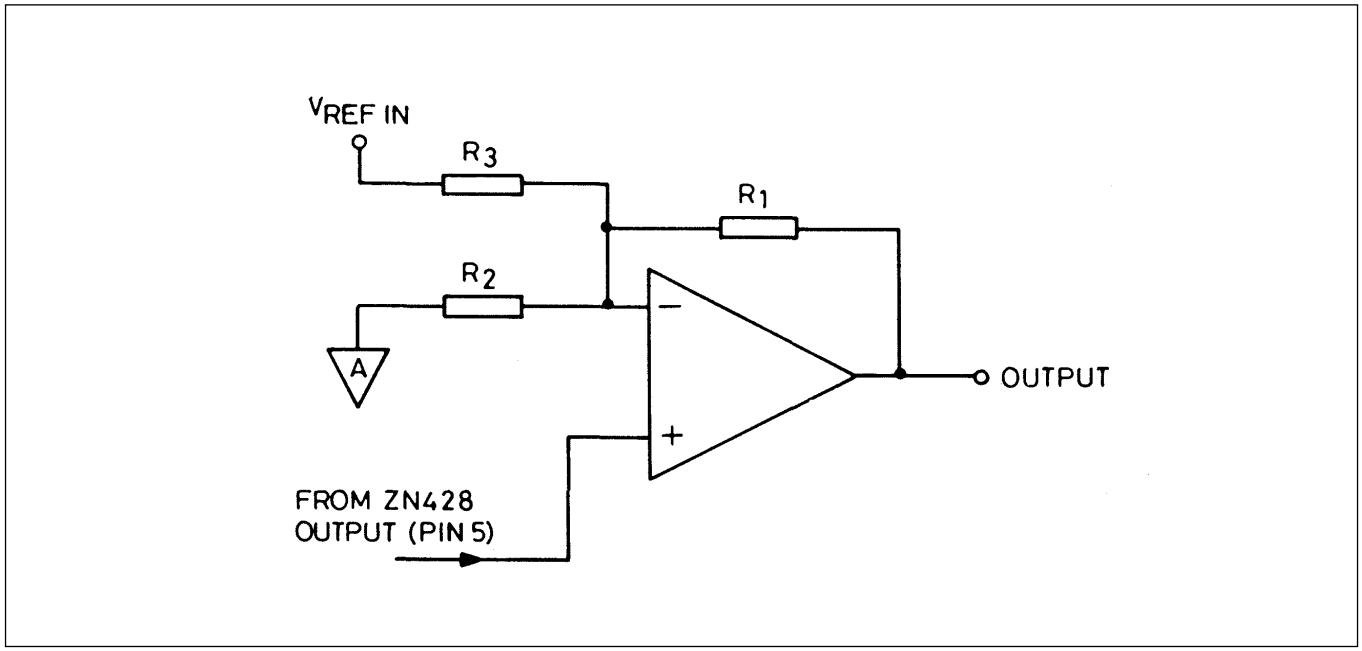


Fig.9 Bipolar operation - basic circuit

(2) Bipolar D-A Converter

For bipolar operation the output from the ZN428 is offset by half full-scale by connecting a resistor R3 between $V_{REF\ IN}$ and the inverting input of the buffer amplifier (Fig.9).

When the digital input to the ZN428 is zero the analog output is zero and the amplifier output should be -Full-scale. An input of all ones to the D-A will give a ZN428 output of $V_{REF\ IN}$ and the amplifier output required is +Full-scale. Also, to match the ladder resistance the parallel combination of R_1, R_2 and R_3 should be 4kΩ.

The nominal values of R_1, R_2 and R_3 which meet these conditions are given by

$R_1 = 8Gk\Omega$, $R_2 = 8G/(G-1)k\Omega$ and $R_3 = 8k\Omega$.

where the resultant output range is $\pm G\ V_{REF\ IN}$. A bipolar output range of $\pm V_{REF\ IN}$ (which corresponds to the basic unipolar range 0 to $V_{REF\ IN}$) is obtained if $R_1 = R_3 = 8k\Omega$ and $R_2 = \infty$.

Assuming that $V_{REF\ IN}$ = 2.5V the nominal values of resistors for ±5 and ±10V output ranges are given in the following table:

Output Range	G	R_1	R_2	R_3
+5V	2	16kΩ	16kΩ	8kΩ
+10V	4	32kΩ	10.66kΩ	8kΩ

Minus full scale (0ffset) is set by adjusting R_1 about its nominal value relative to R_3. Plus full-scale (gain) is set by adjusting R_2 relative to R_1.

Practical circuit realisations are given in Fig.10.

Note that in the ±5V case R_3 has been chosen as 7.5kΩ (instead of 8.2kΩ) to get a more symmetrical range of adjustment using standard potentiometers. Settling time for a major transition is 1.5µs typical.

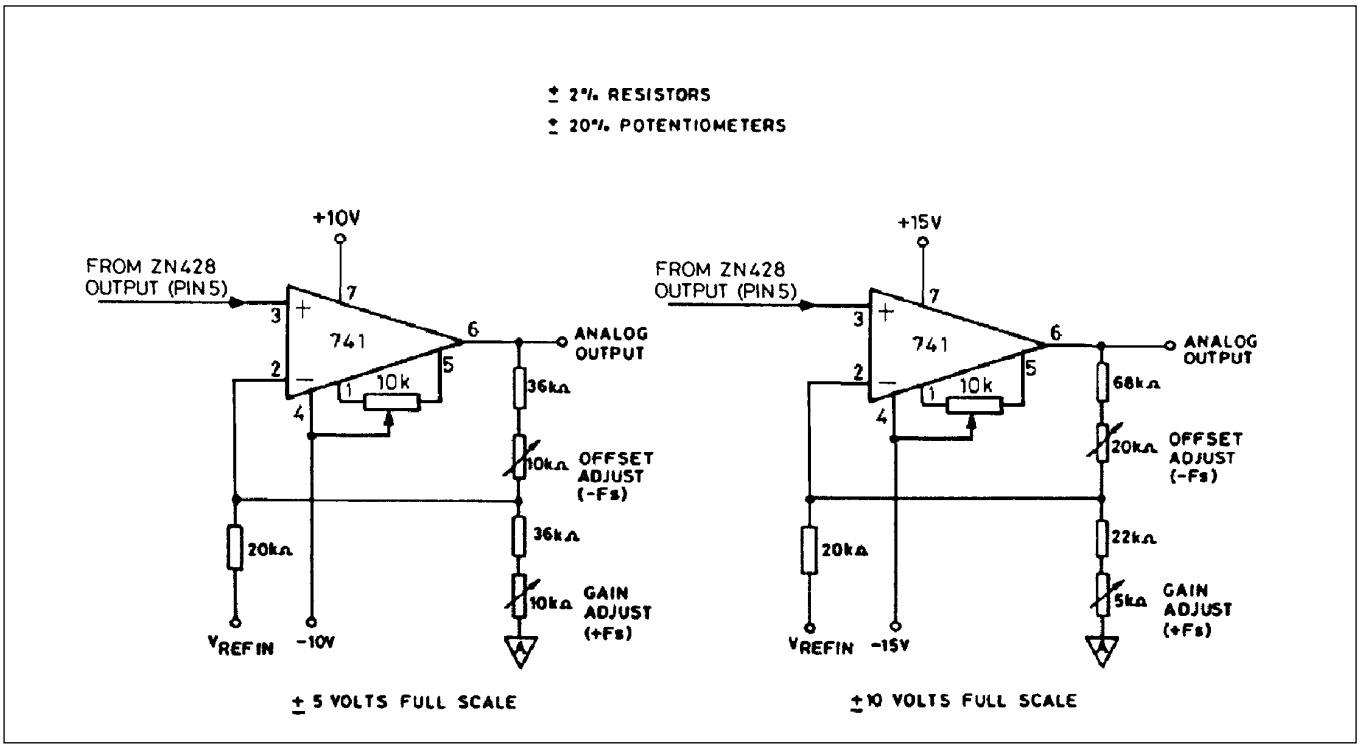


Fig.10 Bipolar operation - component values

BIPOLAR ADJUSTMENT PROCEDURE

(i) Set all bits to OFF (low) with $\overline{\text{ENABLE}}$ low and adjust offset until the amplifier output reads -full-scale.

(ii) Set all bits ON (high) and adjust gain until the amplifier output reads +(full-scale - 1LSB).

BIPOLAR SETTING UP POINTS

Input Range, ± FS	LSB	-FS	+(FS - 1LSB)
±5V	39.1 mV	-5.0000V	+4.9609V
±10V	78.1mV	-10.0000V	9.9219V

$1LSB = \frac{2FS}{256}$

BIPOLAR LOGIC CODING

Input Code (Offset Binary)	Analog Output (Nominal Value)
11111111	+(FS - 1LSB)
11111110	+(FS - 2 LSB)
11000000	$+^1/_2$ FS
10000001	+ 1LSB
10000000	0
01111111	-1 LSB
01000000	$-^1/_2$ FS
00000001	-(FS - 1LSB)
00000000	-FS

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