FAIRCHILD
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Application Note 42040

Applying the ML6431 Video Genlock Using the ML6430/ML6431 Evaluation Kit

GENERAL DESCRIPTION

The ML6430/6431 Evaluation Board contains a single package IC Genlock capable of correcting for VCR glitches and head switching, tape dropouts, missing sync pulses, freeze frames, high speed playback, and camcorder gyro errors. It also generates sampling frequencies for video and audio along with signals for both horizontal and vertical signal processing. All of this is available in PAL, NTSC, and some VGA formats. The ML6431 differs from the ML6430 in its internal register structures.

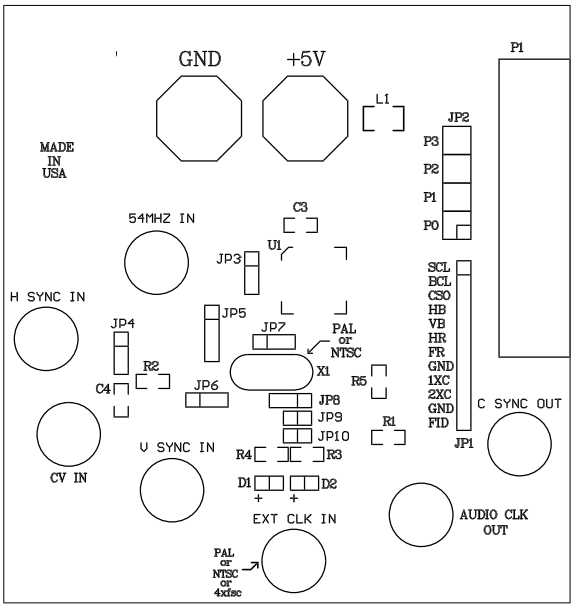
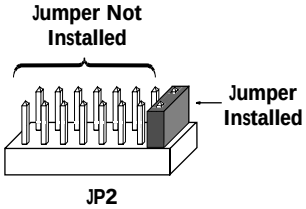


Figure 1. Silkscreen, Component Side, Showing JP2



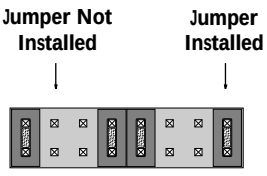


Figure 2a. NTSC Preset

Figure 2b. PAL Preset

Figure 2c. Register Control

Figure 2. JP2 Configurations

THEORY OF OPERATION

The ML6430/ML6431 contains an oscillator, two phase locked loops, registers, a serial port, and pulse generating circuits for the control of both analog and digital video systems. For proper operation this IC requires two different inputs: a reference frequency, and one or two video inputs.

The reference frequency can be produced in any one of four ways. A PAL color subcarrier crystal at 4.43 MHz, or an NTSC subcarrier crystal at 3.58 MHz, connected between pins 11 and 12 will generate all internal timing signals. Also, a separate systems clock at either 4X PAL (*i.e.*, 17.72 MHz) or 4X NTSC (*i.e.*, 14.32 MHz) will also work. Any one of the four will produce complete PAL or NTSC timing. This Evaluation Kit uses an NTSC crystal for reference generation. Certain VGA timings can only be produced with a PAL crystal, others only with an NTSC crystal. A PAL crystal is included so that all the VGA timing illustrated in this document can be produced. The video input can be Composite Video (CV) or separate Horizontal and Vertical TTL level sync signals for interlaced NTSC or PAL.

Table 1, "VGA Rates Supported", shows the configuration for generating VGA timing. The Evaluation Board must first be set up for internal register control (see the following paragraph "Internal Register Control"). The shorting plug on JP4 must be moved up so that H SYNC IN is connected to C_{VIN}/H_{SYNC} on the ML6431. A horizontal clock equal to the horizontal frequency in Table 1 is applied to the H SYNC IN. The ML6431 data registers are loaded with the values from Table 1. If the crystal on the Evaluation Board is the same as the "External Xtal Value" in Table 1 then the pixel frequency and all other locked signals will be found at JP1.

EVALUATION KIT OPERATION

The Evaluation kit circuit board is preset for the NTSC square pixel mode when shipped. Figures 1 and 2a show that preset. In Europe the preset can be changed to the PAL mode. See Figures 1 and 2b. Should a change in mode become necessary only one shorting bar needs to be changed. For all possible preset modes see Table 7 of the Product Data Sheet.

To place the circuit board in operation, a 5 Volt power supply capable of supplying 0.5 Amps should be connected to the banana jack labeled +5V. The return lead should be connected to the banana jack labeled GND. The Signal Absent lamp (D1), the one on the left, will light. Applying a composite video signal to the input BNC connector will cause the Signal Absent lamp to extinguish and the Locked lamp (D2) to light. At this point all of the signals shown in Figures 3 and 5 for NTSC, or Figures 4 and 5 for PAL will be available at header JP1 on the right side of the Evaluation Board.

Performance verification consists of applying noisy composite video signals to the input and noting the effect on the output signals at header JP1.

INTERNAL REGISTER CONTROL

Full control of all of the ML6430/6431 features is possible through the serial port of the ML6430/6431. To demonstrate the control available connect a printer cable from the parallel port of a PC running DOS or WINDOWS to P1 on the Evaluation BOARD. JP2 should be configured as shown in Figures 1 and 2c. All other connections are as they were in the full preset mode. The software included in the kit is listed in this document. The executable software is loaded in the usual way: typing "Video" and pressing the Enter key. After a short time the instrument control panel appears on the screen (see Figure 10). All the available function modifications can be seen by either using a mouse to click on the choices or using the Tab, arrow, and Enter keys. To leave the program press the Escape key. See Table 2 for a list of the choices with comments.

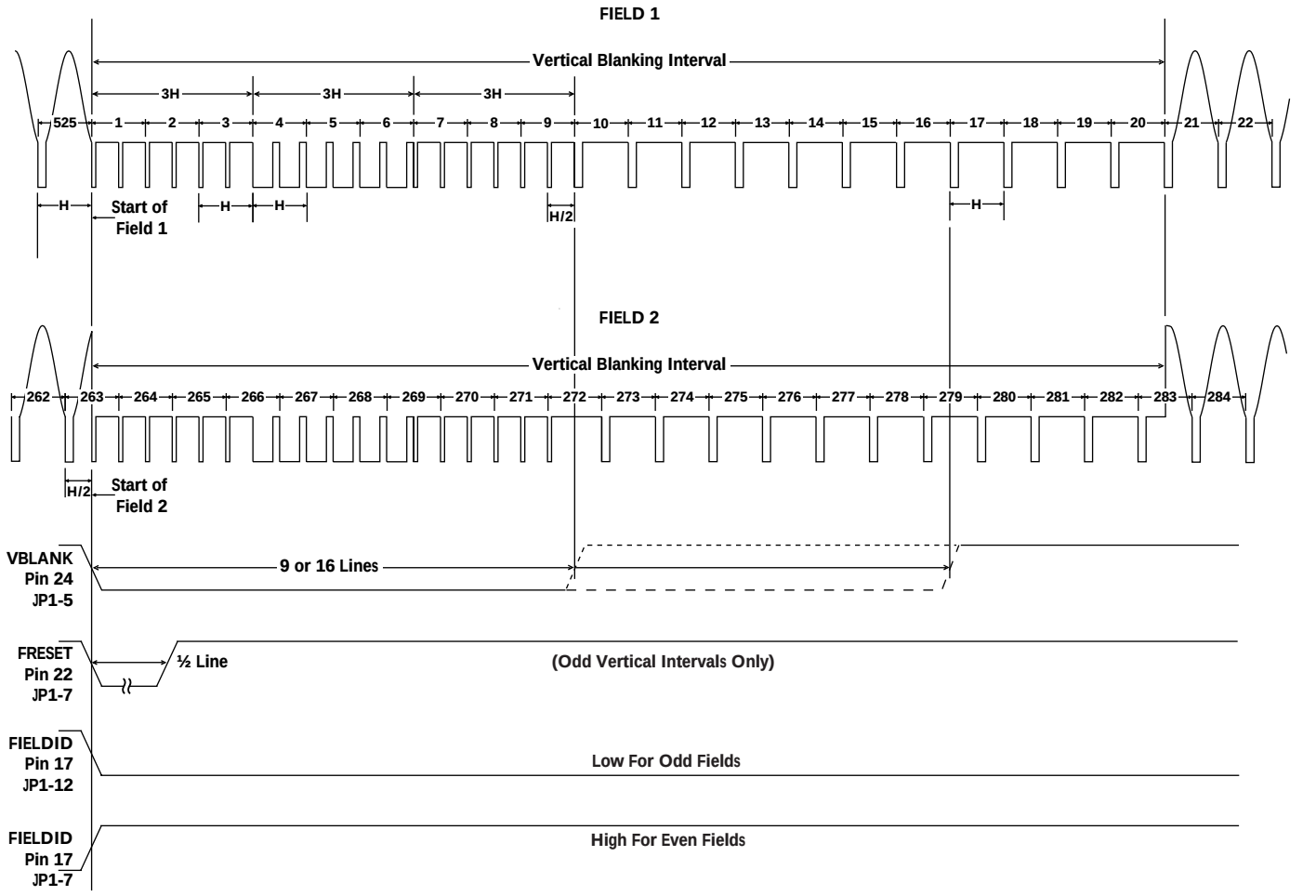


Figure 3. NTSC Field Rate Waveforms

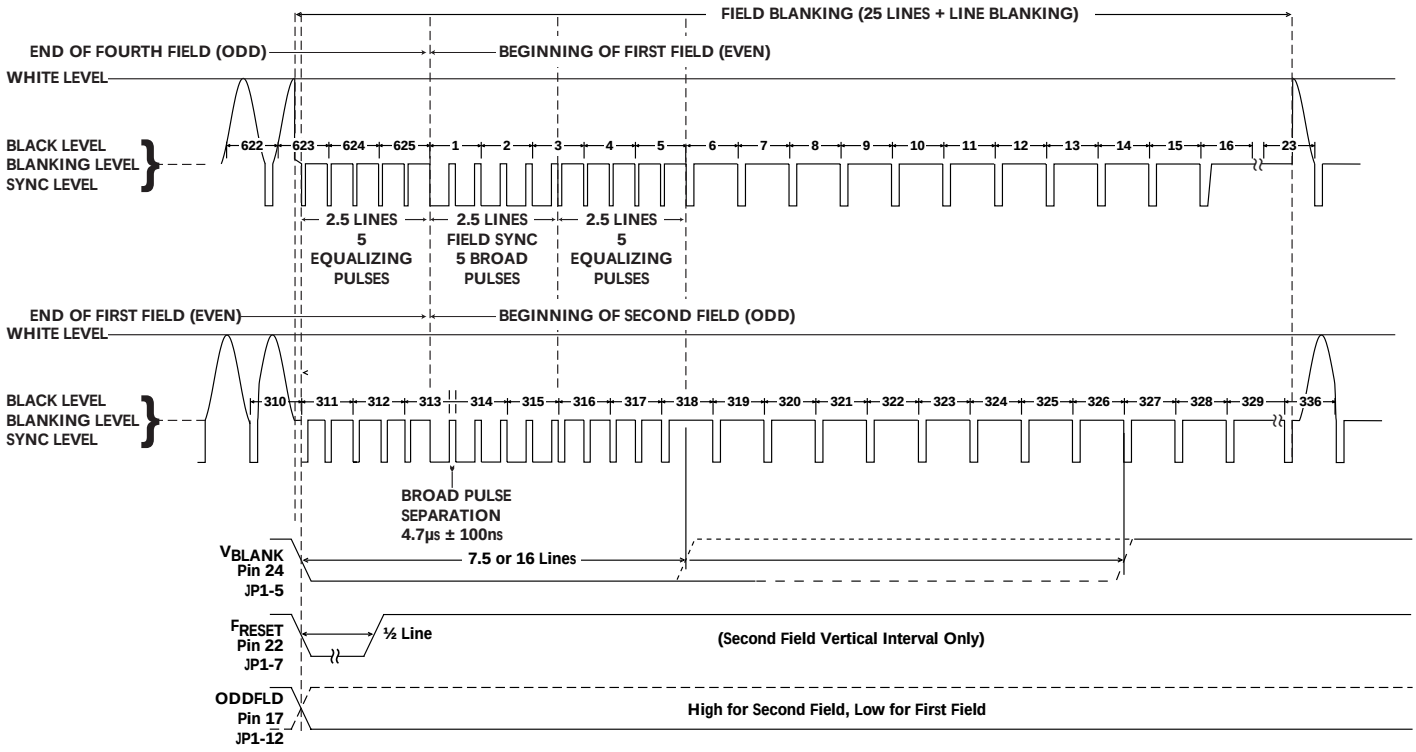


Figure 4. PAL 625 Field Rate Waveforms

							ML6431 Data Register Settings*								
Resolution	**# Pixels per Line**	**Refresh Rate**	**Horizontal Frequency**	**Pixel Frequency**	**Standard Type**	**Original Standard #**	**Freq. Std.**	**PALXtal**	**Pixel Reg**	**PherrOut**	**VGA**	**External Xtal Used**	**Pixel Clk Output**	**Horizontal Pulses**	**Vertical Pulses**
640 x 480	800	60 Hz	31.5 KHz	25.175 MHz	Industry		NTSC Sq Pix =000	1	572	0	1	4.43	2X	"Hsync,Hreset"	Vreset
	832	72 Hz	37.9 KHz	31.500 MHz	VESA	VS901101	NTSC Sq Pix =000	0	640	0	1	4.43	2X	"Hsync,Hreset"	Vreset
	840	75 Hz	37.5 KHz	31.500 MHz	VESA	VDMT75HZ	NTSC Sq Pix =000	0	656	0	1	4.43	2X	"Hsync,Hreset"	Vreset**
800 x 600	1024	56 Hz	35.1 KHz	36.000 MHz	VESA	VG900601	PAL 4FSC =101	1	512	1	1	4.43	4X	"Hsync,Hreset"	Vreset
	1056	60 Hz	37.9 KHz	40.000 MHz	VESA	VG900602	NTSC Sq Pix =000	1	544	1	1	3.58	4X	"Hsync,Hreset"	Vreset**
	1040	72 Hz	48.1 KHz	50.000 MHz	VESA	VS900603A	NTSC Sq Pix =000	1	528	1	1	4.43	4X	"Hsync,Hreset"	Vreset**
	1056	75 Hz	46.9 KHz	49.500 MHz	VESA	VDMT75HZ	NTSC Sq Pix =000	1	544	1	1	4.43	4X	"Hsync,Hreset"	Vreset**
1024 x 768	1264	43 Hz/Int	35.5 KHz	44.900 MHz	Industry		PAL 4FSC =101	0	752	1	1	4.43	4X	"Hsync,Hreset"	Vreset**
	1344	60 Hz	48.4 KHz	65.000 MHz	VESA	VG901101A	PAL 601 = 011	0	832	1	1	4.43	4X	"Hsync,Hreset"	Vreset**
	1328	70 Hz	56.5 KHz	75.000 MHz	VESA	VS910801-2	PAL 4FSC =101	0	816	1	1	3.58	4X & clk doubler	No	No

*For Data Register Settings: TTL = High, VGA = On, VCR = Off, Noise Gating = On, Dis Auto Ver Det = 1

** w/ external glue logic

Table 1. VGA Rates Supported

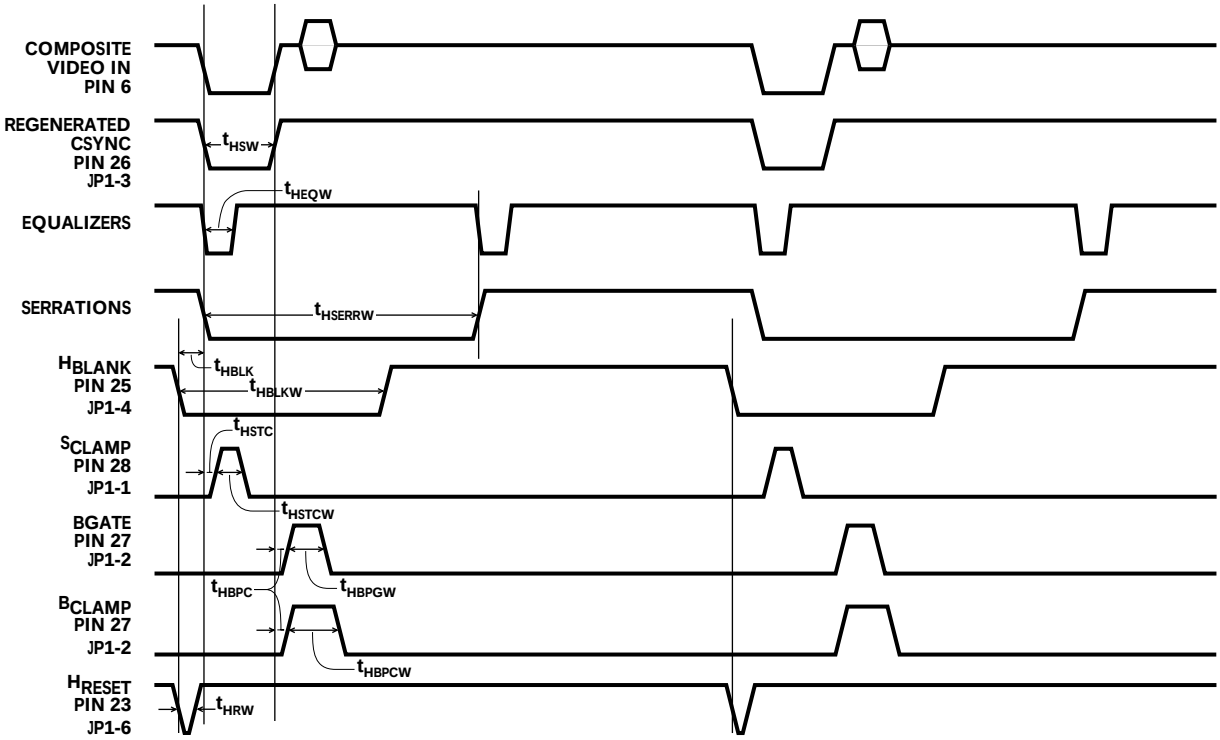


Figure 5. Line Rate Wave Forms

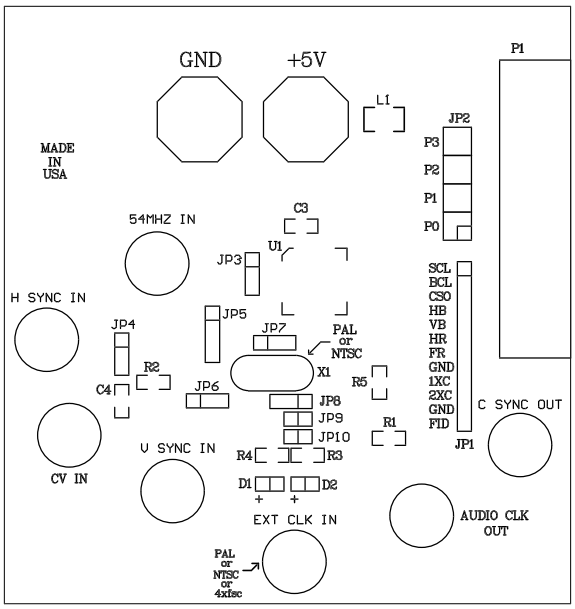


Figure 6. Top Silkscreen

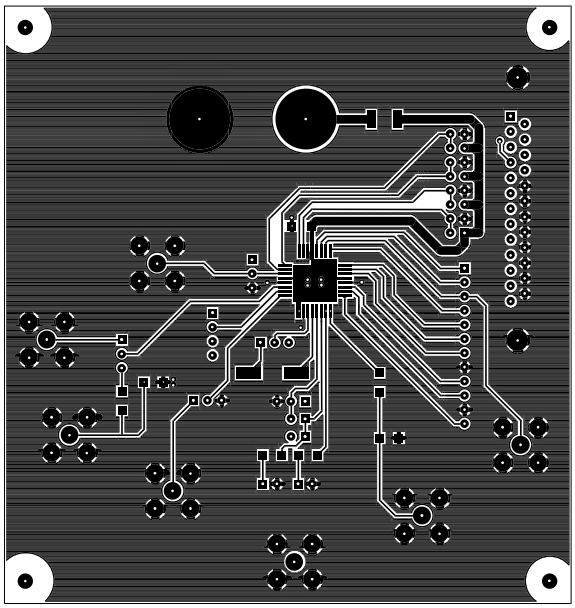


Figure 7. Top Layer

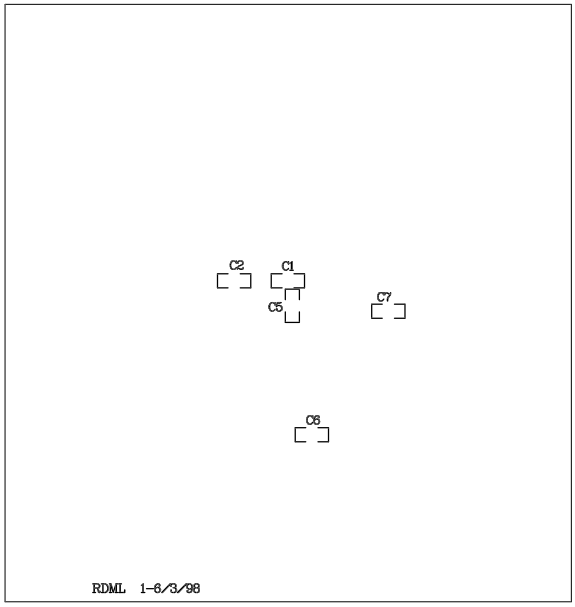


Figure 8. Bottom Silkscreen

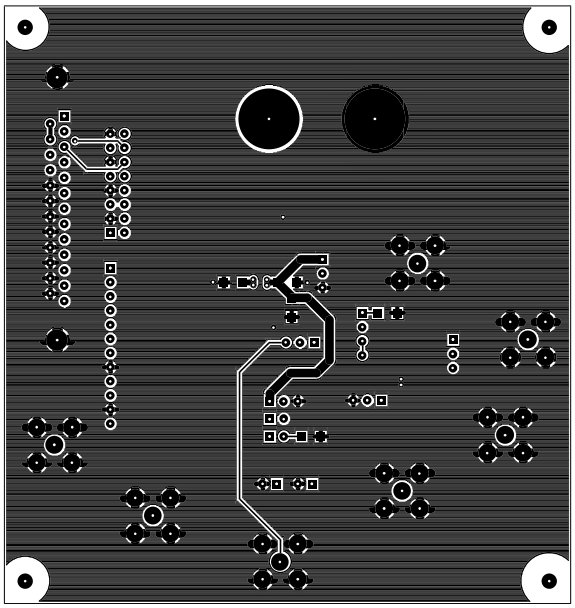


Figure 9. Bottom Layer)

Mode:	Sets IC for PAL or NTSC
Crystal:	Sets IC to crystal frequency
Audio Freq:	Sets audio clock frequency
Sleep:	Turns IC on or off
TTL:	Switches Input from CV to Horizontal/Vertical
Threshold:	Sets " out of lock " threshold
VGA:	Forces IC into VGA mode
VCR:	Forces IC into VCR mode
Frequency:	Clock: 1? or 4?
Pixels:	Sets the number of pixels per line
Horizontal Delay:	Sets the delay between Hsync pulse and all other pulses
Clamp Pulses	
Polarity:	Normal or inverted
Burst:	Sets IC to produce Burst Gate clamp or Back Porch clamp
Mode:	Derives clamp from raw or regenerated sync
Sync Pulses	
Polarity:	Normal or inverted
Csync:	Regenerated or raw sync
Blanking Pulses	
Polarity:	Normal or inverted
Width:	Narrow or wide
Test Modes	
Noise Gating:	Turns Noise Gating on and off
Rst Commutator:	Test only
Ext Clock:	Allows external clock
Dis Auto Vcr Det:	Disable VCR detect
Pherr Out:	Phase Error
ML6440 Comb Filter	
Chip not on this board	

Table 2. Meaning of the Labwindows Display Panel Labels

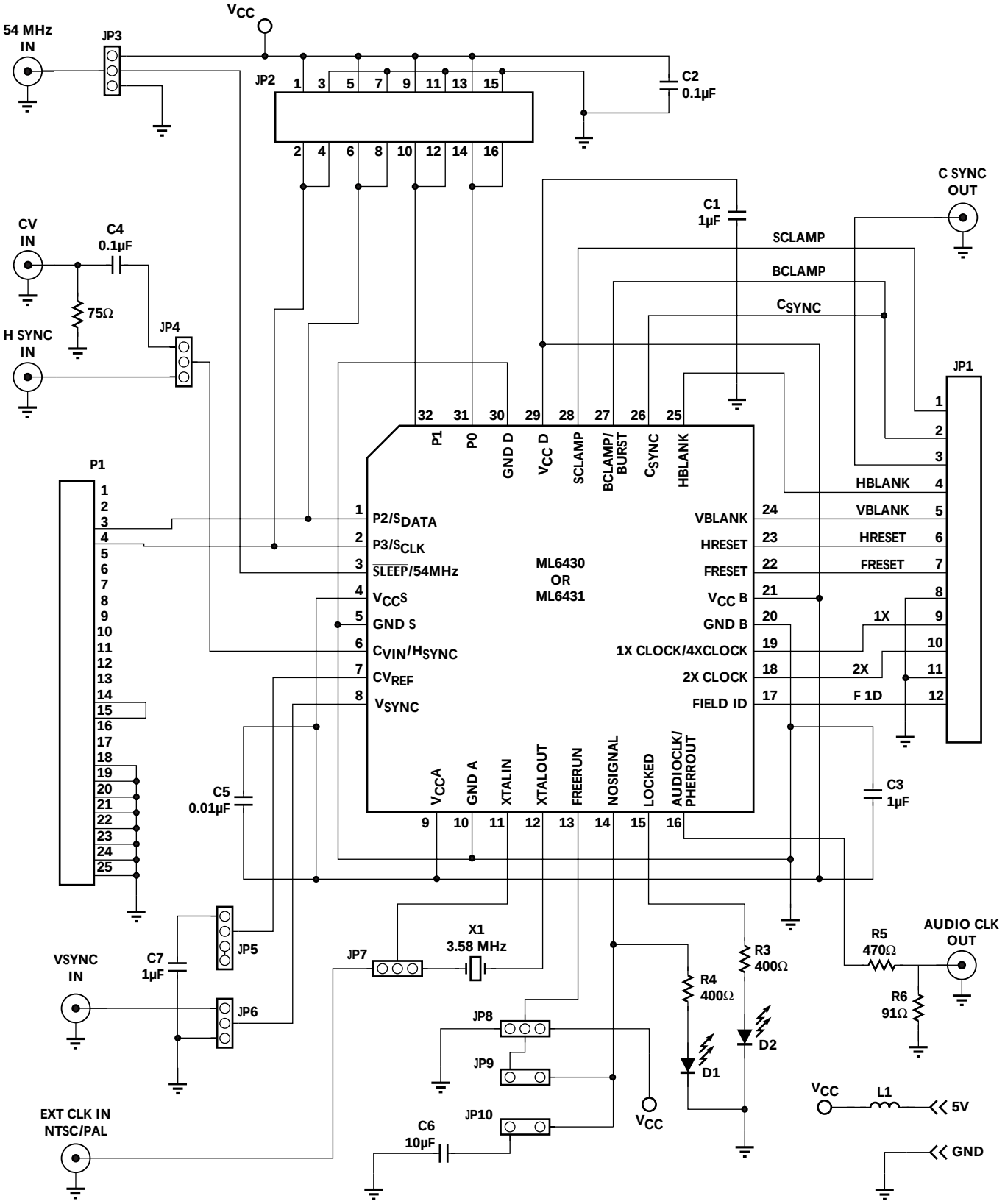


Figure 10. Schematic of the ML6430/6431 Evaluation Board)

ML6430/6431 EVALUATION KIT PARTS LIST

ITEM	QTY	DESCRIPTION	VENDOR / P.N.	DESIGNATION
RESISTORS				
1	1	91Ω, 5%, 1206	Any	R1
2	1	75Ω, 5%, 1206	Any	R2
3	2	330Ω, 5%, 1206	Any	R3, R4
4	1	470Ω, 1%, 1206	Any	R5
CAPACITORS				
1	1	0.01µF, 6V or more 1206	Any	C5
2	1	0.1µF, 6V or more 1206	Any	C2, C4
3	3	1.0µF, 6V or more 1206	Any	C1, C3, C7
4	2	10.0µF, 6V or more 1206	Any	C6
DIODES				
8	2	LEDs	Digi-Key / P407-ND	D1, D2
ICS				
9	1	Gen Lock	Micro Linear / ML6430/6431	U1
OTHER				
10	1	3.58MHz Crystal	Ecliptek / EC2 SM-3.579545M	X1
11	1	Test Point Header, 12 Pin	Digi-Key / WM4010-ND	JP1
12	1	Jumper Header, Dual 8 Pin	Digi-Key / S2012-8-ND	JP2
13	1	DB-25 Connector, Female, Board Mounting	Digi-Key / 325F-ND	P1
14	7	BNC Connector	A/D Electronics / 580-002-00	Several
15	2	Banana Plug	Digi-Key / 108-0740-001	na
16	1	Test Point Header, 4 Pin	Digi-Key / WM4010-ND	JP5
17	5	Test Point Header, 3 Pin	Digi-Key / WM4010-ND	JP4, JP4, JP6, J[7,JP8
18	2	Test Point Header, 2 Pin	Digi-Key / WM4010-ND	JP9, JP10
19	1	Ferrite Bead	Digi-Key / 240-1030-1-ND	L1
20	1	4.43 MHz Crystal	Ecliptek / EC2-4.4336M	X1 Alternate