FAIRCHILD
A Schlumberger Company

DAC08
8-Bit Multiplying D/A Converter

Linear Division Data Acquisition

Description

The DAC08 is an 8-bit multiplying digital-to-analog converter constructed using the Fairchild Planar Epitaxial process. Advanced circuit design achieves very high speed performance with outstanding applications capability and low cost.

- **Fast Settling Time To 1/2 LSB 85 ns**
- **Full Scale Current Prematched To ±1 LSB**
- **Direct Interface To TTL, CMOS, ECL, HTL, PMOS, DTL**
- **Linearity To ±0.19% Max Over Temperature Range**
- **High Output Compliance −10 V To +18 V**
- **True And Complemented Outputs**
- **Wide Range Multiplying Capability**
- **Low Full Scale Current Drift +10 ppm/°C TYP**
- **Wide Power Supply Range ±4.5 V To ±18 V**
- **Low Power Consumption 33 mW at ±5 V**
- **External Compensation For Max Bandwidth**
- **Low Cost**

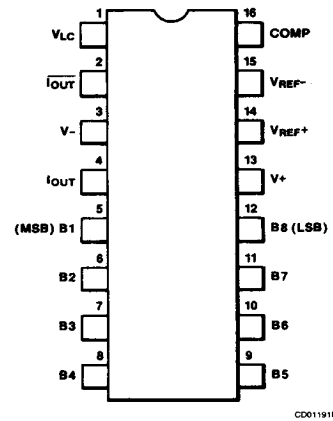
Absolute Maximum Ratings

Storage Temperature Range	
Ceramic DIP	−65°C to +175°C
Molded DIP	−65°C to +150°C
Operating Temperature Range	
Extended (DAC08M)	−55°C to +125°C
Commercial (DAC08C)	0°C to 70°C
Lead Temperature	
Ceramic DIP (soldering, 60 s)	300°C
Molded DIP (soldering, 10 s)	265°C
Internal Power Dissipation[1, 2]	
16L-Ceramic DIP	1.50 W
16L-Molded DIP	1.04 W
V+ to V−	36 V
Logic Inputs	V− to (V−) + 36 V
V_{LC}	V− to V+
Reference Inputs (V_{14}, V_{15})	V− to V+
Reference Input Differential Voltage (V_{14}, V_{15})	±18 V
Reference Input Current I_{REF} (14)	5.0 mA

Notes

1. $T_{J\ Max}$ = 150°C for the Molded DIP, and 175°C for the Ceramic DIP.
2. Ratings apply to ambient temperature at 25°C. Above this temperature, derate the 16L-Molded DIP at 8.3 mW/°C, the 16L-Ceramic DIP at 10 mW/°C.

Connection Diagram
16-Lead DIP
(Top View)



Order Information

Device Code	Package Code	Package Description
DAC08DM	7B	Ceramic DIP
DAC08EDC	7B	Ceramic DIP
DAC08EPC	9B	Molded DIP
DAC08CDC	7B	Ceramic DIP
DAC08CPC	9B	Molded DIP

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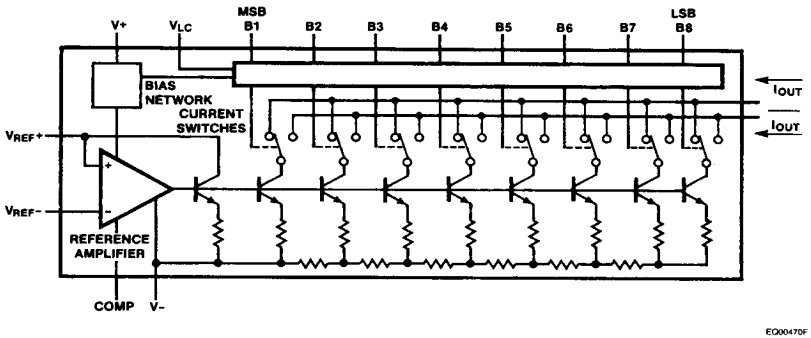
Block Diagram



DAC08, DAC08E, and DAC08C

Electrical Characteristics $T_A = 0°C$ to $70°C$ for the DAC08E and DAC08C, $-55°C$ to $+125°C$ for the DAC08; $V_{CC} = \pm 15$ V, $I_{REF} = 2.0$ mA. Output characteristics refer to both I_{OUT} and $\overline{I_{OUT}}$.

Symbol	Characteristic	Condition		Min	Typ	Max	Unit
RESO	Resolution			8.0	8.0	8.0	bits
MONO	Monotonicity			8.0	8.0	8.0	bits
NL	Nonlinearity	DAC08, DAC08E				±0.19	% FS
		DAC08C				±0.39	
t_s	Settling Time	To ± ½ LSB, all bits switched, ON or OFF $T_A = 25°C$	DAC08		85	135	ns
			DAC08E/C		85	150	
t_{PLH}	Propagation Delay	$T_A = 25°C$	Each bit		35	60	ns
t_{PHL}			All bits switched		35	60	
TCI_{FS}	Full Scale Temperature Coefficient				±10		ppm/°C
V_{OC}	Output Voltage Compliance	Full scale current change < ½ LSB, $R_O > 20$ mΩ		−10		+18	V
I_{FS4}	Full Scale Current	$V_{REF} = 10.000$ V, R_{14}, $R_{15} = 5.000$ kΩ, $T_A = 25°C$		1.940	1.990	2.040	mA
I_{FSS}	Full Scale Symmetry	$I_{FS4} - I_{FS2}$	DAC08/E		±1.0	±8.0	μA
			DAC08C		±2.0	±16	
I_{ZS}	Zero Scale Current		DAC08/E		0.2	2.0	μA
			DAC08C		0.2	4.0	
I_{FSR}	Output Current Range	$R_{14,\ 15} = 5.000$ kΩ					mA
		$V_{REF} = +15.000$ V, V− = −10 V		2.1			
		$V_{REF} = +25.000$ V, V− = −12 V		4.2			
V_{IL}	Logic Input Voltage LOW	$V_{LC} = 0$ V				0.8	V
V_{IH}	Logic Input Voltage HIGH			2.0			
I_{IL}	Logic Input Current LOW	$V_{LC} = 0$ V, $V_I = -10$ V to $+0.8$ V			−2.0	−10	μA

DAC08 Series (Cont.)
Electrical Characteristics $T_A = 0°C$ to $70°C$ for the DAC08E and DAC08C, $-55°C$ to $+125°C$ for the DAC08; $V_{CC} = \pm 15$ V, $I_{REF} = 2.0$ mA. Output characteristics refer to both I_{OUT} and $\overline{I_{OUT}}$.

Symbol	Characteristic	Condition	Min	Typ	Max	Unit
I_{IH}	Logic Input Current HIGH	$V_I = +2.0$ V to $+18$ V		0.002	10	μA
V_{IS}	Logic Input Swing	V– = –15 V	–10		+18	V
V_{THR}	Logic Threshold Range	$V_{CC} = \pm 15$ V	–10		+13.5	V
I_{15}	Reference Input Bias Current			–1.0	–3.0	μA
dI/dt	Reference Current Slew Rate		4.0	8.0		mA/μS
$PSSI_{FS+}$	Power Supply Sensitivity	V+ = +4.5 V to +18 V, $I_{REF} = 1.000$ mA		0.0003	0.01	%/%
$PSSI_{FS-}$		V– = –4.5 V to –18 V, $I_{REF} = 1.000$ mA		0.002	0.01	
I+	Power Supply Current	$V_{CC} = \pm 5.0$ V, $I_{REF} = 1.000$ mA		2.3	3.8	mA
I–				–4.3	–5.8	
I+		V+ = +5.0 V, $I_{REF} = 2.000$ mA, V– = –15 V		2.4	3.8	
I–				–6.4	–7.8	
I+		$V_{CC} = \pm 15$ V, $I_{REF} = 2.000$ mA		2.5	3.8	
I–				–6.4	–7.8	
P_c	Power Consumption	$V_{CC} = \pm 5.0$ V, $I_{REF} = 1.000$ mA		33	48	mW
		V+ = +5.0 V, V– = –15 V, $I_{REF} = 2.000$ mA		108	136	
		$V_{CC} = \pm 15$ V, $I_{REF} = 2.000$ mA		135	174	

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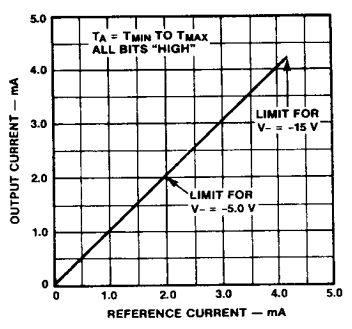
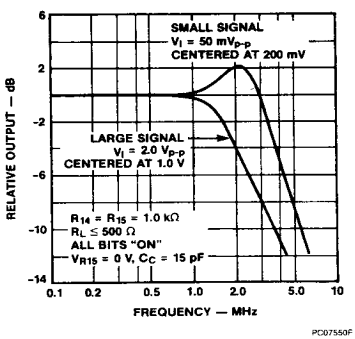
Typical Performance Curves

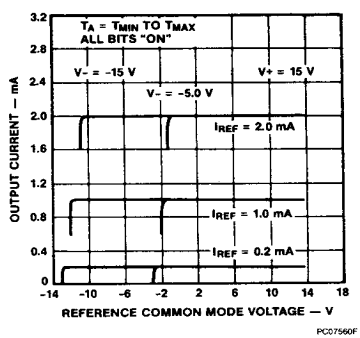
Full Scale Current vs Reference Current



Reference Input Frequency Response



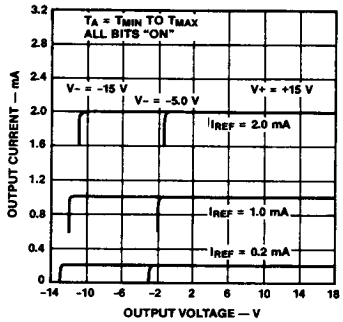
Reference AMP Common Mode Range (Note 1)



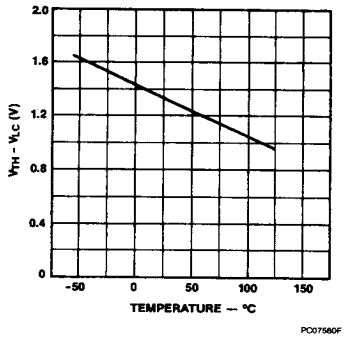
Note
1. Positive common mode range is always (V+) –1.5 V

Typical Performance Curves (Cont.)

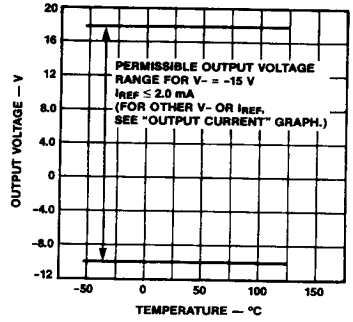
Output Current vs Output Voltage (Output Voltage Compliance)



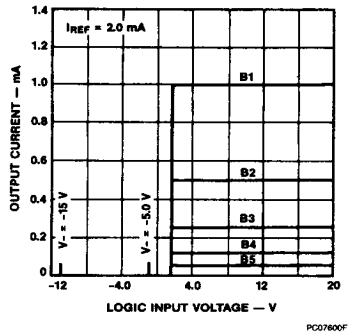
$V_{TH} - V_{LC}$ vs Temperature



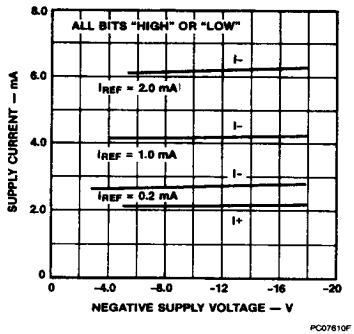
Output Voltage Compliance vs Temperature



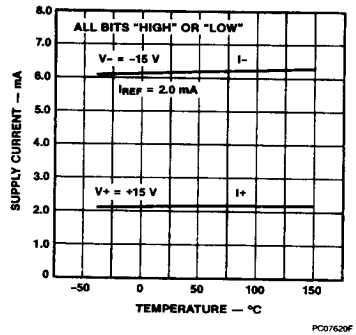
Bit Transfer Characteristics (Note 1)



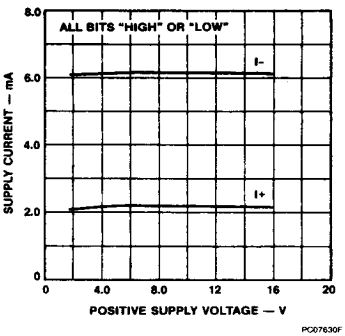
Supply Current vs Negative Supply Voltage



Supply Current vs Temperature



Supply Current vs Positive Supply Voltage

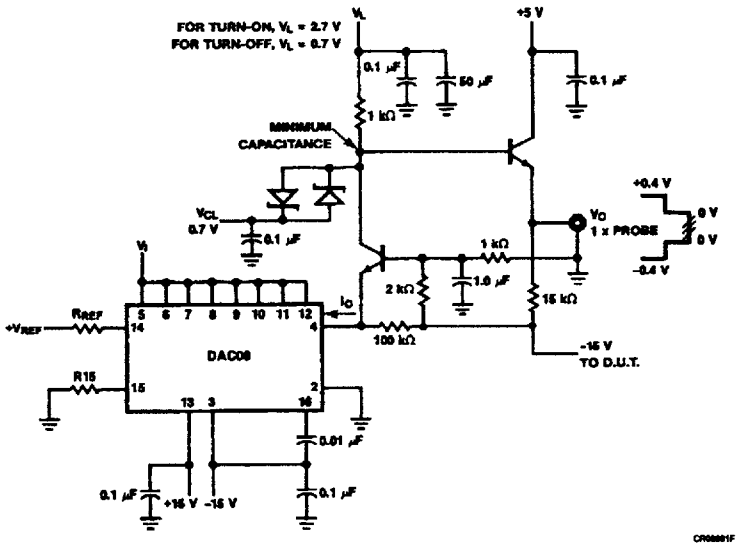


Note

1. B1 through B8 have identical transfer characteristics. Bits are fully switched, with less than 1/2 LSB error. At less than ± 100 mV from actual threshold, these switching points are guaranteed to lie between 0.8 and 2.0 V over the operating temperature range (V_{LC} = 0.0 V).

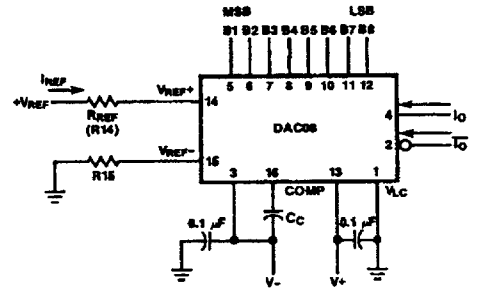
Test Circuits

Figure 1 Settling Time Measurement



Typical Applications

Figure 2 Basic Positive Reference Operation



$$I_{FS} \approx \frac{+V_{REF}}{R_{REF}} \times \frac{255}{256}$$

$I_O + \overline{I_O} = I_{FS}$
For all logic states

For fixed reference, TTL operation, typical values are:
$V_{REF} = +10.000$ V
$R_{REF} = 5\,000$ k
$R_{15} = R_{REF}$
$C_C = 0.01$ µF
$V_{LC} = 0$ V (GROUND)

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Typical Applications (Cont.)

Figure 3 Recommended Full Scale Adjustment Circuit

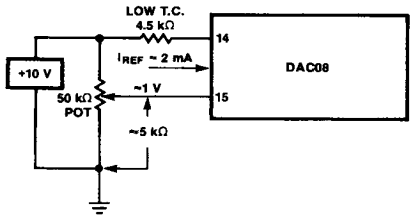
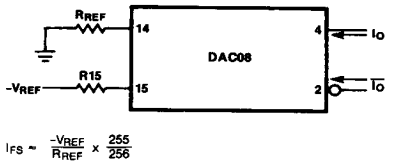


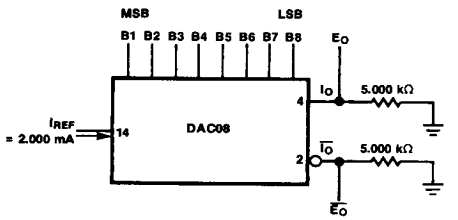
Figure 4 Basic Negative Reference Operation



$$I_{FS} \approx \frac{-V_{REF}}{R_{REF}} \times \frac{255}{256}$$

Note
R_{REF} sets I_{FS}; R15 is for bias current cancellation.

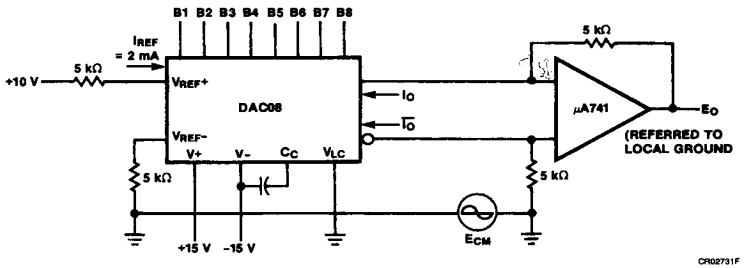
Figure 5 Basic Unipolar Negative Operation



	B1	B2	B3	B4	B5	B6	B7	B8	I_O mA	$\overline{I_O}$ mA	E_O	$\overline{E_O}$
Full Scale	1	1	1	1	1	1	1	1	1.992	.000	−9.960	.000
Full Scale − LSB	1	1	1	1	1	1	1	0	1.984	.008	−9.920	− .040
Half Scale + LSB	1	0	0	0	0	0	0	1	1.008	.984	−5.040	−4.920
Half Scale	1	0	0	0	0	0	0	0	1.000	.992	−5.000	−4.960
Half Scale − LSB	0	1	1	1	1	1	1	1	.992	1.000	−4.960	−5.000
Zero Scale + LSB	0	0	0	0	0	0	0	1	.008	1.984	− .040	−9.920
Zero Scale	0	0	0	0	0	0	0	0	.000	1.992	.000	−9.960

Typical Applications (Cont.)

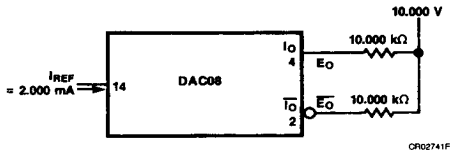
Figure 6 High Noise Immunity Current To Voltage Conversion



Provides isolation from ground loops
Symmetrical ±10 V output
Useful within systems between boards
True complementary/differential current transmission
High speed analog signal transmission

	B1	B2	B3	B4	B5	B6	B7	B8	E_O
Pos Full Scale	1	1	1	1	1	1	1	1	+9.920
Pos Full Scale – LSB	1	1	1	1	1	1	1	0	+9.840
(+) Zero Scale	1	0	0	0	0	0	0	0	+0.040
(–) Zero Scale	0	1	1	1	1	1	1	1	–0.040
Neg Full Scale + LSB	0	0	0	0	0	0	0	1	–9.840
Neg Full Scale	0	0	0	0	0	0	0	0	–9.920

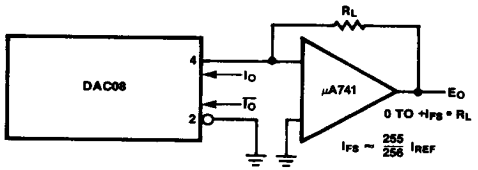
Figure 7 Basic Bipolar Output Operation



	B1	B2	B3	B4	B5	B6	B7	B8	E_O	$\bar{E}_O$
Pos Full Scale	1	1	1	1	1	1	1	1	– 9.920	+10.000
Pos Full Scale – LSB	1	1	1	1	1	1	1	0	– 9.840	+ 9.920
Zero Scale + LSB	1	0	0	0	0	0	0	1	– 0.080	+ 0.160
Zero Scale	1	0	0	0	0	0	0	0	0.000	+ 0.080
Zero Scale – LSB	0	1	1	1	1	1	1	1	+ 0.080	0.000
Neg Full Scale + LSB	0	0	0	0	0	0	0	1	+ 9.920	– 9.840
Neg Full Scale	0	0	0	0	0	0	0	0	+10.000	– 9.920

Typical Applications (Cont.)

Figure 8 Positive Low Impedance Output Operation



For complementary output (operation as negative logic DAC), connect inverting input of Op-Amp to $\overline{I_O}$ (Lead 2); connect I_O (Lead 4) to ground.

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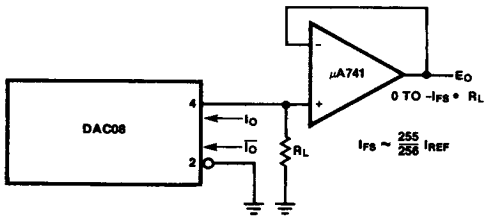
Figure 9 Negative Low Impedance Output Operation



For complementary output (operation as negative logic DAC), connect inverting input of Op-Amp to $\overline{I_O}$ (Lead 2); connect I_O (Lead 4) to ground.

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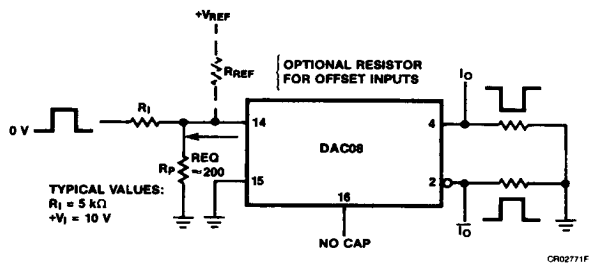
Figure 10 Pulsed Reference Operation



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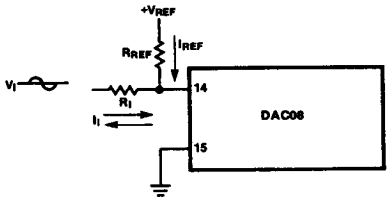
Typical Applications (Cont.)

Figure 11 Accommodating Bipolar References



$I_{REF} \geq$ peak negative swing of I_I

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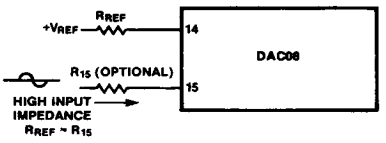

$+V_{REF}$ must be above peak positive swing of V_I

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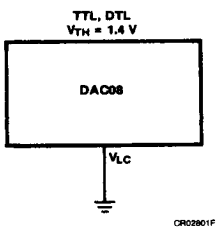
Figure 12 Interfacing With Various Logic Families



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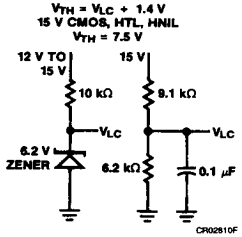

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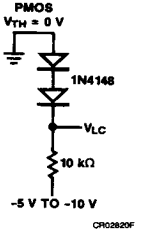

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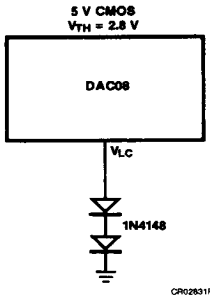

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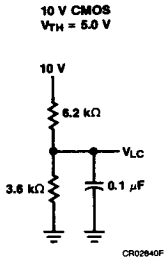

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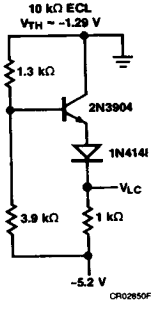

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Note
Do not exceed negative logic input range of DAC

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