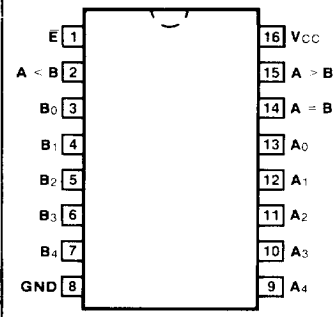
9324 / 93L24

5-BIT COMPARATOR

DESCRIPTION — The '24 expandable comparators provide comparison between two 5-bit words and give three outputs — "less than", "greater than" and "equal to". A HIGH on the active LOW Enable Input forces all three outputs LOW.

- **THREE SEPARATE OUTPUTS — A< B, A > B, A = B**
- **EASILY EXPANDABLE**
- **ACTIVE LOW ENABLE INPUT**

CONNECTION DIAGRAM
PINOUT A



ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE V_{CC} = +5.0 V ±5%, T_A = 0°C to +70°C	MILITARY GRADE V_{CC} = +5.0 V ±10%, T_A = -55°C to +125°C	PKG TYPE
Plastic DIP (P)	A	9324PC, 93L24PC		9B
Ceramic DIP (D)	A	9324DC, 93L24DC	9324DM, 93L24DM	6B
Flatpak (F)	A	9324FC, 93L24FC	9324FM, 93L24FM	4L

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PIN NAMES	DESCRIPTION	93XX (U.L.) HIGH/LOW	93L (U.L.) HIGH/LOW
$\overline{E}$	Enable Input (Active LOW)	2.0/2.0	1.0/0.5
A_0 — A_4	Word A Parallel Inputs	2.0/2.0	1.0/0.5
B_0 — B_4	Word B Parallel Inputs	2.0/2.0	1.0/0.5
A < B	A Less than B Output (Active HIGH)	20/10	10/5.0 (3.0)
A > B	A Greater than B Output (Active HIGH)	20/10	10/5.0 (3.0)
A = B	A Equal to B Output (Active HIGH)	20/10	10/5.0 (3.0)

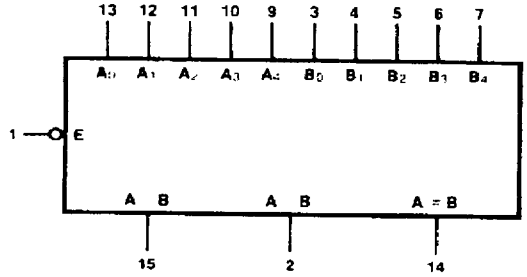
24

FUNCTIONAL DESCRIPTION — The '24 5-bit comparators use combinational circuitry to directly generate "A greater than B" and "A less than B" outputs. As evident from the logic diagram, these outputs are generated in only three gate delays. The "A equals B" output is generated in one additional gate delay by decoding the "A neither less than nor greater than B" condition with a NOR gate. All three outputs are activated by the active LOW Enable Input ($\overline{E}$).

Tying the A > B output from one device into an A input on another device and the A < B output into the corresponding B input permits easy expansion.

The A_4 and B_4 inputs are the most significant inputs and A_0, B_0 the least significant. Thus if A_4 is HIGH and B_4 is LOW, the A > B output will be HIGH regardless of all other inputs except $\overline{E}$.

LOGIC SYMBOL



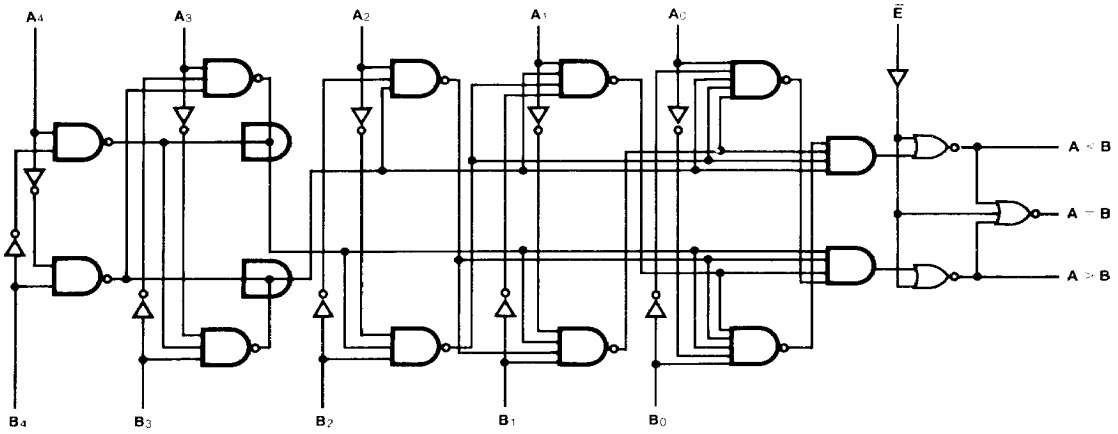
V_{CC} = Pin 16
GND = Pin 8

TRUTH TABLE

INPUTS			OUTPUTS		
$\overline{E}$	A_n	B_n	A < B	A > B	A = B
H	X	X	L	L	L
L	Word A = Word B		L	L	H
L	Word A > Word B		L	H	L
L	Word B > Word A		H	L	L

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

LOGIC DIAGRAM



DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER	93XX		93L		UNITS	CONDITIONS
		Min	Max	Min	Max		
I_{CC}	Power Supply Current		81		21	mA	V_{CC} = Max

AC CHARACTERISTICS: V_{CC} = +5.0 V, T_A = +25° C (See Section 3 for waveforms and load configurations)

SYMBOL	PARAMETER	93XX		93L		UNITS	CONDITIONS
		C_L = 15 pF		C_L = 15 pF			
		Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay $\bar{E}$ to A = B		14 14		32 35	ns	Figs. 3-1, 3-4
t_{PLH} t_{PHL}	Propagation Delay A_2 to A > B		25 22		54 75	ns	Figs. 3-1, 3-5
t_{PLH} t_{PHL}	Propagation Delay A_2 to A < B		26 21		70 77	ns	Figs. 3-1, 3-4
t_{PLH} t_{PHL}	Propagation Delay A_2 to A = B		30 32		100 102	ns	Figs. 3-1, 3-20