

## MM74HC589

### 8-Bit Shift Registers with Input Latches and 3-STATE Serial Output

#### General Description

The MM74HC589 high speed shift register utilizes advanced silicon-gate CMOS technology to achieve the high noise immunity and low power consumption of standard CMOS integrated circuits, as well as the ability to drive 15 LS-TTL loads.

The MM74HC589 comes in a 16-pin package and consists of an 8-bit storage latch feeding a parallel-in, serial-out 8-bit shift register. Data can also be entered serially the shift register through the SER pin. Both the storage register and shift register have positive-edge triggered clocks, RCK and SCK, respectively. SLOAD pin controls parallel LOAD or serial shift operations for the shift register. The shift register has a 3-STATE output to enable the wire-ORing of multiple devices on a serial bus.

The 74HC logic family is speed, function, and pin-out compatible with the standard 74LS logic family. All inputs are protected from damage due to static discharge by internal diode clamps to  $V_{CC}$  and ground.

#### Features

- 8-bit parallel storage register inputs
- Wide operating voltage range: 2V–6V
- Shift register has direct overriding load
- Guaranteed shift frequency. . . DC to 30 MHz
- Low quiescent current: 80  $\mu$ A maximum (74HC Series)
- 3-STATE output for 'Wire-OR'

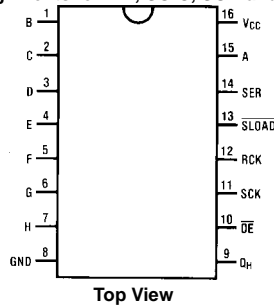
#### Ordering Code:

Order Number	Package Number	Package Description
MM74HC589M	M16A	16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
MM74HC589SJ	M16D	16-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
MM74HC589MTC	MTC16	16-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
MM74HC589N	N16E	16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

#### Connection Diagram

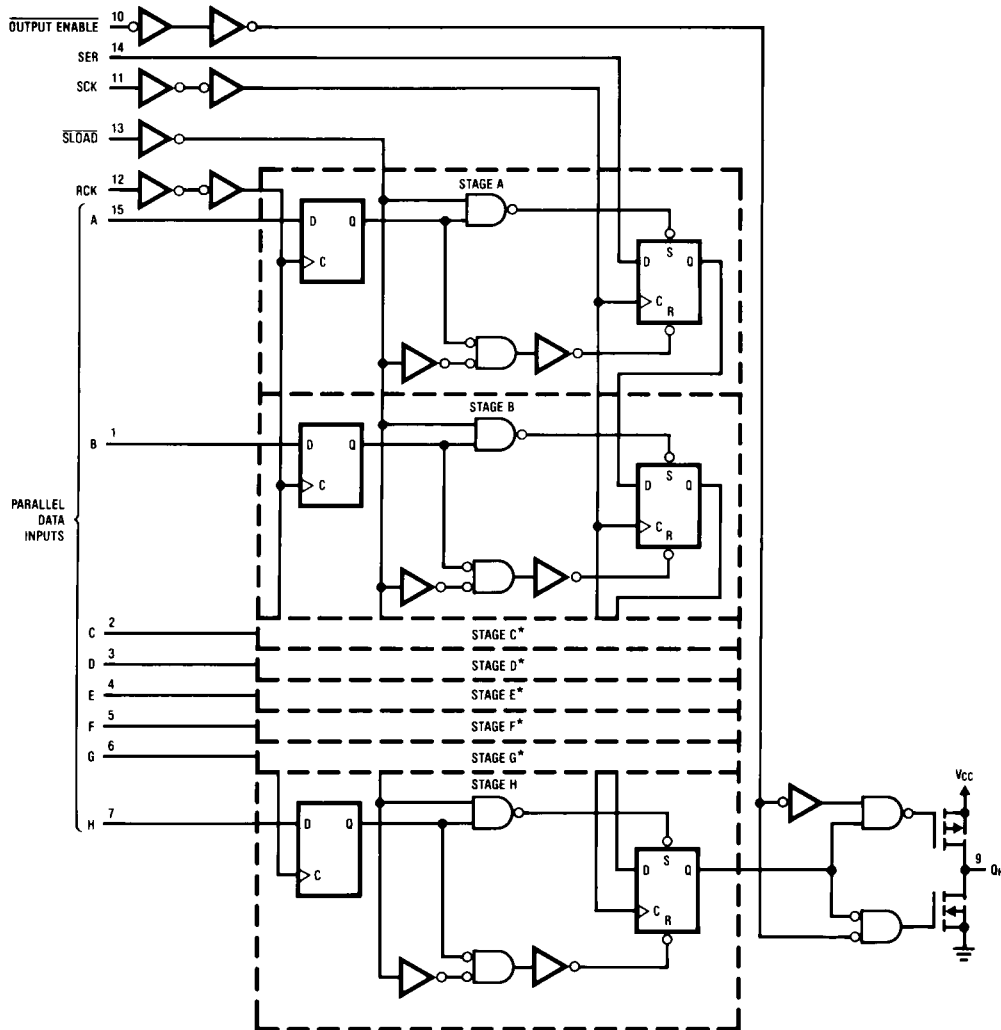
Pin Assignments for DIP, SOIC, SOP and TSSOP



#### Truth Table

RCK	SCK	SLOAD	OE	Function
X	X	X	H	$Q_H$ in Hi-Z State
X	X	X	L	$Q_H$ is enabled
↑	X	X	X	Data loaded into input latches
↑	X	L	X	Data loaded into shift register from pins
H or L	X	L	X	Data loaded from latches to shift register
X	↑	H	X	Shift register is shifted. Data on SER pin is shifted in.
↑	↑	H	X	Data is shifted in shift register, and data is loaded into latches

**Block Diagram** (positive logic)





### AC Electrical Characteristics

$V_{CC} = 5V$ ,  $T_A = 25^\circ C$ ,  $C_L = 15\text{ pF}$ ,  $t_r = t_f = 6\text{ ns}$

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
$f_{MAX}$	Maximum Operating Frequency for SCK		50	30	MHz
$t_{PHL}$ , $t_{PLH}$	Maximum Propagation Delay from SCK to $Q_H$			30	ns
$t_{PHL}$ , $t_{PLH}$	Maximum Propagation Delay from $\overline{SLOAD}$ to $Q_H$			30	ns
$t_{PHL}$ , $t_{PLH}$	Maximum Propagation Delay from LCK to $Q_H$	$\overline{SLOAD} = \text{logic "0"}$	25	45	ns
$t_{PZH}$ , $t_{PZL}$	Output Enable Time	$R_L = 1\text{ k}\Omega$	18	28	ns
$t_{PHZ}$ , $t_{PLZ}$	Output Disable Time	$R_L = 1\text{ k}\Omega$ , $C_L = 5\text{ pF}$	19	25	ns
$t_S$	Minimum Setup Time from RCK to SCK		10	20	ns
$t_S$	Minimum Setup Time from SER to SCK		10	20	ns
$t_S$	Minimum Setup Time from Inputs A thru H to RCK		10	20	ns
$t_H$	Minimum Hold Time		0	5	ns
$t_W$	Minimum Pulse Width SCK, RCK, $\overline{SLOAD}$		8	16	ns

### AC Electrical Characteristics

$V_{CC} = 2.0\text{--}6V$ ,  $C_L = 50\text{ pF}$ ,  $t_r = t_f = 6\text{ ns}$  (unless otherwise specified)

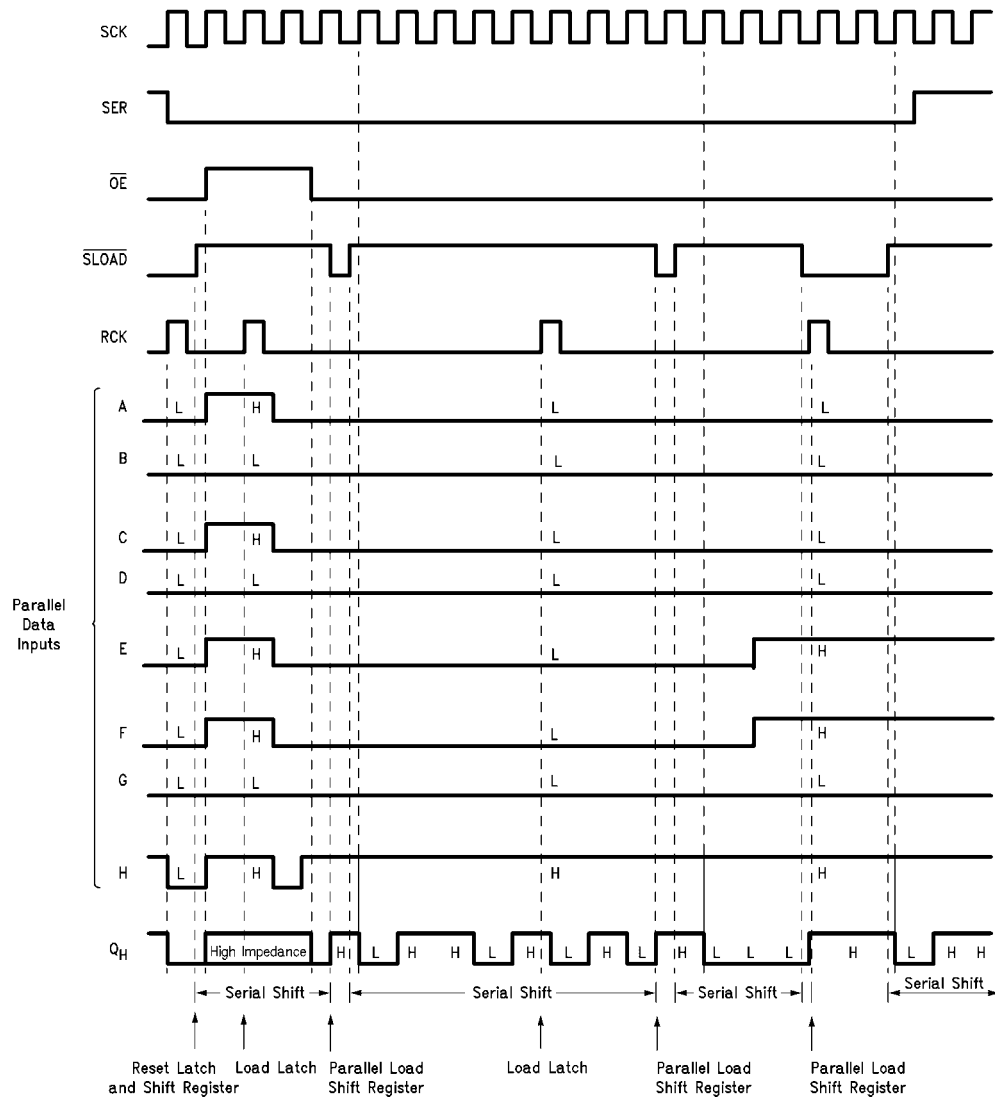
Symbol	Parameter	Conditions	$V_{CC}$	$T_A = 25^\circ C$			$T_A = -40\text{ to }85^\circ C$	$T_A = -55\text{ to }125^\circ C$	Units
				Typ	Guaranteed Limits				
$f_{MAX}$	Maximum Operating Frequency for SCK		2.0V		6	4.8	4	MHz	
			4.5V		30	24	20	MHz	
			6.0V		35	28	24	MHz	
$t_{PHL}$ , $t_{PLH}$	Maximum Propagation Delay from SCK or $\overline{SLOAD}$ to $Q_H$		2.0V	62	175	220	265	ns	
			4.5V	20	35	44	53	ns	
			6.0V	18	30	37	45	ns	
$t_{PHL}$ , $t_{PLH}$	Maximum Propagation Delay from SCK or $\overline{SLOAD}$ to $Q_H$	$C_L = 150\text{ pF}$	2.0V	120	225	280	340	ns	
			4.5V	31	45	56	68	ns	
			6.0V	28	38	48	58	ns	
$t_{PHL}$ , $t_{PLH}$	Maximum Propagation Delay from RCK to $Q_H$		2.0V	80	210	265	315	ns	
			4.5V	25	42	53	63	ns	
			6.0V	21	36	45	54	ns	
$t_{PHL}$ , $t_{PLH}$	Maximum Propagation Delay RCK to $Q_H$	$C_L = 150\text{ pF}$	2.0V	80	210	265	313	ns	
			4.5V	25	52	66	77	ns	
			6.0V	21	44	56	66	ns	
$t_{PZH}$ , $t_{PZL}$	Output Enable Time	$R_L = 1\text{ k}\Omega$	2.0V	70	150	189	224	ns	
			4.5V	22	30	38	45	ns	
			6.0V	20	26	32	38	ns	
$t_{PHZ}$ , $t_{PLZ}$	Output Disable Time	$R_L = 1\text{ k}\Omega$	2.0V	70	150	189	224	ns	
			4.5V	22	30	38	45	ns	
			6.0V	20	26	32	38	ns	
$t_S$	Minimum Setup Time from RCK to SCK		2.0V		100	125	150	ns	
			4.5V		20	25	30	ns	
			6.0V		17	22	25	ns	
$t_S$	Minimum Setup Time from SER to SCK		2.0V		100	125	150	ns	
			4.5V		20	25	30	ns	
			6.0V		17	22	25	ns	
$t_S$	Minimum Setup Time from Inputs A thru H to RCK		2.0V		100	125	150	ns	
			4.5V		20	25	30	ns	
			6.0V		17	22	25	ns	
$t_H$	Minimum Hold Time		2.0V	-5	5	5	5	ns	
			4.5V	0	5	5	5	ns	
			6.0V	1	5	5	5	ns	
$t_W$	Minimum Pulse Width SCK, RCK, $\overline{SLOAD}$ , $\overline{SLOAD}$		2.0V	30	80	100	120	ns	
			4.5V	9	16	20	24	ns	
			6.0V	8	14	17	20	ns	

## AC Electrical Characteristics (Continued)

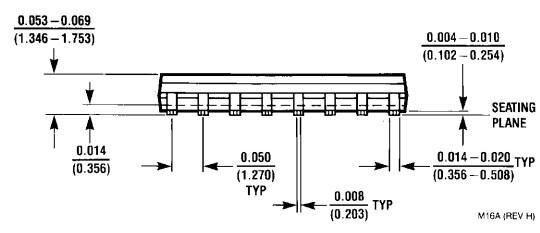
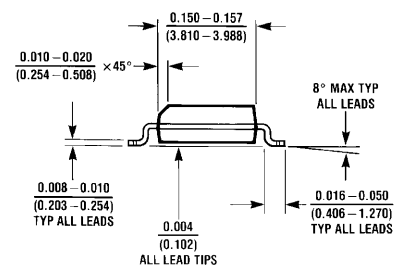
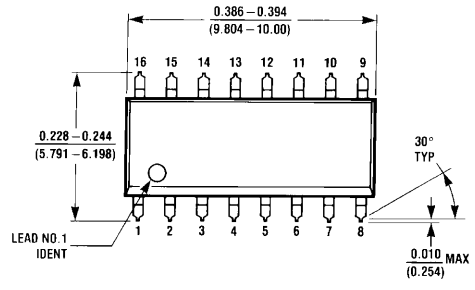
Symbol	Parameter	Conditions	V <sub>CC</sub>	T <sub>A</sub> = 25°C		T <sub>A</sub> = -40 to 85°C	T <sub>A</sub> = -55 to 125°C	Units
				Typ	Guaranteed Limits			
t <sub>r</sub> , t <sub>f</sub>	Maximum Input Rise and Fall Time, Clock		2.0V		1500	1500	1500	ns
			4.5V		500	500	500	ns
			6.0V		400	400	400	ns
t <sub>THL</sub> , t <sub>TLH</sub>	Maximum Output Rise and Fall Time		2.0V	25	60	75	90	ns
			4.5V	6	12	15	18	ns
			6.0V	5	10	12	15	ns
C <sub>PD</sub>	Power Dissipation Capacitance (Note 5)			87				pF
C <sub>IN</sub>	Maximum Input Capacitance			5	10	10	10	pF
C <sub>OUT</sub>	Maximum Output Capacitance			15	20	20	20	pF

**Note 5:** C<sub>PD</sub> determines the no load dynamic power consumption,  $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$ , and the no load dynamic current consumption,  $I_S = C_{PD} V_{CC} sf + I_{CC}$ .

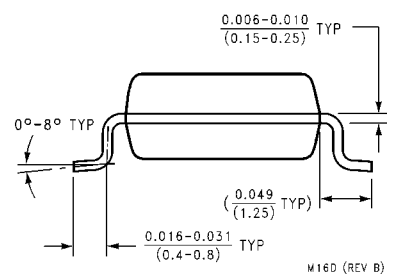
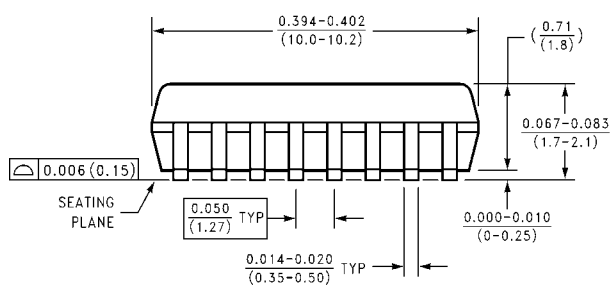
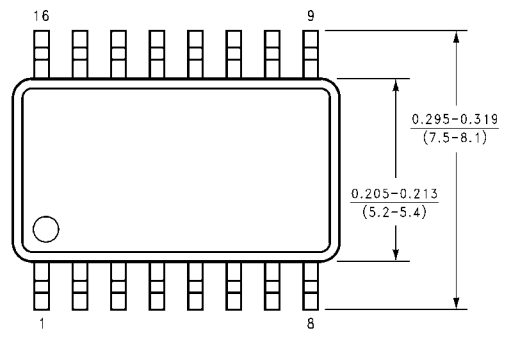
### Timing Diagram



**Physical Dimensions** inches (millimeters) unless otherwise noted

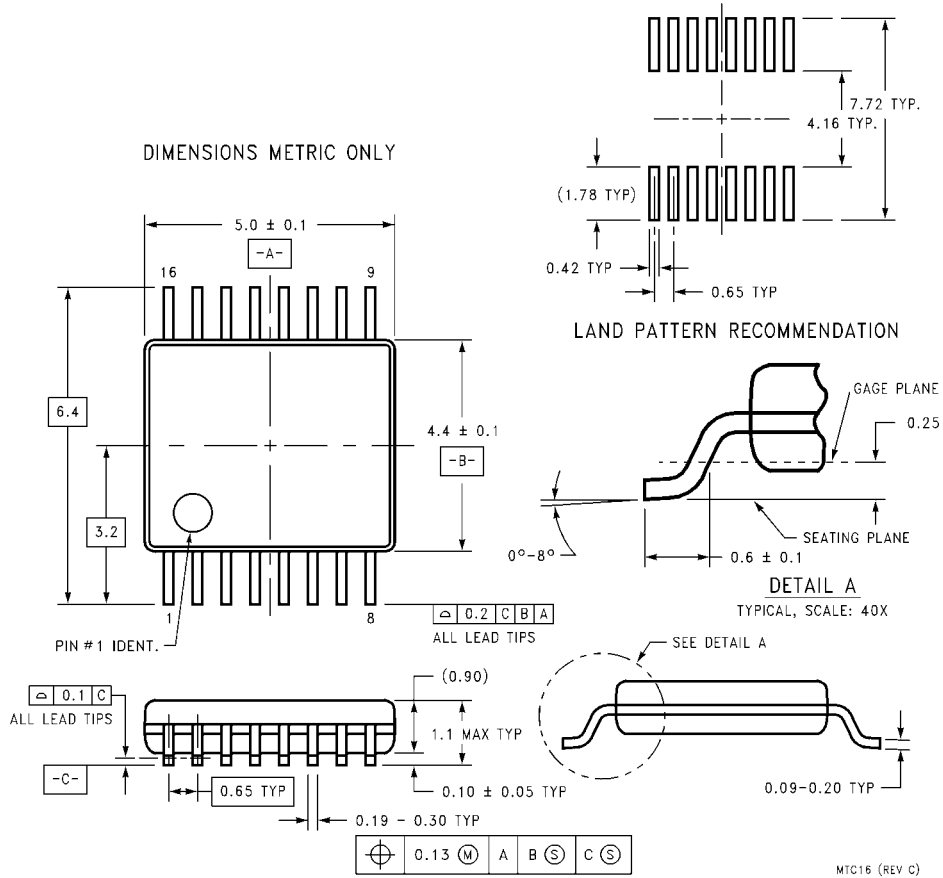


**16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow Package Number M16A**



**16-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide Package Number M16D**

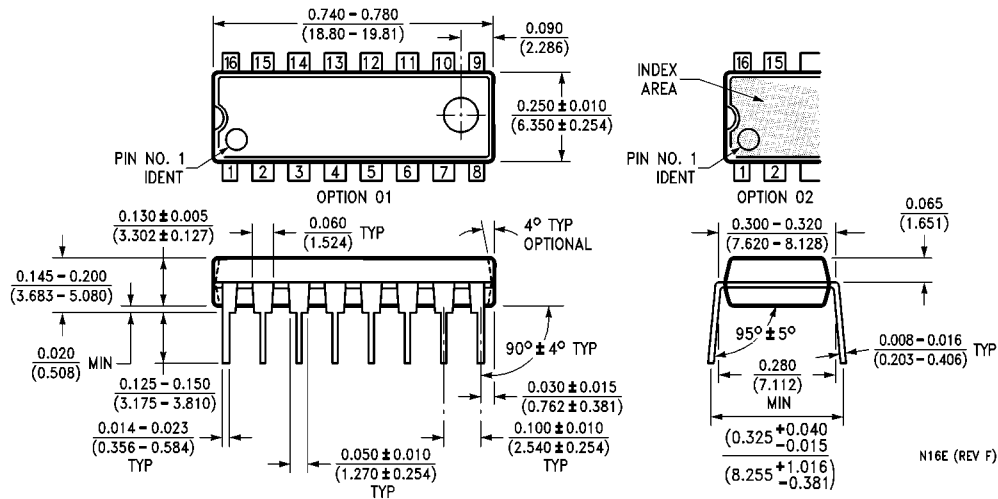
**Physical Dimensions** inches (millimeters) unless otherwise noted (Continued)



**16-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide  
Package Number MTC16**



**Physical Dimensions** inches (millimeters) unless otherwise noted (Continued)



**16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide Package Number N16E**

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