

## 74ABT162244

### 16-Bit Buffer/Line Driver with 25Ω Series Resistors in the Outputs

#### General Description

The ABT162244 contains sixteen non-inverting buffers with 3-STATE outputs designed to be employed as a memory and address driver, clock driver, or bus oriented transmitter/receiver. The device is nibble controlled. Individual 3-STATE control inputs can be shorted together for 8-bit or 16-bit operation.

The 25Ω series resistors in the outputs reduce ringing and eliminate the need for external resistors.

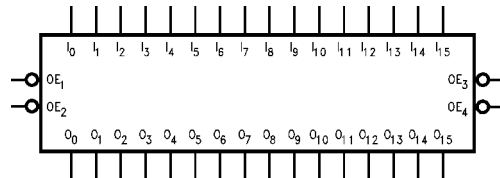
#### Features

- Separate control logic for each nibble
- 16-bit version of the ABT2244
- Guaranteed latchup protection
- High impedance glitch free bus loading during entire power up and power down cycle
- Non-destructive hot insertion capability

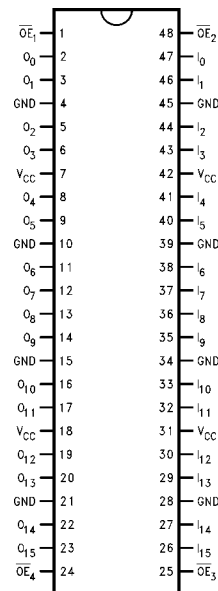
#### Ordering Code:

Order Number	Package Number	Package Description
74ABT162244C55C	MS48A	48-Lead Small Shrink Outline Package (SSOP), JEDEC MO-118, 0.300" Wide [RAIL]
74ABT162244C55X	MS48A	48-Lead Small Shrink Outline Package (SSOP), JEDEC MO-118, 0.300" Wide [TAPE and REEL]
74ABT162244CMTD	MTD48	48-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide [RAIL]
74ABT162244CMTDX	MTD48	48-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide [TAPE and REEL]

#### Logic Symbol



#### Connection Diagram



#### Pin Descriptions

Pin Names	Description
$\overline{OE}_n$	Output Enable Input (Active LOW)
$I_0$ - $I_{15}$	Inputs
$O_0$ - $O_{15}$	Outputs

**Truth Tables**

Inputs		Outputs
$\overline{OE}_1$	I <sub>0-13</sub>	O <sub>0-3</sub>
L	L	L
L	H	H
H	X	Z

Inputs		Outputs
$\overline{OE}_3$	I <sub>8-11</sub>	O <sub>8-11</sub>
L	L	L
L	H	H
H	X	Z

Inputs		Outputs
$\overline{OE}_2$	I <sub>4-7</sub>	O <sub>4-7</sub>
L	L	L
L	H	H
H	X	Z

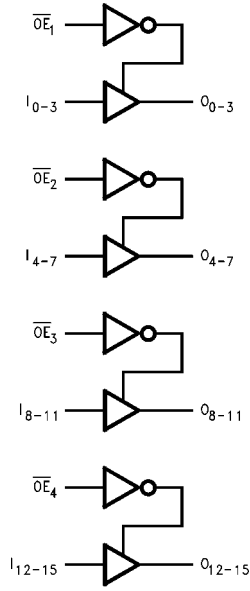
Inputs		Outputs
$\overline{OE}_4$	I <sub>12-15</sub>	O <sub>12-15</sub>
L	L	L
L	H	H
H	X	Z

H = HIGH Voltage Level  
 L = LOW Voltage Level  
 X = Immaterial  
 Z = High Impedance

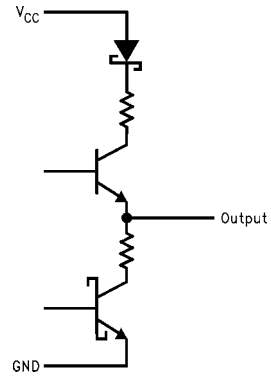
**Functional Description**

The ABT162244 contains sixteen non-inverting buffers with 3-STATE outputs. The device is nibble (4 bits) controlled with each nibble functioning identically, but independent of the other. The control pins can be shorted together to obtain full 16-bit operation.

**Logic Diagram**



**Schematic of each Output**



**Absolute Maximum Ratings**(Note 1)

Storage Temperature	-65°C to +150°C
Ambient Temperature under Bias	-55°C to +125°C
Junction Temperature under Bias	-55°C to +150°C
V <sub>CC</sub> Pin Potential to Ground Pin	-0.5V to +7.0V
Input Voltage (Note 2)	-0.5V to +7.0V
Input Current (Note 2)	-30 mA to +5.0 mA
Voltage Applied to Any Output in the Disabled or Power-Off State	-0.5V to 5.5V
in the HIGH State	-0.5V to V <sub>CC</sub>
Current Applied to Output in LOW State (Max)	twice the rated I <sub>OL</sub> (mA)
DC Latchup Source Current	-500 mA
Over Voltage Latchup (I/O)	10V

**Recommended Operating Conditions**

Free Air Ambient Temperature	-40°C to +85°C
Supply Voltage	+4.5V to +5.5V
Minimum Input Edge Rate ( $\Delta V/\Delta t$ )	
Data Input	50 mV/ns
Enable Input	20 mV/ns

**Note 1:** Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

**Note 2:** Either voltage limit or current limit is sufficient to protect inputs.

**DC Electrical Characteristics**

Symbol	Parameter	Min	Typ	Max	Units	V <sub>CC</sub>	Conditions
V <sub>IH</sub>	Input HIGH Voltage	2.0			V		Recognized HIGH Signal
V <sub>IL</sub>	Input LOW Voltage			0.8	V		Recognized LOW Signal
V <sub>CD</sub>	Input Clamp Diode Voltage			-1.2	V	Min	I <sub>IN</sub> = -18 mA
V <sub>OH</sub>	Output HIGH Voltage	2.5			V	Min	I <sub>OH</sub> = -3 mA
		2.0			V	Min	I <sub>OH</sub> = -32 mA
V <sub>OL</sub>	Output LOW Voltage			0.8	V	Min	I <sub>OL</sub> = 12 mA
I <sub>IH</sub>	Input HIGH Current			1	μA	Max	V <sub>IN</sub> = 2.7V (Note 3)
				1	μA	Max	V <sub>IN</sub> = V <sub>CC</sub>
I <sub>BVI</sub>	Input HIGH Current Breakdown Test			7	μA	Max	V <sub>IN</sub> = 7.0V
I <sub>IL</sub>	Input LOW Current			-1	μA	Max	V <sub>IN</sub> = 0.5V (Note 3)
				-1	μA	Max	V <sub>IN</sub> = 0.0V
V <sub>ID</sub>	Input Leakage Test	4.75			V	0.0	I <sub>ID</sub> = 1.9 μA All Other Pins Grounded
I <sub>OZH</sub>	Output Leakage Current			10	μA	0 - 5.5V	V <sub>OUT</sub> = 2.7V; $\overline{OE}_n = 2.0V$
I <sub>OZL</sub>	Output Leakage Current			-10	μA	0 - 5.5V	V <sub>OUT</sub> = 0.5V; $\overline{OE}_n = 2.0V$
I <sub>OS</sub>	Output Short-Circuit Current	-100		-275	mA	Max	V <sub>OUT</sub> = 0.0V
I <sub>CEx</sub>	Output High Leakage Current			50	μA	Max	V <sub>OUT</sub> = V <sub>CC</sub>
I <sub>ZZ</sub>	Bus Drainage Test			100	μA	0.0	V <sub>OUT</sub> = 5.5V; All Others GND
I <sub>CCH</sub>	Power Supply Current			2.0	mA	Max	All Outputs HIGH
I <sub>CCL</sub>	Power Supply Current			60	mA	Max	All Outputs LOW
I <sub>CCZ</sub>	Power Supply Current			2.0	mA	Max	$\overline{OE}_n = V_{CC}$ All Others at V <sub>CC</sub> or GND
I <sub>CCT</sub>	Additional I <sub>CC</sub> /Input	Outputs Enabled		3.0	mA	Max	V <sub>I</sub> = V <sub>CC</sub> - 2.1V Enable Input V <sub>I</sub> = V <sub>CC</sub> - 2.1V Data Input V <sub>I</sub> = V <sub>CC</sub> - 2.1V All Others at V <sub>CC</sub> or GND
		Outputs 3-STATE		3.0	mA		
		Outputs 3-STATE		50	μA		
I <sub>CCD</sub>	Dynamic I <sub>CC</sub> (Note 3)	No Load		0.1	mA/ MHz	Max	Outputs OPEN $\overline{OE}_n = GND$ One Bit Toggling, 50% Duty Cycle

**Note 3:** Guaranteed, but not tested.

## AC Electrical Characteristics

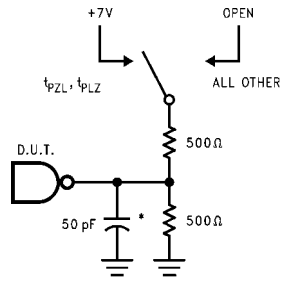
Symbol	Parameter	$T_A = +25^\circ\text{C}$ $V_{CC} = +5\text{V}$ $C_L = 50\text{ pF}$			$T_A = -40^\circ\text{C to } +85^\circ\text{C}$ $V_{CC} = 4.5\text{V} - 5.5\text{V}$ $C_L = 50\text{ pF}$		Units
		Min	Typ	Max	Min	Max	
$t_{PLH}$	Propagation	1.0	2.4	3.9	1.0	3.9	ns
$t_{PHL}$	Delay Data to Outputs	1.0	3.2	4.7	1.0	4.7	
$t_{PZH}$	Output	1.5	3.5	6.3	1.5	6.3	ns
$t_{PZL}$	Enable Time	1.5	4.2	6.9	1.5	6.9	
$t_{PHZ}$	Output	1.0	4.2	6.7	1.0	6.7	ns
$t_{PLZ}$	Disable Time	1.0	3.8	6.7	1.0	6.7	

## Capacitance

Symbol	Parameter	Typ	Units	Conditions $T_A = 25^\circ\text{C}$
$C_{IN}$	Input Capacitance	5.0	pF	$V_{CC} = 0.0\text{V}$
$C_{OUT}$ (Note 4)	Output Capacitance	9.0	pF	$V_{CC} = 5.0\text{V}$

**Note 4:**  $C_{OUT}$  is measured at frequency  $f = 1\text{ MHz}$  per MIL-STD-883, Method 3012.

### AC Loading



\*Includes jig and probe capacitance

FIGURE 1. Standard AC Test Load

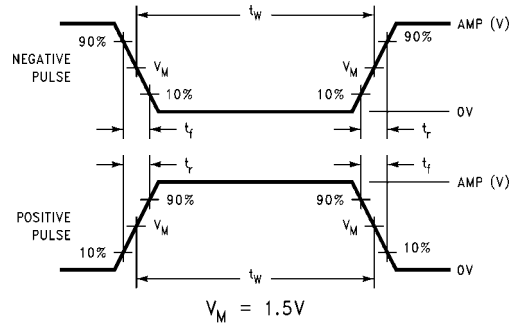


FIGURE 2. Input Pulse Requirements

Amplitude	Rep. Rate	$t_w$	$t_r$	$t_f$
3.0V	1 MHz	500 ns	2.5 ns	2.5 ns

FIGURE 3. Test Input Signal Requirements

### AC Waveforms

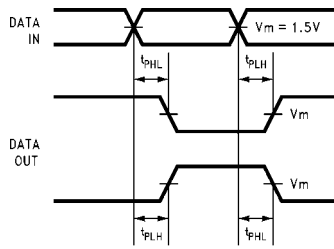


FIGURE 4. Propagation Delay Waveforms for Inverting and Non-Inverting Functions

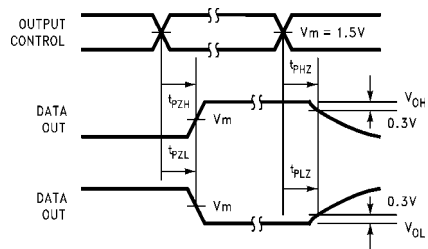


FIGURE 6. 3-STATE Output HIGH and LOW Enable and Disable Times

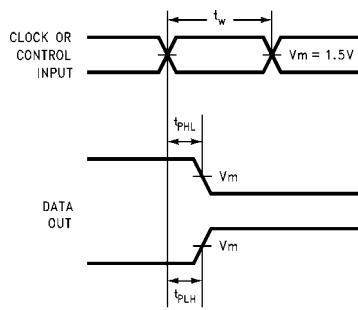


FIGURE 5. Propagation Delay, Pulse Width Waveforms

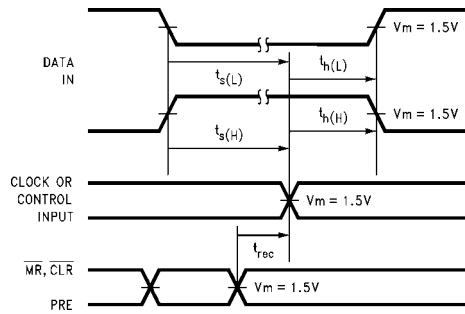
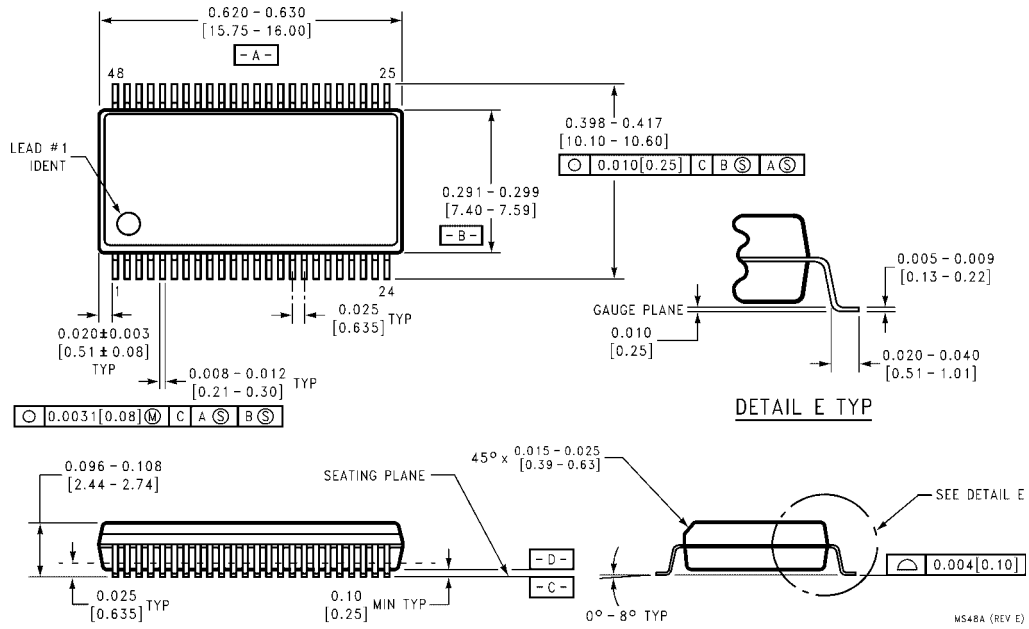


FIGURE 7. Setup Time, Hold Time and Recovery Time Waveforms

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**Physical Dimensions** inches (millimeters) unless otherwise noted



**48-Lead Small Shrink Outline Package (SSOP), JEDEC MO-118, 0.300" Wide  
Package Number MS48A**

**Physical Dimensions** inches (millimeters) unless otherwise noted (Continued)



MTD48REVC

**48-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide Package Number MTD48**

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