

## 256Mb (2Mx4Bankx32) Synchronous DRAM

### Features

- Fully Synchronous to Positive Clock Edge
- Single 3.3V ±0.3V Power Supply
- LVTTTL Compatible with Multiplexed Address
- Programmable Burst Length (B/L) - 1, 2, 4, 8 or Full Page
- Programmable CAS Latency (C/L) - 2 or 3
- Data Mask (DQM) for Read / Write Masking
- Programmable Wrap Sequence
  - Sequential (B/L = 1/2/4/8/full Page)
  - Interleave (B/L = 1/2/4/8)
- Burst Read with Single-bit Write Operation
- All Inputs are Sampled at the Rising Edge of the System Clock
- Auto Refresh and Self Refresh
- 4,096 Refresh Cycles / 64ms (15.625us)

### Description

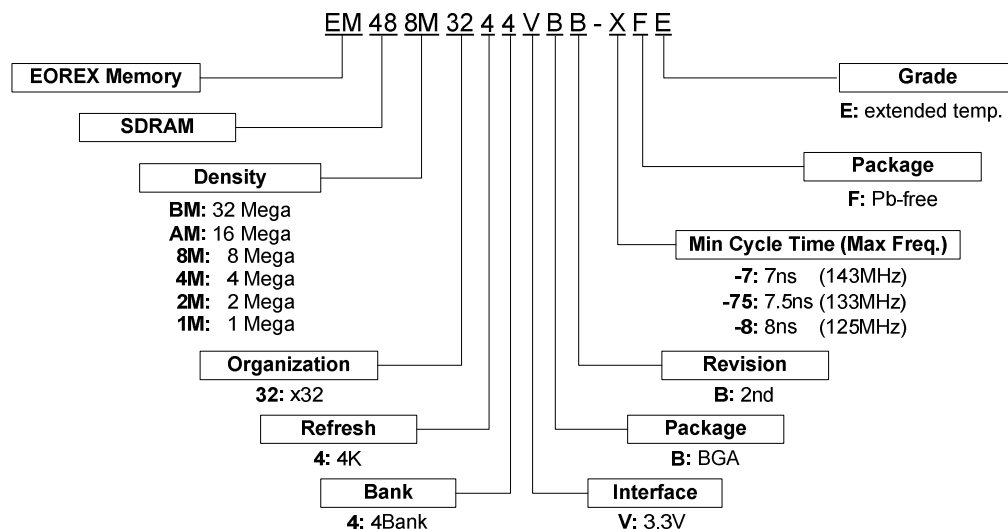
The EM488M3244VBB is Synchronous Dynamic Random Access Memory (SDRAM) organized as 2Meg words x 4 banks by 32 bits. All inputs and outputs are synchronized with the positive edge of the clock.

The 256Mb SDRAM uses synchronized pipelined architecture to achieve high speed data transfer rates and is designed to operate at 3.3V low power memory system. It also provides auto refresh with power saving / down mode. All inputs and outputs voltage levels are compatible with LVTTTL.

Available packages: TFBGA-90B(13mmx8mm).

### Ordering Information

Part No	Organization	Max. Freq	Package	Grade	Pb
EM488M3244VBB-75F	8M X 32	133MHz @CL3	TFBGA-90B	Commercial	Free
EM488M3244VBB-7F	8M X 32	143MHz @CL3	TFBGA-90B	Commercial	Free
EM488M3244VBB-75FE	8M X 32	133MHz @CL3	TFBGA-90B	Extend temp.	Free
EM488M3244VBB-7FE	8M X 32	143MHz @CL3	TFBGA-90B	Extend temp.	Free



\* EOREX reserves the right to change products or specification without notice.

***Pin Assignment***

1	2	3		7	8	9
DQ26	DQ24	VSS	A	VDD	DQ23	DQ21
DQ28	VDDQ	VSSQ	B	VDDQ	VSSQ	DQ19
VSSQ	DQ27	DQ25	C	DQ22	DQ20	VDDQ
VSSQ	DQ29	DQ30	D	DQ17	DQ18	VDDQ
VDDQ	DQ31	NC	E	NC	DQ16	VSSQ
VSS	DQM3	A3	F	A2	DQM2	VDD
A4	A5	A6	G	A10	A0	A1
A7	A8	NC	H	NC	BA1	A11
CLK	CKE	A9	J	BA0	/CS	/RAS
DQM1	NC	NC	K	/CAS	/WE	DQM0
VDDQ	DQ8	VSS	L	VDD	DQ7	VSSQ
VSSQ	DQ10	DQ9	M	DQ6	DQ5	VDDQ
VSSQ	DQ12	DQ14	N	DQ1	DQ3	VDDQ
DQ11	VDDQ	VSSQ	P	VDDQ	VSSQ	DQ4
DQ13	DQ15	VSS	R	VDD	DQ0	DQ2

90ball TFBGA / (13mm x 8mm)

**Pin Description (Simplified)**

Pin	Name	Function
J1	CLK	<b>(System Clock)</b> Master clock input (Active on the positive rising edge)
J8	/CS	<b>(Chip Select)</b> Selects chip when active
J2	CKE	<b>(Clock Enable)</b> Activates the CLK when "H" and deactivates when "L". CKE should be enabled at least one cycle prior to new command. Disable input buffers for power down in standby.
G8,G9,F7,F3,G1, G2,G3,H1,H2,J3, G7,H9	A0~A11	<b>(Address)</b> Row address (A0 to A11) is determined by A0 to A11 level at the bank active command cycle CLK rising edge. CA (CA0 to CA8) is determined by A0 to A8 level at the read or write command cycle CLK rising edge. And this column address becomes burst access start address. A10 defines the pre-charge mode. When A10= High at the pre-charge command cycle, all banks are pre-charged. But when A10= Low at the pre-charge command cycle, only the bank that is selected by BA is pre-charged.
J7,H8	BA0,BA1	<b>(Bank Address)</b> Selects which bank is to be active.
J9	/RAS	<b>(Row Address Strobe)</b> Latches Row Addresses on the positive rising edge of the CLK with /RAS "L". Enables row access & pre-charge.
K7	/CAS	<b>(Column Address Strobe)</b> Latches Column Addresses on the positive rising edge of the CLK with /CAS low. Enables column access.
K8	/WE	<b>(Write Enable)</b> Latches Column Addresses on the positive rising edge of the CLK with /CAS low. Enables column access.
K9,K1,F8,F2	DQM0~DQM3	<b>(Data Input/Output Mask)</b> DQM controls I/O buffers.
R8,N7,R9,N8,P9, M8,M7,L8,L2,M3, M2,P1,N2,R1,N3, R2,E8,D7,D8,B9, C8,A9,C7,A8,A2, C3,A1,C2,B1,D2, D3,E2	DQ0~DQ31	<b>(Data Input/Output)</b> DQ pins have the same function as I/O pins on a conventional DRAM.
A7,F9,L7,R7	V <sub>DD</sub>	<b>(Power Supply)</b> power supply pins for internal circuits.
A3,F1,L3,R3	V <sub>SS</sub>	<b>(Ground)</b> ground pins for internal circuits.
B2,B7,C9,D9,E1, L1,M9,N9,P2,P7	V <sub>DDQ</sub>	<b>(Power Supply)</b> power supply pins for the output buffers.
B8,B3,C1,D1,E9, L9,M1,N1,P3,P8	V <sub>SSQ</sub>	<b>(Ground)</b> ground pins for the output buffers.

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E3,E7,H3,H7,K2, K3	NC	<b>(No Connection)</b> This pin is recommended to be left No Connection on the device.
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**Absolute Maximum Rating**

Symbol	Item	Rating		Units
V <sub>IN</sub> , V <sub>OUT</sub>	Input, Output Voltage	-0.3 ~ +4.6		V
V <sub>DD</sub> , V <sub>DDQ</sub>	Power Supply Voltage	-0.3 ~ +4.6		V
T <sub>OP</sub>	Operating Temperature Range	Commercial	0 ~ +70	°C
		Extended	-25 ~ +85	
T <sub>STG</sub>	Storage Temperature Range	-55 ~ +150		°C
P <sub>D</sub>	Power Dissipation	1		W
I <sub>OS</sub>	Short Circuit Current	50		mA

**Note:** Caution Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

**Capacitance (V<sub>CC</sub>=3.3V, f=1MHz, T<sub>A</sub>=25°C)**

Symbol	Parameter	Min.	Typ.	Max.	Units
C <sub>CLK</sub>	Clock Capacitance	2.5		4.0	pF
C <sub>I</sub>	Input Capacitance for CLK, CKE, Address, /CS, /RAS, /CAS, /WE, DQML, DQMU	2.5		3.0	pF
C <sub>O</sub>	Input/Output Capacitance	4.0		6.5	pF

**Recommended DC Operating Conditions (T<sub>A</sub>=0°C ~70°C)**

Symbol	Parameter	Min.	Typ.	Max.	Units
V <sub>DD</sub>	Power Supply Voltage	3.0	3.3	3.6	V
V <sub>DDQ</sub>	Power Supply Voltage (for I/O Buffer)	3.0	3.3	3.6	V
V <sub>IH</sub>	Input Logic High Voltage	2.0		V <sub>DD</sub> +0.3	V
V <sub>IL</sub>	Input Logic Low Voltage	-0.3		0.8	V

**Note:** \* All voltages referred to V<sub>SS</sub>.  
 \* V<sub>IH</sub> (max.) = 5.6V for pulse width 3ns  
 \* V<sub>IL</sub> (min.) = -2.0V for pulse width 3ns

**Recommended DC Operating Conditions**

( $V_{DD}=3.3V\pm 0.3V$ ,  $T_A=0^{\circ}C \sim 70^{\circ}C$ ,  $-25^{\circ}C \sim +85^{\circ}C$ )

Symbol	Parameter	Test Conditions	Max.	Units
$I_{CC1}$	Operating Current <i>(Note 1)</i>	Burst length=1, $t_{RC} \geq t_{RC}(\text{min.})$ , $I_{OL}=0\text{mA}$ , One bank active	125	mA
$I_{CC2P}$	Precharge Standby Current in Power Down Mode	$CKE \leq V_{IL}(\text{max.})$ , $t_{CK}=15\text{ns}$	3	mA
$I_{CC2PS}$		$CKE \leq V_{IL}(\text{max.})$ , $t_{CK} = \infty$	3	mA
$I_{CC2N}$	Precharge Standby Current in Non-power Down Mode	$CKE \geq V_{IL}(\text{min.})$ , $t_{CK}=15\text{ns}$ , $/CS \geq V_{IH}(\text{min.})$ Input signals are changed one time during 30ns	30	mA
$I_{CC2NS}$		$CKE \geq V_{IL}(\text{min.})$ , $t_{CK} = \infty$ , Input signals are stable	20	mA
$I_{CC3P}$	Active Standby Current in Power Down Mode	$CKE \leq V_{IL}(\text{max.})$ , $t_{CK}=15\text{ns}$	5	mA
$I_{CC3PS}$		$CKE \leq V_{IL}(\text{max.})$ , $t_{CK} = \infty$	5	mA
$I_{CC3N}$	Active Standby Current in Non-power Down Mode	$CKE \geq V_{IL}(\text{min.})$ , $t_{CK}=15\text{ns}$ , $/CS \geq V_{IH}(\text{min.})$ Input signals are changed one time during 30ns	45	mA
$I_{CC3NS}$		$CKE \geq V_{IL}(\text{min.})$ , $t_{CK} = \infty$ , Input signals are stable	35	mA
$I_{CC4}$	Operating Current (Burst Mode) <i>(Note 2)</i>	$t_{CCD} \geq 2\text{CLKs}$ , $I_{OL}=0\text{mA}$	150	mA
$I_{CC5}$	Refresh Current <i>(Note 3)</i>	$t_{RC} \geq t_{RC}(\text{min.})$	270	mA
$I_{CC6}$	Self Refresh Current	$CKE \leq 0.2V$	3 <i>(Note 4)</i>	mA

\*All voltages referenced to  $V_{SS}$ .

**Note 1:**  $I_{CC1}$  depends on output loading and cycle rates.

Specified values are obtained with the output open.

Input signals are changed only one time during  $t_{CK}$  (min.)

**Note 2:**  $I_{CC4}$  depends on output loading and cycle rates.

Specified values are obtained with the output open.

Input signals are changed only one time during  $t_{CK}$  (min.)

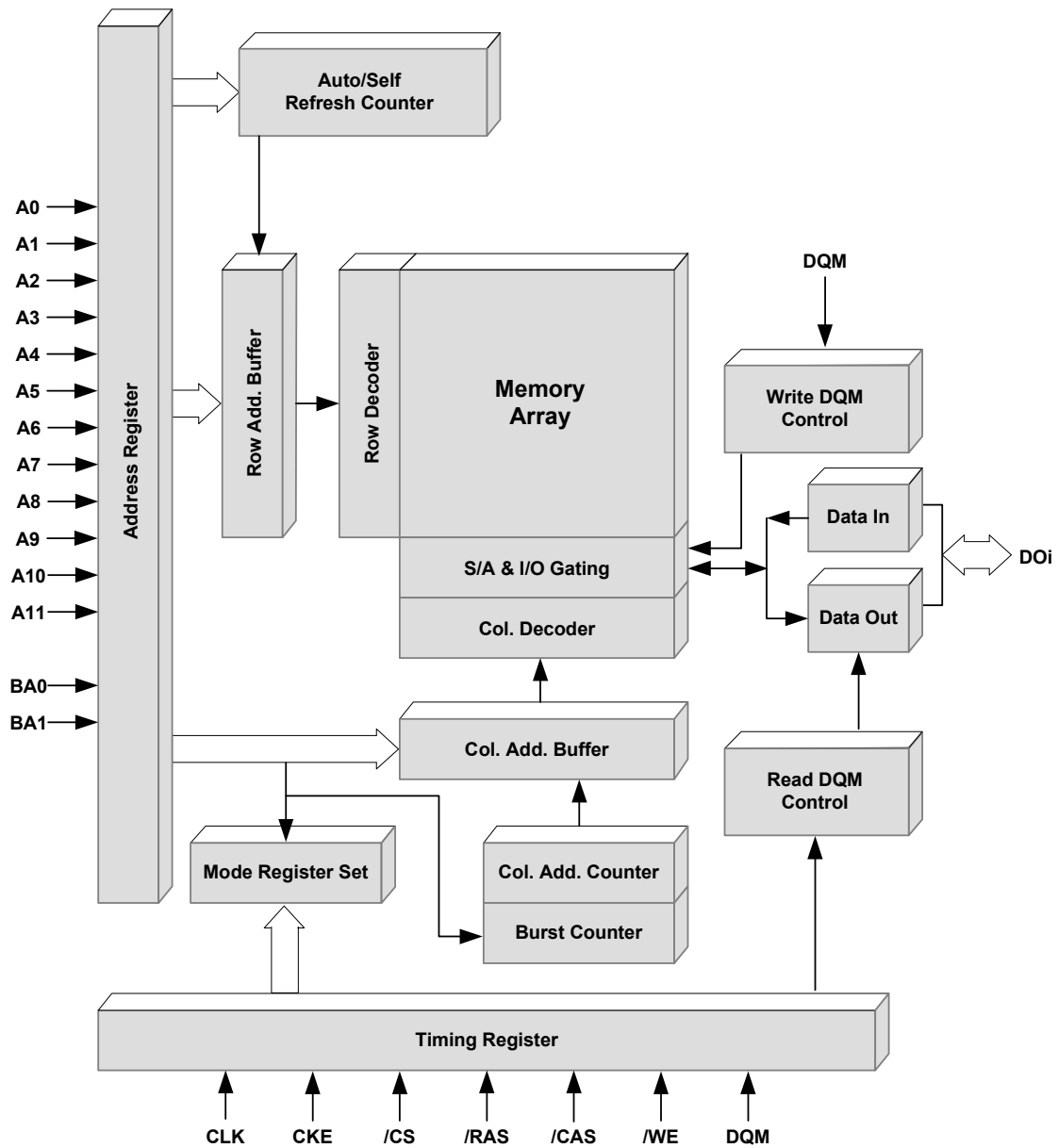
**Note 3:** Input signals are changed only one time during  $t_{CK}$  (min.)

**Note 4:** Standard power version.

**Recommended DC Operating Conditions (Continued)**

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
$I_{IL}$	Input Leakage Current	$0 \leq V_I \leq V_{DDQ}$ , $V_{DDQ}=V_{DD}$ All other pins not under test=0V	-0.5		+0.5	uA
$I_{OL}$	Output Leakage Current	$0 \leq V_O \leq V_{DDQ}$ , $D_{OUT}$ is disabled	-0.5		+0.5	uA
$V_{OH}$	High Level Output Voltage	$I_O = -2\text{mA}$	2.4			V
$V_{OL}$	Low Level Output Voltage	$I_O = +2\text{mA}$			0.4	V

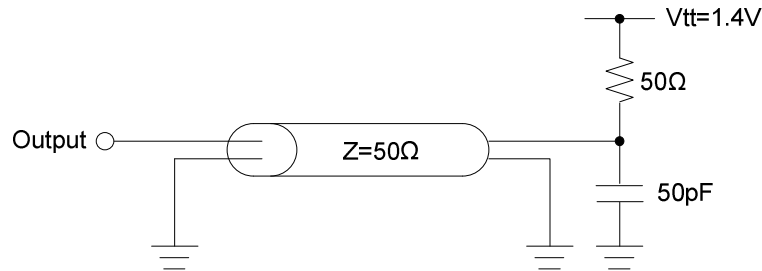
Block Diagram



## AC Operating Test Conditions

( $V_{DD}=3.3V\pm 0.3V$ ,  $T_A=0^{\circ}C \sim 70^{\circ}C$ )

Item	Conditions
Output Reference Level	1.4V/1.4V
Output Load	See diagram as below
Input Signal Level	2.4V/0.4V
Transition Time of Input Signals	2ns
Input Reference Level	1.4V



## AC Operating Test Characteristics

( $V_{DD}=3.3V\pm 0.3V$ ,  $T_A=0^{\circ}C \sim 70^{\circ}C$ ,  $-25^{\circ}C \sim +85^{\circ}C$ )

Symbol	Parameter	-7		-7.5		Units
		Min.	Max.	Min.	Max.	
$t_{CK}$	Clock Cycle Time	CL=3	7		7.5	ns
		CL=2	7.5		10	
$t_{AC}$	Access Time form CLK	CL=3		5.4	5.4	ns
		CL=2		5.4	6	
$t_{CH}$	CLK High Level Width		2.5		2.5	ns
$t_{CL}$	CLK Low Level Width		2.5		2.5	ns
$t_{OH}$	Data-out Hold Time	CL=3	3		3	ns
		CL=2				
$t_{HZ}$	Data-out High Impedance Time <i>(Note 5)</i>	CL=3	3	7	3	ns
		CL=2				
$t_{LZ}$	Data-out Low Impedance Time		0		0	ns
$t_{IH}$	Input Hold Time		0.8		1	ns
$t_{IS}$	Input Setup Time		1.5		1.5	ns

\* All voltages referenced to  $V_{SS}$ .

**Note 5:**  $t_{HZ}$  defines the time at which the output achieve the open circuit condition and is not referenced to output voltage levels.



**AC Operating Test Characteristics (Continued)**

( $V_{DD}=3.3V\pm 0.3V$ ,  $T_A=0^{\circ}C \sim 70^{\circ}C$ ,  $-25^{\circ}C \sim +85^{\circ}C$ )

Symbol	Parameter	-7		-75		Units
		Min.	Max.	Min.	Max.	
$t_{RC}$	ACTIVE to ACTIVE Command Period <i>(Note 6)</i>	62		67		ns
$t_{RAS}$	ACTIVE to PRECHARGE Command Period <i>(Note 6)</i>	42	100k	45	100k	ns
$t_{RP}$	PRECHARGE to ACTIVE Command Period <i>(Note 6)</i>	20		20		ns
$t_{RCD}$	ACTIVE to READ/WRITE Delay Time <i>(Note 6)</i>	20		20		ns
$t_{RRD}$	ACTIVE(one) to ACTIVE(another) Command <i>(Note 6)</i>	14		15		ns
$t_{CCD}$	READ/WRITE Command to READ/WRITE Command	1		1		CLK
$t_{DPL}$	Date-in to PRECHARGE Command	2		2		CLK
$t_{BDL}$	Date-in to BURST Stop Command	1		1		CLK
$t_{ROH}$	Data-out to High Impedance from PRECHARGE Command	CL=3	3		3	CLK
		CL=2	2		2	
$t_{REF}$	Refresh Time (4,096 cycle)		64		64	ms

\* All voltages referenced to  $V_{SS}$ .

**Note 6:** These parameters account for the number of clock cycles and depend on the operating frequency of the clock, as follows:

The number of clock cycles = Specified value of timing/clock period (Count Fractions as a whole number)

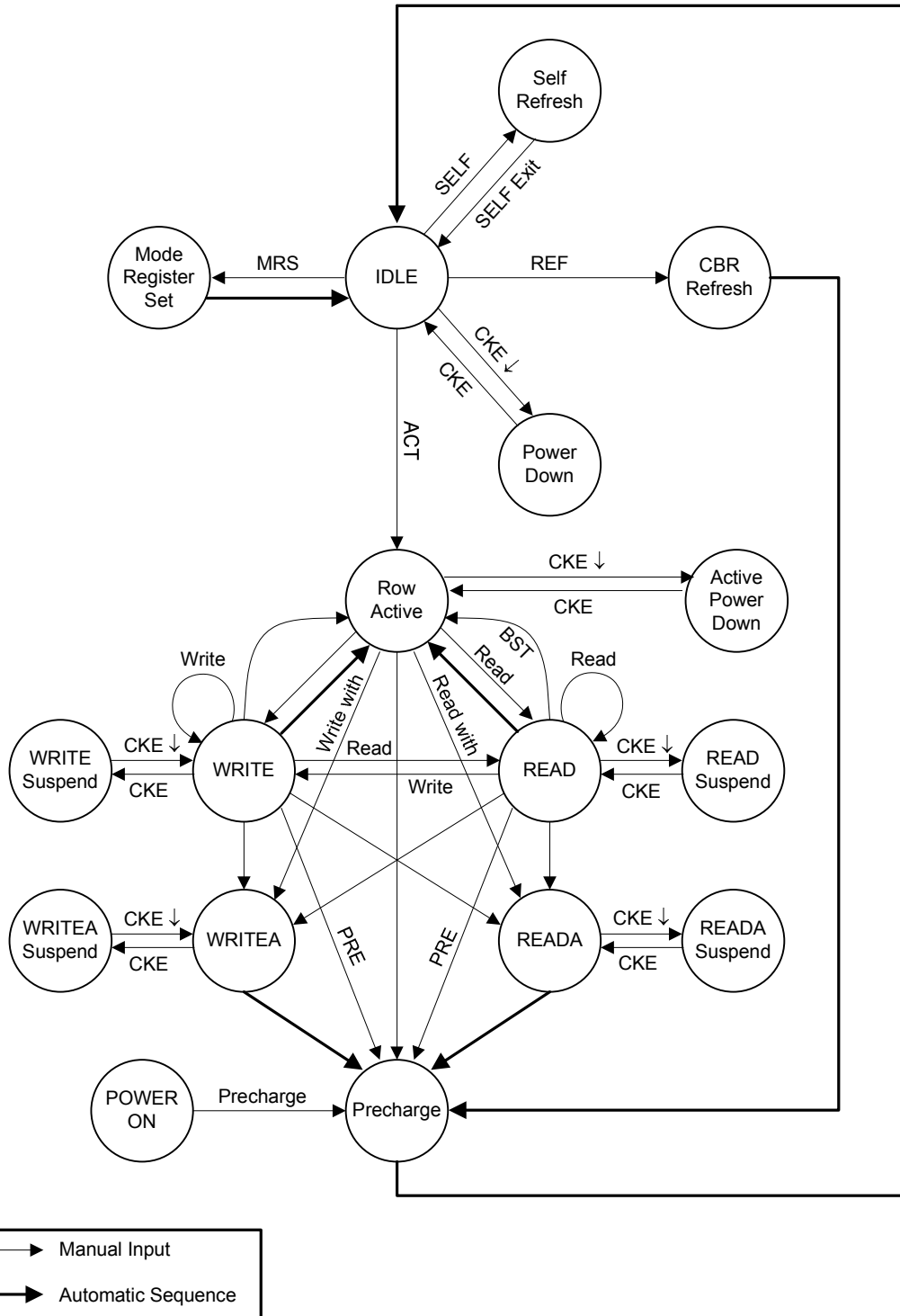
**Recommended Power On and Initialization**

The following power on and initialization sequence guarantees the device is preconditioned to each user's specific needs. (Like a conventional DRAM) During power on, all  $V_{DD}$  and  $V_{DDQ}$  pins must be built up simultaneously to the specified voltage when the input signals are held in the "NOP" state. The power on voltage must not exceed  $V_{DD}+0.3V$  on any of the input pins or  $V_{DD}$  supplies. (CLK signal started at same time)

After power on, an initial pause of 200  $\mu s$  is required followed by a precharge of all banks using the precharge command.

To prevent data contention on the DQ bus during power on, it is required that the DQM and CKE pins be held high during the initial pause period. Once all banks have been precharged, the Mode Register Set Command must be issued to initialize the Mode Register. A minimum of eight Auto Refresh cycles (CBR) are also required, and these may be done before or after programming the Mode Register.

Simplified State Diagram



**Address Input for Mode Register Set**

BA1	BA0	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
Operation Mode							CAS Latency			BT	Burst Length		



Burst Length				
Sequential	Interleave	A2	A1	A0
1	1	0	0	0
2	2	0	0	1
4	4	0	1	0
8	8	0	1	1
Reserved	Reserved	1	0	0
Reserved	Reserved	1	0	1
Reserved	Reserved	1	1	0
Full Page	Reserved	1	1	1

Burst Type	A3
Interleave	1
Sequential	0

CAS Latency	A6	A5	A4
Reserved	0	0	0
Reserved	0	0	1
2	0	1	0
3	0	1	1
Reserved	1	0	0
Reserved	1	0	1
Reserved	1	1	0
Reserved	1	1	1

BA1	BA0	A11	A10	A9	A8	A7	Operation Mode
0	0	0	0	0	0	0	Normal
0	0	0	0	1	0	0	Burst Read with Single-bit Write

**Burst Type (A3)**

Burst Length	A2	A1	A0	Sequential Addressing	Interleave Addressing
2	X	X	0	0 1	0 1
	X	X	0	1 0	1 0
4	X	0	0	0 1 2 3	0 1 2 3
	X	0	1	1 2 3 0	1 0 3 2
	X	1	0	2 3 0 1	2 3 0 1
	X	1	1	3 0 1 2	3 2 1 0
8	0	0	0	0 1 2 3 4 5 6 7	0 1 2 3 4 5 6 7
	0	0	1	1 2 3 4 5 6 7 0	1 0 3 2 5 4 7 6
	0	1	0	2 3 4 5 6 7 0 1	2 3 0 1 6 7 4 5
	0	1	1	3 4 5 6 7 0 1 2	3 2 1 0 7 6 5 4
	1	0	0	4 5 6 7 0 1 2 3	4 5 6 7 0 1 2 3
	1	0	1	5 6 7 0 1 2 3 4	5 4 7 6 1 0 3 2
	1	1	0	6 7 0 1 2 3 4 5	6 7 4 5 2 3 0 1
	1	1	1	7 0 1 2 3 4 5 6	7 6 5 4 3 2 1 0
Full Page*	n	n	n	Cn Cn+1 Cn+2.....	-

\* Page length is a function of I/O organization and column addressing ×32 (CA0 ~ CA8):  
Full page = 512bits

**1. Command Truth Table**

Command	Symbol	CKE		/CS	/RAS	/CAS	/WE	BA0, BA1	A10	A11, A9~A10
		n-1	n							
Ignore Command	DESL	H	X	H	X	X	X	X	X	X
No Operation	NOP	H	X	L	H	H	H	X	X	X
Burst Stop	BSTH	H	X	L	H	H	L	X	X	X
Read	READ	H	X	L	H	L	H	V	L	V
Read with Auto Pre-charge	READA	H	X	L	H	L	H	V	H	V
Write	WRIT	H	X	L	H	L	L	V	L	V
Write with Auto Pre-charge	WRITA	H	X	L	L	H	H	V	H	V
Bank Activate	ACT	H	X	L	L	H	H	V	V	V
Pre-charge Select Bank	PRE	H	X	L	L	H	L	V	L	X
Pre-charge All Banks	PALL	H	X	L	L	H	L	X	H	X
Mode Register Set	MRS	H	X	L	L	L	L	L	L	V

H = High level, L = Low level, X = High or Low level (Don't care), V = Valid data input

**2. DQM Truth Table**

Command	Symbol	CKE		/CS
		n-1	n	
Data Write/Output Enable	ENB	H	X	H
Data Mask/Output Disable	MASK	H	X	L
Upper Byte Write Enable/Output Enable	BSTH	H	X	L
Read	READ	H	X	L
Read with Auto Pre-charge	READA	H	X	L
Write	WRIT	H	X	L
Write with Auto Pre-charge	WRITA	H	X	L
Bank Activate	ACT	H	X	L
Pre-charge Select Bank	PRE	H	X	L
Pre-charge All Banks	PALL	H	X	L
Mode Register Set	MRS	H	X	L

H = High level, L = Low level, X = High or Low level (Don't care), V = Valid data input

**3. CKE Truth Table**

Item	Command	Symbol	CKE		/CS	/RAS	/CAS	/WE	Addr.
			n-1	n					
Activating	Clock Suspend Mode Entry		H	L	X	X	X	X	X
Any	Clock Suspend Mode		L	L	X	X	X	X	X
Clock Suspend	Clock Suspend Mode Exit		L	H	X	X	X	X	X
Idle	CBR Refresh Command	REF	H	H	L	L	L	H	X
Idle	Self Refresh Entry	SELF	H	L	L	L	L	H	X
Self Refresh	Self Refresh Exit		L	H	L	H	H	H	X
			L	H	H	X	X	X	X
Idle	Power Down Entry		H	L	X	X	X	X	X
Power Down	Power Down Exit		L	H	X	X	X	X	X

**Remark** H = High level, L = Low level, X = High or Low level (Don't care)

**4. Operative Command Table** (Note 7)

Current State	/CS	/R	/C	/W	Addr.	Command	Action
Idle	H	X	X	X	X	DESL	Nop or power down (Note 8)
	L	H	H	X	X	NOP or BST	Nop or power down (Note 8)
	L	H	L	H	BA/CA/A10	READ/READA	ILLEGAL (Note 9)
	L	H	L	L	BA/CA/A10	WRIT/WRITA	ILLEGAL (Note 9)
	L	L	H	H	BA/RA	ACT	Row activating
	L	L	H	L	BA, A10	PRE/PALL	Nop
	L	L	L	H	X	REF/SELF	Refresh or self refresh (Note 10)
	L	L	L	L	Op-Code	MRS	Mode register accessing
Row Active	H	X	X	X	X	DESL	Nop
	L	H	H	X	X	NOP or BST	Nop
	L	H	L	H	BA/CA/A10	READ/READA	Begin read: Determine AP (Note 11)
	L	H	L	L	BA/CA/A10	WRIT/WRITA	Begin write: Determine AP (Note 11)
	L	L	H	H	BA/RA	ACT	ILLEGAL (Note 9)
	L	L	H	L	BA, A10	PRE/PALL	Pre-charge (Note 12)
	L	L	L	H	X	REF/SELF	ILLEGAL (Note 10)
	L	L	L	L	Op-Code	MRS	ILLEGAL
Read	H	X	X	X	X	DESL	Continue burst to end → Row active
	L	H	H	H	X	NOP	Continue burst to end → Row active
	L	H	H	L	X	BST	Burst stop → Row active
	L	H	L	H	BA/CA/A10	READ/READA	Terminate burst, new read: Determine AP (Note 13)
	L	L	L	L	BA/CA/A10	WRIT/WRITA	Terminate burst, start write: Determine AP (Note 13, 14)
	L	L	H	H	BA/RA	ACT	ILLEGAL (Note 9)
	L	L	H	L	BA, A10	PRE/PALL	Terminate burst, pre-charging (Note 10)
	L	L	L	H	X	REF/SELF	ILLEGAL
	L	L	L	L	Op-Code	MRS	ILLEGAL
Write	H	X	X	X	X	DESL	Continue burst to end → Write recovering
	L	H	H	H	X	NOP	Continue burst to end → Write recovering
	L	H	H	L	X	BST	Burst stop → Row active
	L	H	L	H	BA/CA/A10	READ/READA	Terminate burst, start read: Determine AP 7, 8 (Note 13, 14)
	L	L	L	L	BA/CA/A10	WRIT/WRITA	Terminate burst, new write: Determine AP 7 (Note 13)
	L	L	H	H	BA/RA	ACT	ILLEGAL (Note 9)
	L	L	H	L	BA, A10	PRE/PALL	Terminate burst, pre-charging (Note 15)
	L	L	L	H	X	REF/SELF	ILLEGAL
	L	L	L	L	Op-Code	MRS	ILLEGAL

Remark H = High level, L = Low level, X = High or Low level (Don't care)

4. Operative Command Table (Continued) (Note 7)

Current State	/CS	/R	/C	/W	Addr.	Command	Action
Read with AP	H	X	X	X	X	DESL	Continue burst to end → Pre-charging
	L	H	H	H	X	NOP	Continue burst to end → Pre-charging
	L	H	H	L	X	BST	ILLEGAL
	L	H	L	H	BA/CA/A10	READ/READA	ILLEGAL (Note 9)
	L	H	L	L	BA/CA/A10	WRIT/WRITA	ILLEGAL (Note 9)
	L	L	H	H	BA/RA	ACT	ILLEGAL (Note 9)
	L	L	H	L	BA, A10	PRE/PALL	ILLEGAL (Note 9)
	L	L	L	H	X	REF/SELF	ILLEGAL
	L	L	L	L	Op-Code	MRS	ILLEGAL
Write with AP	H	X	X	X	X	DESL	Burst to end → Write recovering with auto pre-charge
	L	H	H	H	X	NOP	Continue burst to end → Write recovering with auto pre-charge
	L	H	H	L	X	BST	ILLEGAL
	L	H	L	H	BA/CA/A10	READ/READA	ILLEGAL (Note 9)
	L	H	L	L	BA/CA/A10	WRIT/WRITA	ILLEGAL (Note 9)
	L	L	H	H	BA/RA	ACT	ILLEGAL (Note 9)
	L	L	H	L	BA, A10	PRE/PALL	ILLEGAL (Note 9)
	L	L	L	H	X	REF/SELF	ILLEGAL
	L	L	L	L	Op-Code	MRS	ILLEGAL
Pre-charging	H	X	X	X	X	DESL	Nop → Enter idle after t <sub>RP</sub>
	L	H	H	H	X	NOP	Nop → Enter idle after t <sub>RP</sub>
	L	H	H	L	X	BST	ILLEGAL
	L	H	L	H	BA/CA/A10	READ/READA	ILLEGAL (Note 9)
	L	H	L	L	BA/CA/A10	WRIT/WRITA	ILLEGAL (Note 9)
	L	L	H	H	BA/RA	ACT	ILLEGAL (Note 9)
	L	L	H	L	BA, A10	PRE/PALL	Nop → Enter idle after t <sub>RP</sub>
	L	L	L	H	X	REF/SELF	ILLEGAL
	L	L	L	L	Op-Code	MRS	ILLEGAL
Row Activating	H	X	X	X	X	DESL	Nop → Enter idle after t <sub>RCD</sub>
	L	H	H	H	X	NOP	Nop → Enter idle after t <sub>RCD</sub>
	L	H	H	L	X	BST	ILLEGAL
	L	H	L	H	BA/CA/A10	READ/READA	ILLEGAL (Note 9)
	L	H	L	L	BA/CA/A10	WRIT/WRITA	ILLEGAL (Note 9)
	L	L	H	H	BA/RA	ACT	ILLEGAL (Note 9, 16)
	L	L	H	L	BA, A10	PRE/PALL	ILLEGAL (Note 9)
	L	L	L	H	X	REF/SELF	ILLEGAL
	L	L	L	L	Op-Code	MRS	ILLEGAL

Remark H = High level, L = Low level, X = High or Low level (Don't care), AP = Auto Pre-charge

4. Operative Command Table (Continued) (Note 7)

Current State	/CS	/R	/C	/W	Addr.	Command	Action
Write Recovering	H	X	X	X	X	DESL	Nop → Enter row active after t <sub>DPL</sub>
	L	H	H	H	X	NOP	Nop → Enter row active after t <sub>DPL</sub>
	L	H	H	L	X	BST	Nop → Enter row active after t <sub>DPL</sub>
	L	H	L	H	BA/CA/A10	READ/READA	Start read, Determine AP
	L	H	L	L	BA/CA/A10	WRIT/WRITA	New write, Determine AP (Note 14)
	L	L	H	H	BA/RA	ACT	ILLEGAL (Note 9)
	L	L	H	L	BA, A10	PRE/PALL	ILLEGAL (Note 9)
	L	L	L	H	X	REF/SELF	ILLEGAL
Write Recovering with AP	L	L	L	L	Op-Code	MRS	ILLEGAL
	H	X	X	X	X	DESL	Nop → Enter pre-charge after t <sub>DPL</sub>
	L	H	H	H	X	NOP	Nop → Enter pre-charge after t <sub>DPL</sub>
	L	H	H	L	X	BST	Nop → Enter pre-charge after t <sub>DPL</sub>
	L	H	L	H	BA/CA/A10	READ/READA	ILLEGAL (Note 9, 14)
	L	H	L	L	BA/CA/A10	WRIT/WRITA	ILLEGAL (Note 9)
	L	L	H	H	BA/RA	ACT	ILLEGAL (Note 9)
	L	L	H	L	BA, A10	PRE/PALL	ILLEGAL
Refreshing	L	L	L	H	X	REF/SELF	ILLEGAL
	L	L	L	L	Op-Code	MRS	ILLEGAL
	H	X	X	X	X	DESL	Nop → Enter idle after t <sub>RC</sub>
	L	H	H	X	X	NOP/BST	Nop → Enter idle after t <sub>RC</sub>
	L	H	L	X	X	READ/WRIT	ILLEGAL
Mode Register Accessing	L	L	L	X	X	ACT/PRE/PALL	ILLEGAL
	L	L	L	X	X	REF/SELF/MRS	ILLEGAL
	H	X	X	X	X	DESL	Nop
	L	H	H	H	X	NOP	Nop
	L	H	H	L	X	BST	ILLEGAL
	L	H	L	X	X	READ/WRIT	ILLEGAL
	L	L	X	X	X	ACT/PRE/PALL/REF/SELF/MRS	ILLEGAL

**Remark** H = High level, L = Low level, X = High or Low level (Don't care), AP = Auto Pre-charge

**Note 7:** All entries assume that CKE was active (High level) during the preceding clock cycle.

**Note 8:** If all banks are idle, and CKE is inactive (Low level), SDRAM will enter Power down mode. All input buffers except CKE will be disabled.

**Note 9:** Illegal to bank in specified states;

Function may be legal in the bank indicated by Bank Address (BA), depending on the state of that bank.

**Note 10:** If all banks are idle, and CKE is inactive (Low level), SDRAM will enter Self refresh mode. All input buffers except CKE will be disabled.

**Note 11:** Illegal if t<sub>RC</sub>D is not satisfied.

**Note 12:** Illegal if t<sub>RAS</sub> is not satisfied.

**Note 13:** Must satisfy burst interrupt condition.

**Note 14:** Must satisfy bus contention, bus turn around, and/or write recovery requirements.

**Note 15:** Must mask preceding data which don't satisfy t<sub>DPL</sub>.

**Note 16:** Illegal if t<sub>RRD</sub> is not satisfied.



5. Command Truth Table for CKE

Current State	CKE		/CS	/R	/C	/W	Addr.	Action
	n-1	n						
Self Refresh	H	X	X	X	X	X	X	INVALID, CLK(n-1) would exit self refresh
	L	H	H	X	X	X	X	Self refresh recovery
	L	H	L	H	H	X	X	Self refresh recovery
	L	H	L	H	L	X	X	ILLEGAL
	L	H	L	L	X	X	X	ILLEGAL
	L	L	X	X	X	X	X	Maintain self refresh
Self Refresh Recovery	H	H	H	X	X	X	X	Idle after $t_{RC}$
	H	H	L	H	H	X	X	Idle after $t_{RC}$
	H	H	L	H	L	X	X	ILLEGAL
	H	H	L	L	X	X	X	ILLEGAL
	H	L	H	X	X	X	X	ILLEGAL
	H	L	L	H	H	X	X	ILLEGAL
	H	L	L	H	L	X	X	ILLEGAL
Power Down	H	X	X	X	X	X	X	INVALID, CLK(n-1) would exit power down
	L	H	X	X	X	X	X	Exit power down → Idle
	L	L	X	X	X	X	X	Maintain power down mode
Both Banks Idle	H	H	H	X	X	X		Refer to operations in Operative Command Table
	H	H	L	H	X	X		
	H	H	L	L	H	X		
	H	H	L	L	L	H	X	Refresh
	H	H	L	L	L	L	Op-Code	Refer to operations in Operative Command Table
	H	L	H	X	X	X		
	H	L	L	H	X	X		
	H	L	L	L	H	X		
	H	L	L	L	L	H	X	Self refresh <i>(Note 17)</i>
	H	L	L	L	L	L	Op-Code	Refer to operations in Operative Command Table
L	X	X	X	X	X	X	Power down <i>(Note 17)</i>	
Row Active	H	X	X	X	X	X	X	Refer to operations in Operative Command Table
	L	X	X	X	X	X	X	Power down <i>(Note 17)</i>
Any State Other than Listed above	H	H	X	X	X	X		Refer to operations in Operative Command Table
	H	L	X	X	X	X	X	Begin clock suspend next cycle <i>(Note 18)</i>
	L	H	X	X	X	X	X	Exit clock suspend next cycle
	L	L	X	X	X	X	X	Maintain clock suspend

**Remark:** H = High level, L = Low level, X = High or Low level (Don't care)

**Notes 17:** Self refresh can be entered only from the both banks idle state.

Power down can be entered only from both banks idle or row active state.

**Notes 18:** Must be legal command as defined in Operative Command Table

Package Description

90-ball FBGA

Solder ball: Lead free (Sn-Ag-Cu)

Unit: mm

