EXAR

XR-16C550

T-75-37-05

Universal Asynchronous Receiver / Transmitter with FIFOs

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GENERAL DESCRIPTION

The XR-16C550 is a universal asynchronous receiver and transmitter with an on-chip FIFO and modem control signal compatibility. An internal programmable baud rate generator is provided to select transmit and receive clock rates from 50Hz to 112kHz. The XR-16C550 is fabricated on an advanced 1.2 µm CMOS process to achieve low power consumption and high operation speed .

FEATURES

Pin to pin and functional compatibility to VL16C550
Modem control signals (CTS~, RTS~, DSR~, DTR~, RI~, CD~)
16 byte programmable FIFO for transmit and receive sections
Programmable character lengths (5, 6, 7, 8)
Even, odd, or no parity bit generation and detection
Status report register
Independent transmit and receive control
TTL compatible inputs and outputs
448 kHz transmit/receive operation with 7.372 MHz crystal or external clock source
Enhanced current drive capability on all I/O ports

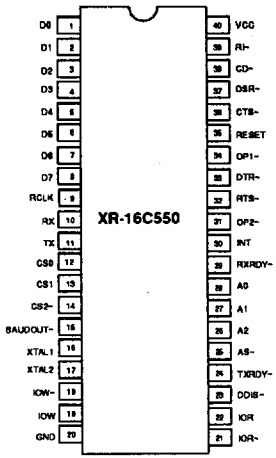
APPLICATIONS

RS232 receiver or transmitter
Serial to parallel/parallel to serial converter
Modem handshaking
IBM PS/2 serial port
Multimedia Systems

ABSOLUTE MAXIMUM RATINGS

Operating Supply Range	5 Volts ± 5%
Voltage at any Pin	GND-0.3 V to VCC+0.3 V
Operating Temperature	0°C to +70°C
Storage Temperature	-40°C to +150°C
Package Dissipation	500 mW

PIN ASSIGNMENT



Please refer to page 19 for PLCC Pin Assignment

ORDERING INFORMATION

Part number	Package	Operating Temperature
XR-16C550CP	Plastic	0°C to + 70°C
XR-16C550CJ	PLCC	0°C to + 70°C

SYSTEM DESCRIPTION

The XR-16C550 is an improved version of the VL16C550 UART with higher operating speed and lower access time. The XR-16C550 performs the parallel to serial and serial to parallel conversion on the data characters received from a CPU or MODEM. The on chip status registers will provide the error conditions, as well as the type and status of the transfer operations being performed. Also included in the XR-16C550 is a complete MODEM control capability, and a processor interrupt system. The latter may be software tailored to the user's requirements thereby allowing the user to minimize the computing time required to service the communications link. The on-chip 16 byte FIFO (plus 3 bits of error data per byte in the RX-FIFO) and two DMA signaling functions are provided to also assist in minimizing system computing overhead and maximizing system efficiency.The XR-16C550 also provides an internal loop-back capability for on-board diagnostic testing.

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DC ELECTRICAL CHARACTERISTICS

Test Conditions: TA=25° C, VCC=5.0 V ± 5% unless otherwise specified.

Symbol	Parameter	Limits			Units	Conditions
		min	typ	max		
VILCK	Clock input low level	-0.5		0.6	V	
VIHCK	Clock input high level	3.0		VCC	V	
VIL	Input low level	-0.5		0.8	V	
VIH	Input high level	2.2		VCC	V	
VOL	Output low level			0.4	V	IOL= 6 mA on all outputs
VOH	Output high level	2.4			V	IOH= -6 mA
ICC	Avg power supply current			6	mA	
IIL	Input leakage			±10	µA	
ICL	Clock leakage			±10	µA	

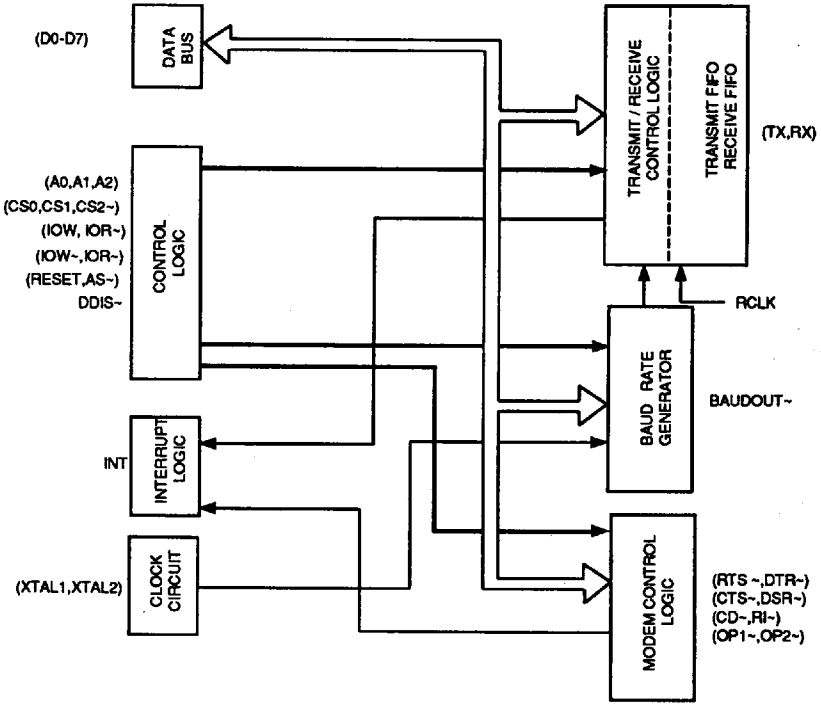

Figure 1. Block Diagram

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AC ELECTRICAL CHARACTERISTICS

Test Conditions: TA=25°C, VCC=5.0 V ± 5% unless otherwise specified.

Symbol	Parameter	Limits			Units	Conditions
		min	typ	max		
T1	Clock high pulse duration	55			ns	
T2	Clock low pulse duration	55			ns	External clock
T3	Clock rise/fall time					
T5	Address strobe width	30			ns	
T6	Address setup time	30			ns	
T7	Address hold time	5			ns	
T8	Chip select setup time	25			ns	
T9	Chip select hold time	0			ns	
T11	IOR~ to drive disable delay			35	ns	100 pF load
T12	Address hold time from IOW~	20			ns	Note: 1
T13	IOW~ delay from address	25			ns	Note: 1
T14	IOW~ delay from chip select	10			ns	Note: 1
T15	IOW~ strobe width	50			ns	
T16	Chip select hold time from IOW~	5			ns	Note: 1
T17	Write cycle delay	55			ns	
Tw	Write cycle=T15+T17	135			ns	
T18	Data setup time	20			ns	
T19	Data hold time	25			ns	
T20	Address hold time from IOR~	0			ns	Note: 1
T21	IOR~ delay from address	10			ns	Note: 1
T22	IOR~ delay from chip select	10			ns	Note: 1
T23	IOR~ strobe width	75			ns	
T24	Chip select hold time from IOR~	0			ns	Note: 1
T25	Read cycle delay	50			ns	
Tr	Read cycle=T23+T25	135			ns	
T26	Delay from IOR~ to data		75		ns	100 pF load
T27	IOR~ to floating data delay	0	50		ns	100 pF load

AC ELECTRICAL CHARACTERISTICS

Test Conditions: TA = 25°C, VCC = 5.0 V ± 5% unless otherwise specified

Symbol	Parameter	Limits			Units	Conditions
		min	typ	max		
MODEM CONTROL						
T28	Delay from IOW~ to output			50	ns	100 pF load
T29	Delay to set interrupt from MODEM input			70	ns	100 pF load
T30	Delay to reset interrupt from IOR~			70	ns	100 pF load
BAUD RATE GENERATOR						
N	Baud rate devisor	1		$2^{16}-1$		
T4	Baud out negative edge delay			100	ns	100 pF load
T4	Baud out positive edge delay			100	ns	100 pF load
RECEIVER						
T31	Delay from stop to set interrupt			^{1}Rclk	ns	100 pF load
T32	Delay from IOR~ to reset interrupt			200	ns	100 pF load
TRANSMITTER						
T33	Delay from initial INT reset to transmit start	8		24	*	
T34	Delay from stop to interrupt			100	ns	
T35	Delay from IOW~ to reset interrupt			125	ns	
T36	Delay from initial Write to interrupt	16		24	*	
T37	Delay from IOR~ to reset interrupt			75	ns	100 pF load

*Note 1: Applicable only when AS~ is tied low
Baudout~ cycle

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PIN DESCRIPTION

Pin#	Symbol	Type	Description
1-8	D0-D7	I/O	**Bidirectional Data Bus.** Eight bit, three state data bus to transfer information to or from the CPU. D0 is the least significant bit of the data bus and the first serial data bit to be received or transmitted.
9	RCLK	I	**Receive Clock Input.** The external clock input to the XR-16C550 receiver section.
10	RX	I	**Serial Data Input.** The serial information (data) received from MODEM or RS232 to XR-16C550 receive circuit. A mark (high) is logic one and a space (low) is logic zero. During the local loopback mode the RX input is disabled from external connection and connected to the TX output internally.
11	TX	O	**Serial Data Output.** The serial data is transmitted via this pin with additional start, stop and parity bits. The TX will be held in mark (high) state during reset, local loopback mode or when the transmitter is disabled.
12	CSO	I	**Chip Select 1 (active high).** A high at this pin (while CS1=1 and CS2~=0) will enable the UART / CPU data transfer operation.
13	CS1	I	**Chip Select 2 (active high).** A high at this pin (while CS0=1 and CS2~=0) will enable the UART / CPU data transfer operation.
14	CS2~	I	**Chip Select 3 (active low).** A low at this pin (while CS0=1 and CS1=1) will enable the UART / CPU data transfer operation.
15	BAUDOUT~	O	**Baud Rate Generator Clock Output.** This output provides the 16x clock of the internal selected baud rate.
16	XTAL1	I	**Crystal Input 1 or External Clock Input.** A crystal can be connected to this pin and XTAL2 pin to utilize the internal oscillator circuit. An external clock can be used to clock internal circuit and baud rate generator for custom transmission rates.
17	XTAL2	I	**Crystal Input 2.** See XTAL1.
18	IOW~	I	**Write Strobe (active low).** A low on this pin will transfer the contents of the CPU data bus to the addressed register.
19	IOW	I	**Write Strobe (active high).** Same as IOW~, but uses active high input. Note that only an active IOW~ or IOW input is required to transfer data from CPU to XR-16C550 during write operation (while CS0=1, CS1=1 and CS2~=0). The unused pin should be tied to VCC or GND (IOW = GND or IOW~=VCC) .
20	GND	O	**Signal and Power Ground.**

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Pin#	Symbol	Type	Description
21	IOR~	I	**I/O Read Strobe (active low).** A low level on this pin (while CS0=1, CS1=1 and CS2~=0) will transfer the contents of the XR-16C550 data bus to the CPU.
22	IOR	I	**Read Strobe (active high).** Same as IOR~, but uses active high input. Note that only an active IOR~ or IOR input is required to transfer data from XR-16C550 to CPU during read operation (while CS0=1, CS1=1 and CS2~=0). The unused pin should be tied to VCC or GND (IOR=GND or IOR~=VCC) .
23	DDIS~	O	**Drive Disable (active low).** This pin goes low when the CPU is reading data from the XR-16C550 to disable the external transceiver or logics.
24	TXRDY~	O	**Transmit Ready (active low).** This pin goes low when the transmit FIFO of the XR-16C550 is full. It can be used as a single or multitransfer DMA.
25	AS~	I	**Address Strobe (active low).** A low on this pin will latch the state of the chip selects and addressed register (A2-A0). This input is used when signals are not stable for the duration of a read or write operation. If not required, tie the AS~ input permanently low.
26	A2	I	**Address Line 2.** To select internal registers.
27	A1	I	**Address Line 1.** To select internal registers.
28	A0	I	**Address Line 0.** To select internal registers.
29	RXRDY~	O	**Receive Ready (active low).** This pin goes low when the receive FIFO is full. It can be used as a single or multitransfer DMA.
30	INT	O	**Interrupt Output (active high).** This pin goes high (when enabled by the interrupt enable register) whenever a receiver error, receiver data available, transmitter empty, or modem status condition flag is detected.
31	OP2~	O	**General Purpose Output (active low).** User defined output. See bit-3 modem control register.
32	RTS~	O	**Request to Send (active low).** To indicate that the transmitter has data ready to send. Writing a "1" in the modem control register (MCR bit-1) will set this pin to a low state. After the reset this pin will be set to high.
33	DTR~	O	**Data Terminal Ready (active low).** To indicate that the XR-16C550 is ready to receive data. This pin can be controlled via the modem control register (MCR bit-0). Writing a "1" to the MCR bit-0 will set the DTR~ output to low. This pin will be set to high state after writing a "0" to that register or after a reset.
34	OP1~	O	**General Purpose Output (active low).** User defined output. See bit-2 of modem control register.

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Pin#	Symbol	Type	Description
35	RESET	I	**Master Reset (active high).** A high on this pin will reset all the outputs and internal registers. The transmitter output and the receiver input will be disabled during reset time.
36	CTS~	I	**Clear to Send (active low).** The CTS~ signal is a MODEM control function input whose conditions can be tested by reading the MSR BIT-4. CTS~ has no effect on the transmitter output.
37	DSR~	I	**Data Set Ready (active low).** A low on this pin indicates the MODEM is ready to exchange data with the UART.
38	CD~	I	**Carrier Detect (active low).** A low on this pin indicates the carrier has been detected by the modem.
39	RI~	I	**Ring Detect Indicator (active low).** A low on this pin indicates the modem has received a ringing signal from the telephone line.
40	VCC	I	**Power Supply Input.**

PROGRAMMING TABLE

DLAB	A2	A1	A0	READ MODE	WRITE MODE
0	0	0	0	Receive Holding Register	Transmit Holding Register
0	0	0	1		Interrupt Enable Register
x	0	1	0	Interrupt Status Register	FIFO Control Register
x	0	1	1		Line Control Register
x	1	0	0		Modem Control Register
x	1	0	1	Line Status Register	
x	1	1	0	Modem Status Register	
x	1	1	1	Scratchpad Register	Scratchpad Register
1	0	0	0		LSB of Divisor Latch
1	0	0	1		MSB of Divisor Latch

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XR-16C550 ACCESSIBLE REGISTERS

A2	A1	A0	Register	BIT-7	BIT-6	BIT-5	BIT-4	BIT-3	BIT-2	BIT-1	BIT-0
0	0	0	**RHR**	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
0	0	0	**THR**	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
0	0	1	**IER**	0	0	0	0	modem status interrupt	receive line status interrupt	transmit holding register	receive holding register
0	1	0	**FCR**	RCVR trigger (MSB)	RCVR trigger (LSB)	0	0	DMA mode select	XMIT FIFO reset	RCVR FIFO reset	FIFO enable
0	1	0	**ISR**	0/ FIFOs enabled	0/ FIFOs enabled	0	0	0	int priority bit-1	int priority bit-0	int status
0	1	1	**LCR**	divisor latch enable	set break	set parity	even parity	parity enable	stop bits	word length bit-1	word length bit-0
1	0	0	**MCR**	0	0	0	loop back	OP2~	OP1~	RTS~	DTR~
1	0	1	**LSR**	0/ FIFO error	trans. empty	trans. holding empty	break interrupt	framing error	parity error	overrun error	receive data ready
1	1	0	**MSR**	CD	RI	DSR	CTS	delta CD~	delta RI~	delta DSR~	delta CTS~
1	1	1	**SPR**	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
0	0	0	**DLL**	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
0	0	1	**DLM**	bit-15	bit-14	bit-13	bit-12	bit-11	bit-10	bit-9	bit-8

REGISTER FUNCTIONAL DESCRIPTIONS

Transmit and Receive Holding Register

The serial transmitter section consists of a Transmit Hold Register (THR) and Transmit Shift Register (TSR). The status of the transmit hold register is provided in the Line Status Register (LSR). Writing to this register will transfer the contents of the data bus (D7-D0) to the Transmit holding register whenever the transmitter holding register or transmitter shift register is empty. The transmit holding register empty flag will be set to "1" when the transmitter is empty or data is transferred to the transmit shift register. Note that a write operation should be performed when the transmit holding register empty flag is set.

On the falling edge of the start bit, the receiver internal counter will start to count 7 1/2 clocks (16x clock) which is the center of the start bit. The start bit is valid if the SIN is still low at the mid-bit sample of the start bit. Verifying the start bit prevents the receiver from assembling a false data character due to a low going noise spike on the SIN input. Receiver status codes will be posted in the Line Status Register.

FIFO Interrupt Mode Operation

When the receive FIFO (FCR BIT-0=1) and receive interrupts (IER BIT-0=1) are enabled, receiver interrupt will occur as follows:

A) The receive data available interrupts will be issued to the CPU when the FIFO has reached its programmed trigger level; it will be cleared as soon as the FIFO drops below its programmed trigger level.

B) The ISR receive data available indication also occurs when the FIFO trigger level is reached, and like the interrupt it is cleared when the FIFO drops below the trigger level.

C) The data ready bit (LSR BIT-0) is set as soon as a character is transferred from the shift register to the receiver FIFO. It is reset when the FIFO is empty.

FIFO Polled Mode Operation

When FCR BIT-0=1; resetting IER BIT 3-0 to zero puts the XR-16C550 in the FIFO polled mode of operation. Since the receiver and transmitter are controlled separately either one or both can be in the polled mode operation by utilizing the Line Status Register.

A) LSR BIT-0 will be set as long as there is one byte in the receive FIFO.

B) LSR BIT4-1 will specify which error(s) has occurred.

C) LSR BIT-5 will indicate when the transmit FIFO is empty.

D) LSR BIT-6 will indicate when both transmit FIFO and transmit shift registers are empty.

E) LSR BIT-7 will indicate when there are any errors in the receive FIFO.

Programmable Baud Rate Generator

The XR-16C550 contains a programmable Baud Rate Generator that is capable of taking any clock input from DC to 16 MHz and dividing it by any divisor from 2 to 2^{16} -1. The output frequency of the Baudout~ is equal to 16X of the transmission baud rate (Baudout~=16 x Baud Rate). Baud Rates can be achieved by selecting proper divisor values for MSB and LSB of the baud rate generator.

INTERRUPT ENABLE REGISTER (IER)

The Interrupt Enable Register (IER) masks the incoming interrupts from receiver ready, transmitter empty, line status and modem status registers to the INT output pin.

IER BIT-0:
0=disable the receiver ready interrupt.
1=enable the receiver ready interrupt.

IER BIT-1:
0=disable the transmitter empty interrupt.
1=enable the transmitter empty interrupt.

IER BIT-2:
0=disable the receiver line status interrupt.
1=enable the receiver line status interrupt.

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IER BIT-3:
0=disable the modem status register interrupt.
1=enable the modem status register interrupt.

IER BIT 7-4:
All these bits are set to logic zero.

INTERRUPT STATUS REGISTER (ISR)

The XR-16C550 provides four level prioritized interrupt conditions to minimize software overhead during data character transfers. The Interrupt Status Register (ISR) provides the source of the interrupt in prioritized matter. During the read cycle the XR-16C550 provides the highest interrupt level to be serviced by CPU. No other interrupts are acknowledged until the particular interrupt is serviced. The following are the prioritized interrupt levels:

Priority level				Source of the interrupts
P	D2	D1	D0	
1	1	1	0	LSR (Receiver Line Status Register)
2	1	0	0	RXRDY (Received Data Ready)
3	0	1	0	TXRDY(Transmitter Holding Register Empty)
4	0	0	0	MSR (Modem Status Register)

ISR BIT-0:
0=an interrupt is pending and the ISR contents may be used as a pointer to the appropriate interrupt service routine.
1=no interrupt pending.

ISR BIT 1-2:
Logical combination of these bits, provides the highest priority interrupt pending.

ISR BIT 3-7:
These bits are not used and are set to zero in XR-16C450 mode. BIT 6-7: are set to "1" in XR-16C550 mode.

FIFO CONTROL REGISTER (FCR)

This register is used to enable the FIFOs, clear the FIFOs, set the receiver FIFO trigger level, and select the type of DMA signalling.

FCR BIT-0:
0=Disable the transmit and receive FIFO.
1=Enable the transmit and receive FIFO.

FCR BIT-1:
0=No change.
1=Clears the contents of the receive FIFO and resets its counter logic to 0 (the receive shift register is not cleared or altered). This bit will return to zero after clearing the FIFOs.

FCR BIT-2:
0=No change.
1=Clears the contents of the transmit FIFO and resets its counter logic to 0 (the transmit shift register is not cleared or altered). This bit will return to zero after clearing the FIFOs.

FCR BIT-3:
0=No change.
1=Changes RXRDY and TXRDY pins from mode "0" to mode "1".

FCR BIT 4-5:
Not used.

FCR BIT 6-7:
These bits are used to set the trigger level for the receiver FIFO interrupt.

BIT-7	BIT-6	FIFO trigger level
0	0	01
0	1	04
1	0	08
1	1	14

LINE CONTROL REGISTER (LCR)

The Line Control Register is used to specify the asynchronous data communication format. The number of the word length, stop bits, and parity can be selected by writing appropriate bits in this register.

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LCR BIT1-0:
These two bits specify the word length to be transmitted or received.

BIT-1	BIT-0	Word length
0	0	5
0	1	6
1	0	7
1	1	8

LCR BIT-2:
The number of stop bits can be specified by this bit.

BIT-2	World length	Stop bit(s)
0	5,6,7,8	1
1	5	1-1/2
1	6,7,8	2

LCR BIT-3:
Parity or no parity can be selected via this bit.
0=no parity
1=a parity bit is generated during the transmission, receiver also checks for received parity.

LCR BIT-4:
If the parity bit is enabled, LCR BIT-4 selects the even or odd parity format.
0=ODD parity is generated by forcing an odd number of 1's in the transmitted data, receiver also checks for same format.
1= EVEN parity bit is generated by forcing an even number of 1's in the transmitted data, receiver also checks for same format.

LCR BIT-5:
If the parity bit is enabled, LCR BIT-5 selects the forced parity format.
LCR BIT-5=1 and LCR BIT-4=0, parity bit is forced to "1" in the transmitted and received data.
LCR BIT-5=1 and LCR BIT-4=1, parity bit is forced to "0" in the transmitted and received data.

LCR BIT-6:
Break control bit. It causes a break condition to be transmitted (the TX is forced to low state).
0=normal operating condition.
1=forces the transmitter output (TX) to go low to alert the communication terminal.

LCR BIT-7:
The internal baud rate counter latch enable(DLAB).
0=normal operation.
1=select divisor latch register.

MODEM CONTROL REGISTER (MCR)

This register controls the interface with the MODEM or a peripheral device (RS232).

MCR BIT-0:
0=force DTR~ output to high.
1=force DTR~ output to low.

MCR BIT-1:
0=force RTS~ output to high.
1=force RTS~ output to low.

MCR BIT-2:
0=set OP1~ output to high.
1=set OP1~ output to low.

MCR BIT-3:
0=set OP2~ output to high.
1=set OP2~ output to low.

MCR BIT-4:
0=normal operating mode.
1=enable local loop-back mode (diagnostics). The transmitter output (TX) is set high (Mark condition), the receiver input (RX) , CTS~, DSR~, CD~, and RI~ are disabled. Internally the transmitter output is connected to the receiver input and DTR~, RTS~, OP1~ and OP2~ are connected to modem control inputs. In this mode , the receiver and transmitter interrupts are fully operational. The Modem Control Interrupts are also operational, but the interrupts sources are now the lower four bits of the Modem Control Register instead of the four Modem Control inputs. The interrupts are still controlled by the IER .

MCR BIT 5-7:
Not used. Are set to zero permanently.

LINE STATUS REGISTER (LSR)

This register provides the status of data transfer to CPU.

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LSR BIT-0:
0=no data in receive holding register or FIFO.
1=data has been received and saved in the receive holding register or FIFO.

LSR BIT-1:
0=no overrun error (normal).
1=overrun error, next character arrived before receive holding register was emptied or if FIFOs are enabled, an overrun error will occur only after the FIFO is full and the next character has been completely received in the shift register. The character in the shift register is overwritten, but it is not transferred to the FIFO.

LSR BIT-2:
0=no parity error (normal).
1=parity error, received data does not have correct parity information. In the FIFO mode this error is associated with the character at the top of the FIFO.

LSR BIT-3:
0=no framing error (normal).
1=framing error received, received data did not have a valid stop bit. In the FIFO mode this error is associated with the character at the top of the FIFO.

LSR BIT-4:
0=no break condition (normal).
1=a break signal was received by the receiver (RX was low for one character time frame). In the FIFO mode, only one zero character is loaded into the FIFO.

LSR BIT-5:
0=transmit holding register is full. XR-16C550 will not accept any data for transmission.
1=transmit holding register (or FIFO) is empty. CPU can load the next character.

LSR BIT-6:
0=transmitter holding and shift registers are full.
1=transmitter holding and shift registers are empty. In FIFO mode this bit is set to one whenever the transmitter FIFO and transmit shift register are empty.

LSR BIT-7:
0=Normal.
1=At least one parity error, framing error or break indication in the FIFO. This bit is cleared when LSR is read.

MODEM STATUS REGISTER (MSR)

This register provides the current state of the control lines from the modem or peripheral to the CPU. Four bits of this register are used to indicate the changed information. These bits are set to "1" whenever a control input from the MODEM changes state. They are set to "0" whenever the CPU reads this register.

MSR BIT-0:
Indicates that the CTS~ input to the XR-16C550 has changed state since the last time it was read.

MSR BIT-1:
Indicates that the DSR~ input to the XR-16C550 has changed state since the last time it was read.

MSR BIT-2:
Indicates that the RI~ input to the XR-16C550 has changed from a low to a high state.

MSR BIT-3:
Indicates that the CD~ input to the XR-16C550 has changed state since the last time it was read.

MSR BIT-4:
This bit is equivalent to RTS in the MCR during local loop-back mode. It is the compliment of the CTS~ input.

MSR BIT-5:
This bit is equivalent to DTR in the MCR during local loop-back mode. It is the compliment of the DSR~ input.

MSR BIT-6:
This bit is equivalent to OP1 in the MCR during local loop-back mode. It is the compliment of the RI~ input.

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MSR BIT-7:
This bit is equivalent to OP2 in the MCR during local loop-back mode. It is the compliment to the CD~ input.

Note: Whenever MSR BIT3-0: is set to logic "1", a MODEM Status Interrupt is generated.

SCRATCHPAD REGISTER (SR)

XR-16C550 provides a temporary data register to store 8 bits of information for variable use.

BAUD RATE GENERATOR PROGRAMMING TABLE (1.8432 MHz CLOCK):

BAUD RATE	16 x CLOCK DIVISOR	% ERROR
50	2304	
75	1536	
110	1047	0.026
134.5	857	0.058
150	768	
300	384	
600	192	
1200	96	
2400	48	
3600	32	
4800	24	
7200	16	
9600	12	
19.2K	6	
38.4K	3	
56K	2	2.86
112K	1	

XR-16C550 EXTERNAL RESET CONDITION

REGISTERS	RESET STATE
IER	IER BITS 0-7=0
ISR	ISR BIT-0=1, ISR BITS 1-7=0
LCR	LCR BITS 0-7=0
MCR	MCR BITS 0-7=0
LSR	LSR BITS 0-4=0, LSR BITS 5-6=1 LSR, BIT 7=0
MSR	MSR BITS 0-3=0, MSR BITS 4-7=input signals
FCR	FCR BITS 0-7=0

SIGNALS	RESET STATE
TX	High
OP1~	High
OP2~	High
RTS~	High
DTR~	High
INT	BITS 0-3=low

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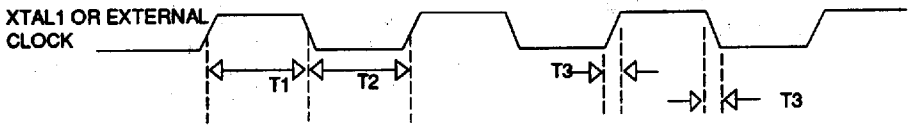
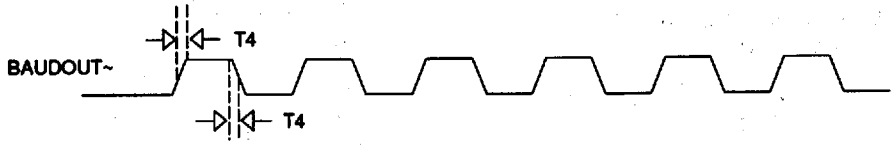
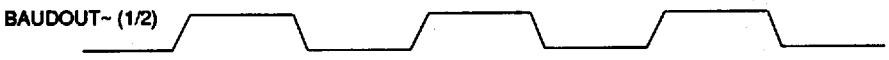
TIMING DIAGRAM

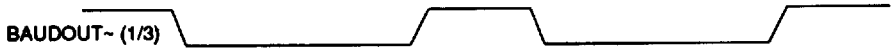
CLOCK TIMING

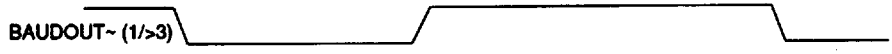


BAUDOUT~TIMING









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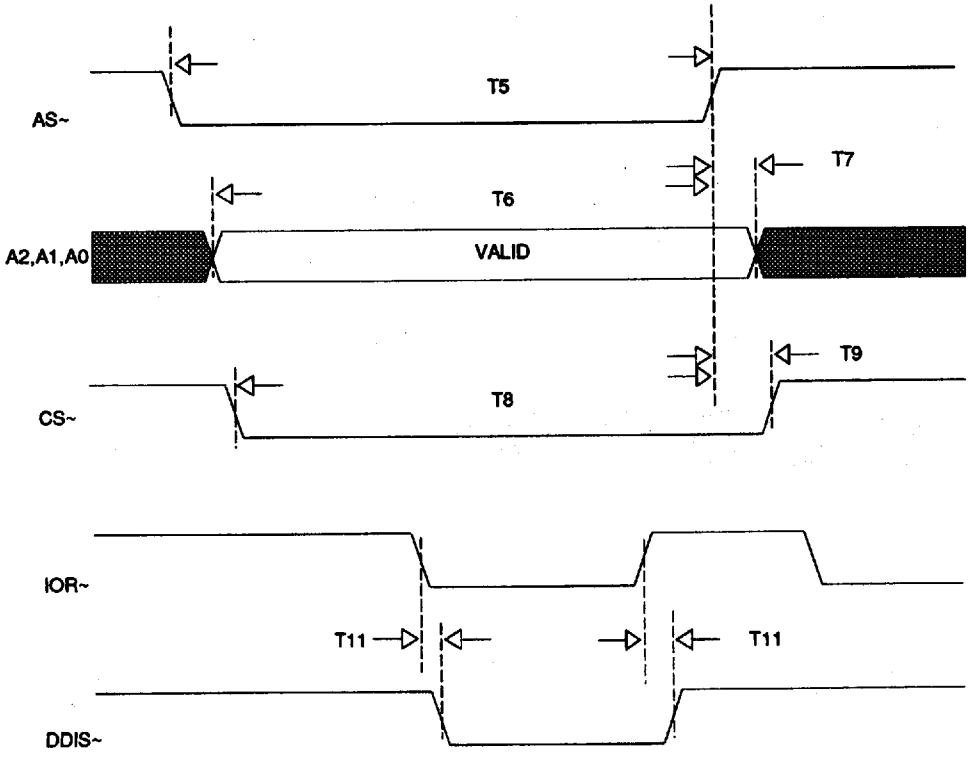
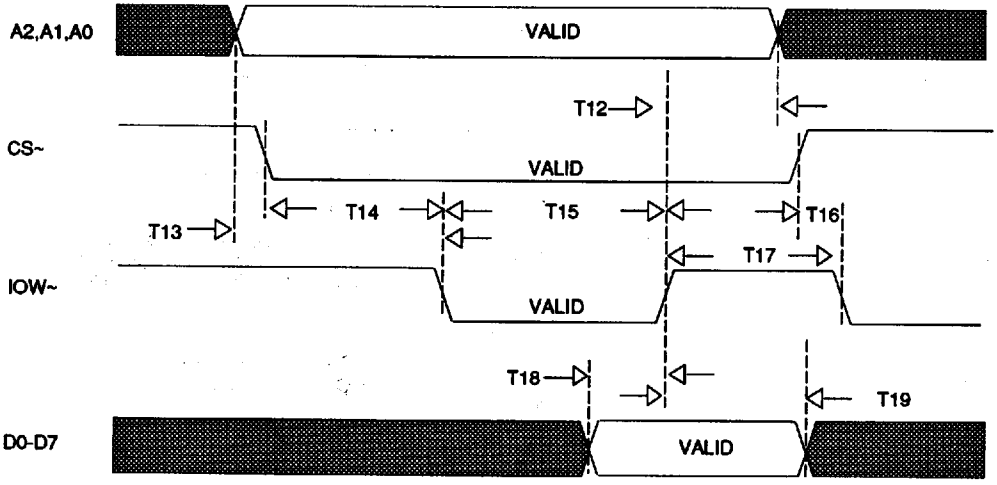
TIMING DIAGRAM

GENERAL TIMING

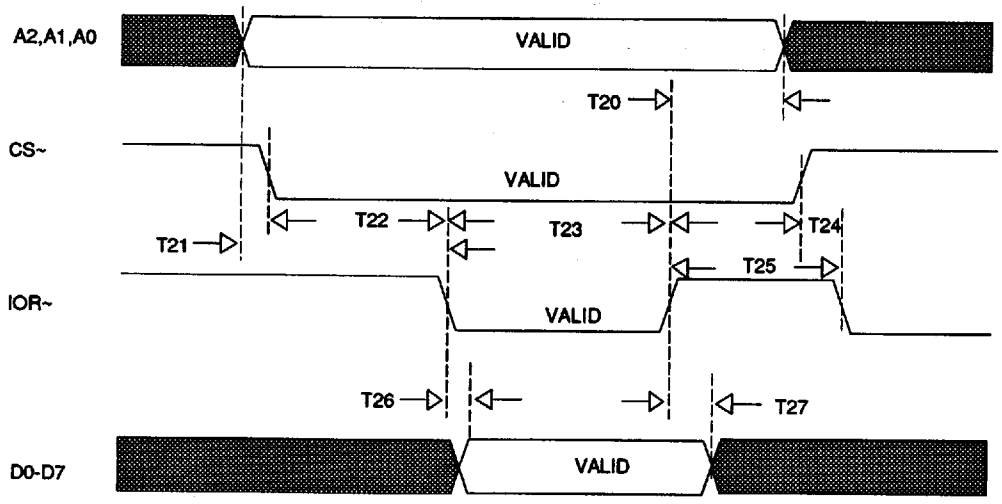


TIMING DIAGRAM

WRITE CYCLE TIMING



READ CYCLE TIMING



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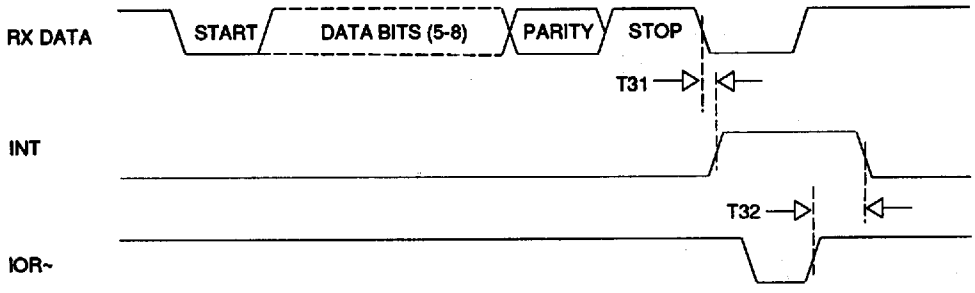
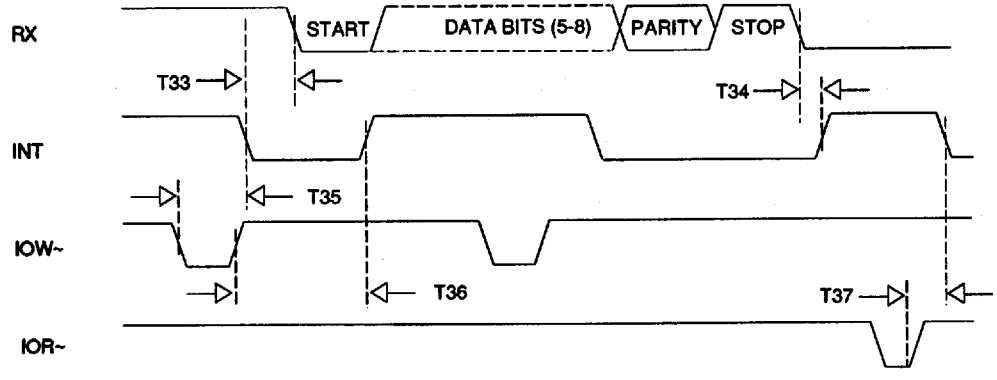
TIMING DIAGRAM

RECEIVER TIMING



TRANSMITTER TIMING



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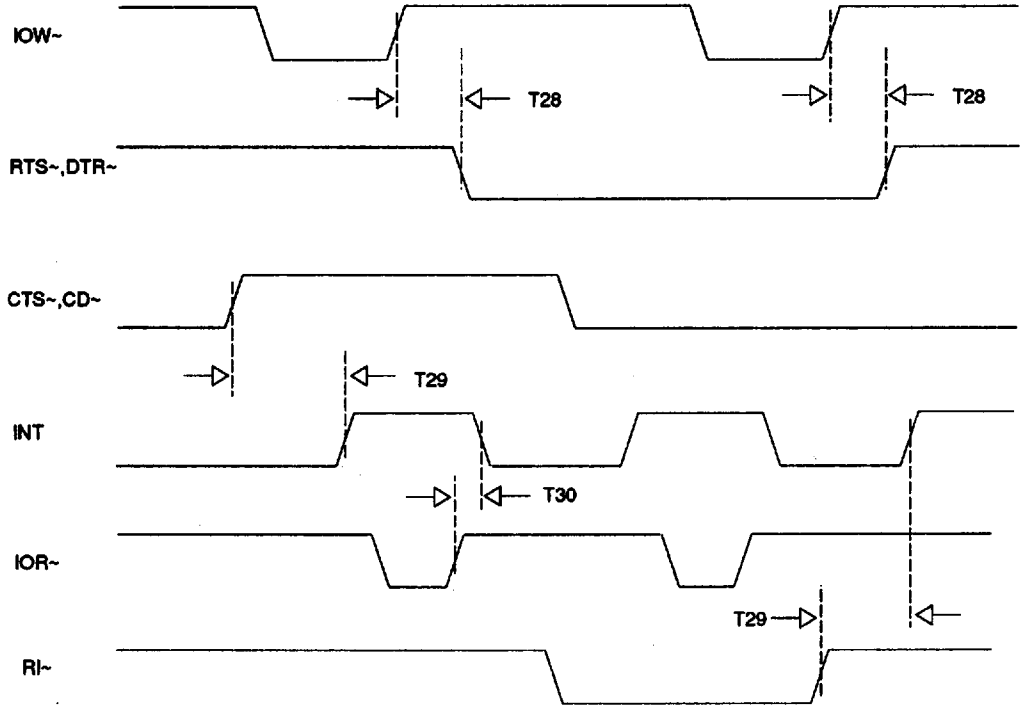
TIMING DIAGRAM

MODEM TIMING



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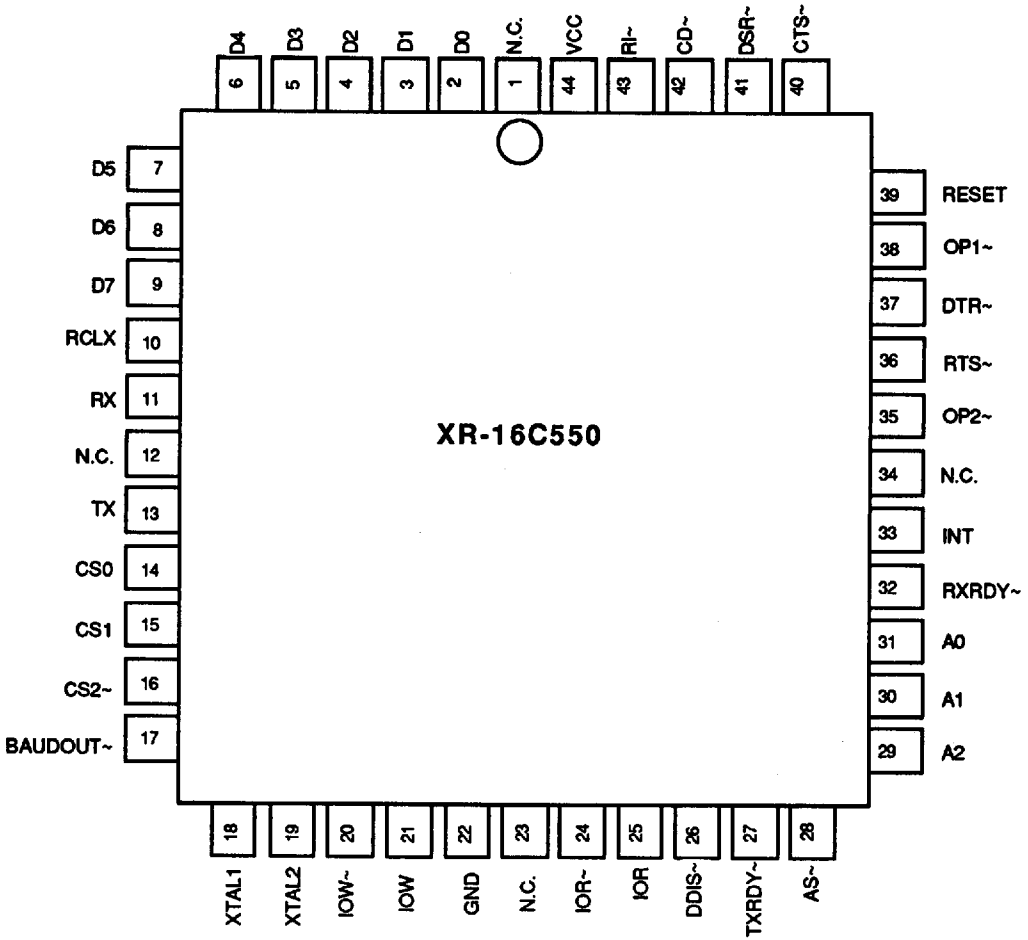
D4 6
D3 5
D2 4
D1 3
D0 2
N.C. 1
VCC 44
RI~ 43
CD~ 42
DSR~ 41
CTS~ 40
D5 7
D6 8
D7 9
RCLX 10
RX 11
N.C. 12
TX 13
CS0 14
CS1 15
CS2~ 16
BAUDOUT~ 17
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39 RESET
38 OP1~
37 DTR~
36 RTS~
35 OP2~
34 N.C.
33 INT
32 RXRDY~
31 A0
30 A1
29 A2
18 XTAL1
19 XTAL2
20 IOW~
21 IOW
22 GND
23 N.C.
24 IOR~
25 IOR
26 DDIS~
27 TXRDY~
28 AS~