Variable Delay Lines

VDS	Ultra High-Speed Variable Delay Lines

The VDS family of high-speed vailable delay lines is available in a dual in-line package for a variety of types in either standard or custom specifications.

FEATURES

- High-speed SMD delay lines that have achieved 40 step variability of delay time through a combination of 20 sections of ELMEC's own high-function, high-density delay line elements and high-increment variable structure.
- Suitable for application in a broad range of high-speed logic elements such as the ECL 10KH or 10K series as well as TTL FAST, CMOS FAST and others of similar switching speed.
- They are also suitable for use in a wide range of applications in analog circuits.

COMMON SPECIFICATIONS

Inherent Delay:	450ps max. at the minimum point within the variable range
Waveform Distortion:	Overshoot/preshoot under ±20%
Operating Temperature Range:	-10°C to +80°C
Storage Temperature Range:	-40°C to +120°C
Switching Life Expectancy:	Guaranteed within 100 cycles. (One cycle is defined as the movement of the knob from one end to the other.)

SPECIFICATIONS

Part Number	Delay Time Range -0 to +20%	Increment Resolution (40 Steps) *(1)		Rise Time	Input Impedence	Output Impedence	DC Max. Voltage	Preferred Logic Family
		1.75%	3.25%					
VDS5010	0-5ns	88ps	163ps	0.8ns Max. *(2)	50Ω±10%	100Ω±10%	DC 3V Max. Constantly	ECL10KH ECL10K TTL-FAST CMOS-FACT
VDS1110	0-10ns	175ps	325ps	1.3ns Max. *(2)				
VDS2110	0-20ns	350ps	650ps	2.3ns Max. *(2)				
VDS3110	0-30ns	525ps	975ps	4.0ns Max. *(2)				
VDS5020	0-5ns	88ps	163ps	2.0ns Max. *(3)	100Ω±10%	200Ω±10%	DC 4.5V Max. Voltage	
VDS1120	0-10ns	175ps	325ps	2.5ns Max. *(3)				
VDS2120	0-20ns	350ps	650ps	3.5ns Max. *(3)				

*(1) Changes at a ratio of 1.75% and 3.25% occur alternately.
*(2) 20%-80%.
*(3) 10%-90%.
Deray time temperature coefficient ±100ppm/°C(However, VDS 1110,2110,2120,3110 are -400±200ppm/°C).
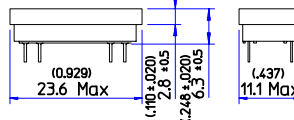
PACKAGE DIMENSIONS & PIN CONFIGURATION

Delay Time Control Knob
(We recommend use of our special tool when moving the selector knob)
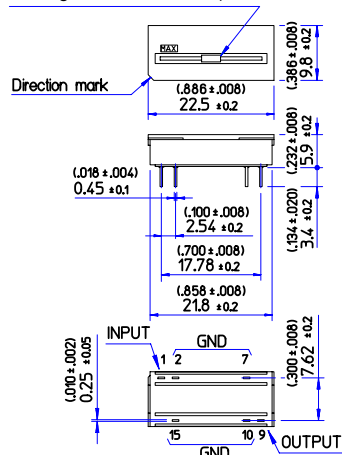
Unit:mm (inch)

In board design, please note the changes in the dimensions of the VDK Type indicated below when the dust cover cap is attached.

Direction mark

(.886±.008) 22.5 ±0.2
(.386±.008) 9.8 ±0.2
(.232±.008) 5.9 ±0.2
(.018±.004) 0.45 ±0.1
(.100±.008) 2.54 ±0.2
(.700±.008) 17.78 ±0.2
(.134±.020) 3.4 ±0.2
(.858±.008) 21.8 ±0.2

INPUT GND
1 2 7
(.010±.002) 0.25 ±0.05
(.300±.008) 7.62 ±0.2
15 10 9
GND OUTPUT

(0.929) 23.6 Max
(.110±.020) 2.8 ±0.5
(.248±.020) 6.3 ±0.5
(.437) 11.1 Max

Application Notes:
Care is to be exercised in aqueous cleaning since the VDK Type is not hermetically sealed.
We recommend hand soldering this part. A dust cover cap is provided on the top of each part.

Note: Published specifications are subject to change without prior notice.

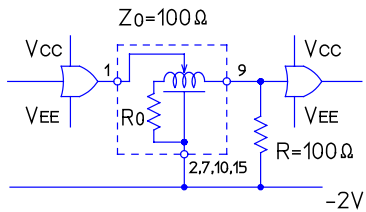| VDS	Ultra High-Speed Variable Delay Lines

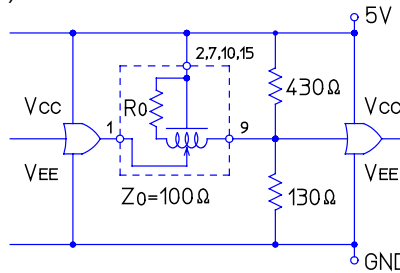## TYPICAL APPLICATIONS AND TERMINATION METHODS

(1) Analog circuit
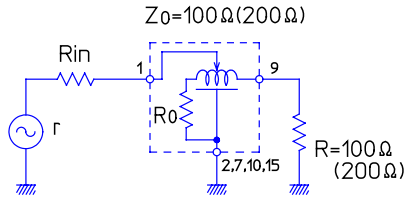
r   :Impedance of signal source
Rin:Input adjustment resistance
Zo :Characteristics impedance of internal
    Elements (=Output impedance)
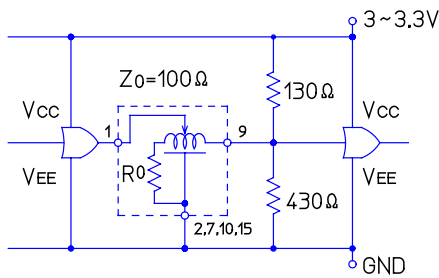Ro :Internal adjustment resistance (=Zo)
$2(r+Rin)=Zo=R$

(2) ECL (-2V termination line used)

(3) PECL
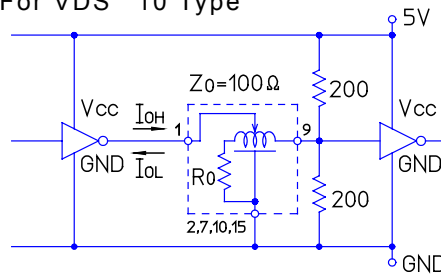

(4) LVPECL

(5) TTL(FAST)
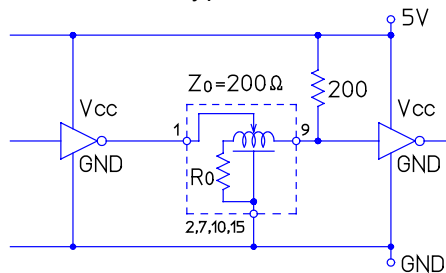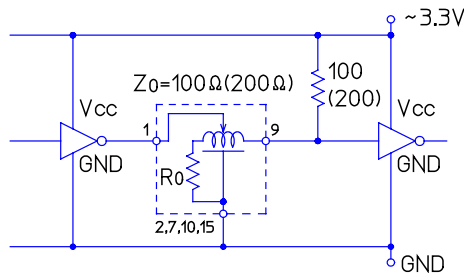For VDS**10 Type

I_{OH} is approx. 45mA, I_{OL} is approx. 15mA

(6) TTL(FAST)
For VDS**20 Type

(7) CMOS,LVCMOS

RoHS Compliance Status

Compliance Status
RoHS-compliant components are available.

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