CDAD Surface-Mount High-Speed Differential Delay Lines

The CDAD family of high-speed differential delay lines are available in surface-mount (SMD) packaging in either standard or custom specification.

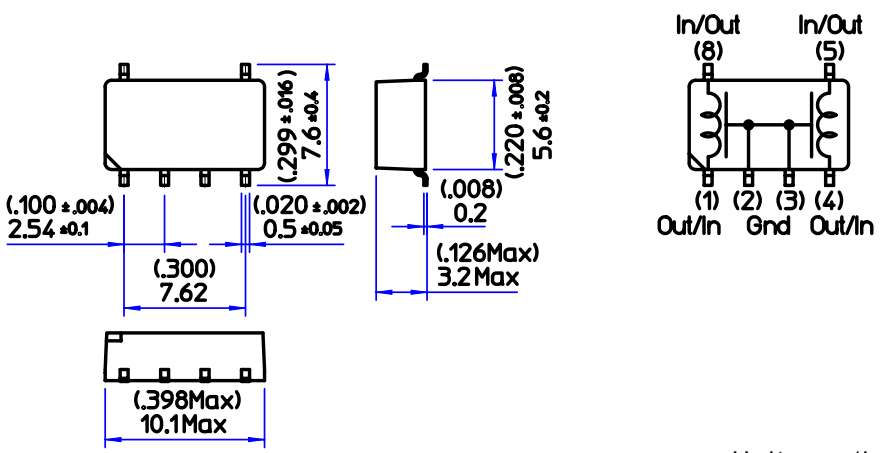
FEATURES

- Miniaturized high-speed differential delay lines that combine ELMEC's high-density delay line elements in the same surface-mount package as the CDA family of single fixed SMD delay line.
- Suitable for use with a variety of logic elements including the ECLinPS, ECL 100KH, 10K series as well as TTL FAST, CMOS FACT and analog circuits.
- The CDAD family of differential delay lines are cased in the exact same package and footprint so that it can be inserted onto the CDA family land pattern.

COMMON SPECIFICATIONS

Impedance:	single-ended: 50Ω±10% / differential: 100Ω±10%
Waveform Distortion:	Overshoot/preshoot under 20%
Temperature Coefficient:	0~150ppm/°C
Insulation Resistance:	DC50V, over 100M Ω
Durable Voltage:	DC50V, 1 minute
Operating Temperature Range:	-40°C to +85°C
Storage Temperature Range:	-40°C to +120°C

PACKAGE DIMENSIONS & PIN CONFIGURATION

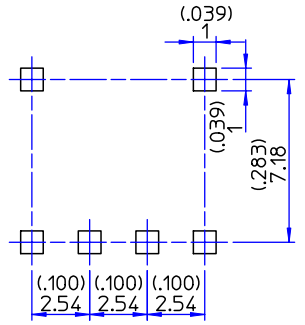


Unit:mm (inch)

CDAD Surface-Mount High-Speed Differential Delay Lines

SUGGESTED LAND PATTERN

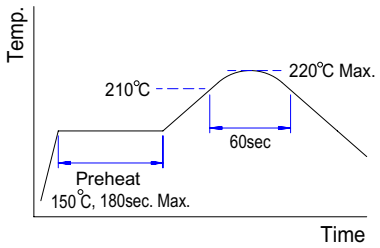
Unit:mm (inch)



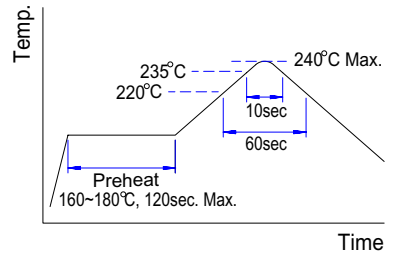
REFLOW SOLDERING CONDITIONS

ELMEC does not guarantee MSL Standards Classification. Please bake all components prior to reflow.
Baking Conditions:120°C, 24 hours; or 80°C, 100 hours
However, because baking of T&R parts is not possible, transferring to trays is recommended prior to baking.

Non-RoHS-compliant components
Maximum Reflow Cycles:1



RoHS-compliant components
Maximum Reflow Cycles:2



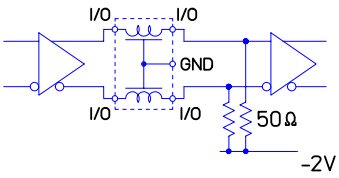
SPECIFICATIONS

Part Number	Delay Time	Delay Difference	Rise Time (20%-80% Max)	-3 dB Passband (Minimum)	DC Resistance
CDAD0105	100ps±50ps	15ps Max	150ps	2GHz	1.5Ω Max
CDAD0205	200ps±50ps				
CDAD0305	300ps±50ps				
CDAD0405	400ps±50ps				
CDAD0505	500ps±50ps				
CDAD0605	600ps±50ps		200ps	1.5GHz	
CDAD0705	700ps±50ps				
CDAD0805	800ps±50ps				
CDAD0905	900ps±50ps				
CDAD1005	1.0ns±50ps				
CDAD1105	1.1ns±50ps	20ps Max	250ps	1.1GHz	2.0ΩMax
CDAD1205	1.2ns±50ps				
CDAD1305	1.3ns±50ps				
CDAD1405	1.4ns±50ps				2.5ΩMax
CDAD1505	1.5ns±50ps				
CDAD1605	1.6ns±50ps		300ps	800MHz	
CDAD1705	1.7ns±50ps				3.0Ω Max
CDAD1805	1.8ns±50ps				
CDAD1905	1.9ns±50ps				
CDAD2005	2.0ns±50ps				

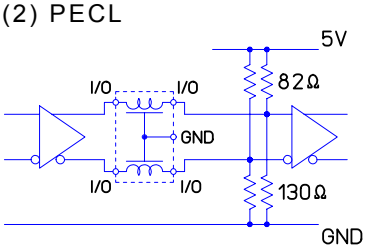
CDAD Surface-Mount High-Speed Differential Delay Lines

TYPICAL APPLICATIONS AND TERMINATION METHODS

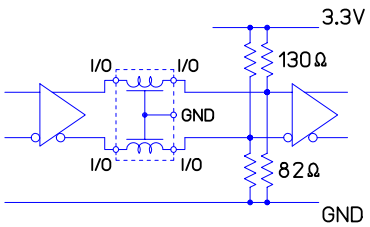
(1) ECL
(-2V termination line used)



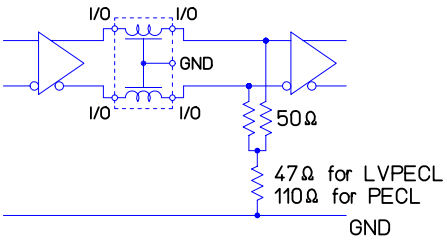
(2) PECL



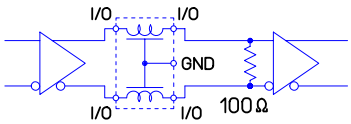
(3) ECL LVPECL



(4) Twisted Pair Termination

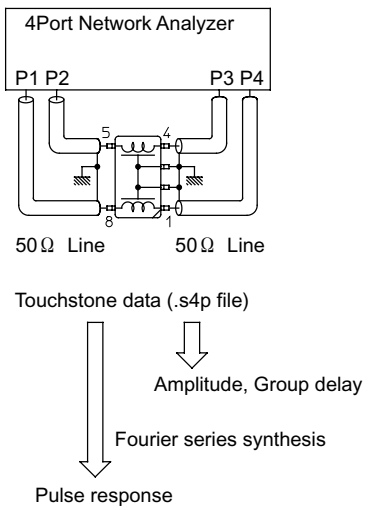


(5) LVDS



Note: The Delay Line can be used with the GND disconnected, however, in order to obtain superior performance, we recommend that all GND pins should be connected.

MEASUREMENT CONDITIONS FOR WAVEFORM PLOT

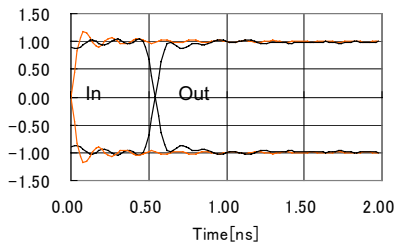


CDAD Surface-Mount High-Speed Differential Delay Lines

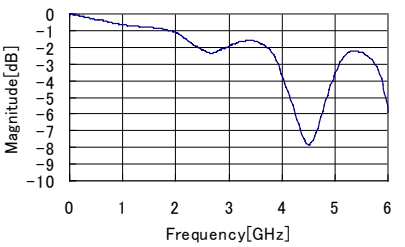
OUTPUT WAVEFORMS (1)

(1) CDAD0505

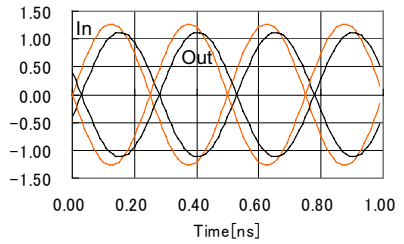
Output waveform (Step function)



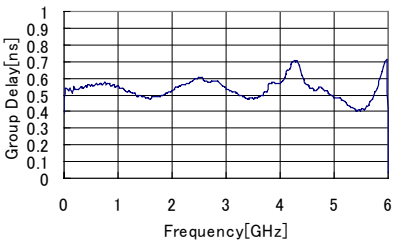
Sdd21 Amplitude / Frequency



Output waveform (2GHz Clock)

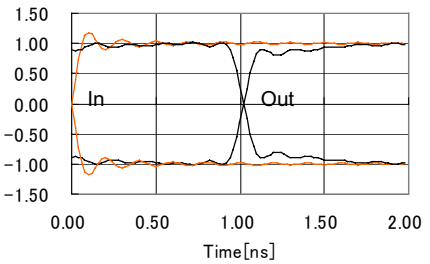


Group Delay

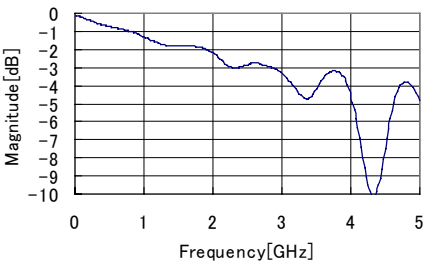


(2) CDAD1005

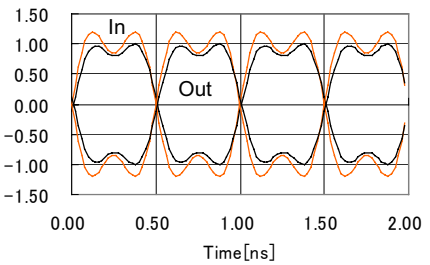
Output waveform (Step function)



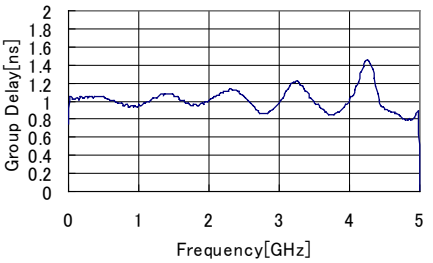
Sdd21 Amplitude / Frequency



Output waveform (1GHz Clock)



Group Delay

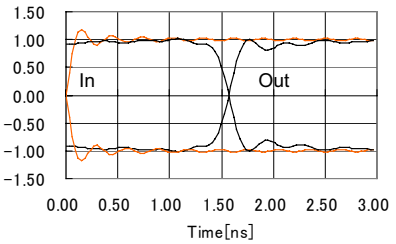


CDAD Surface-Mount High-Speed Differential Delay Lines

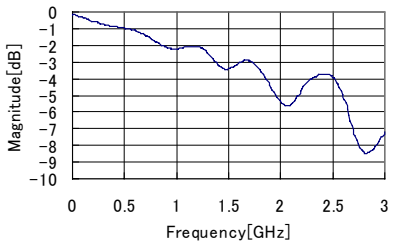
OUTPUT WAVEFORMS (2)

(3) CDAD1505

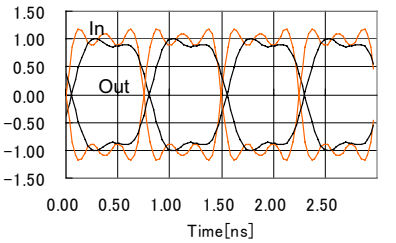
Output waveform (Step function)



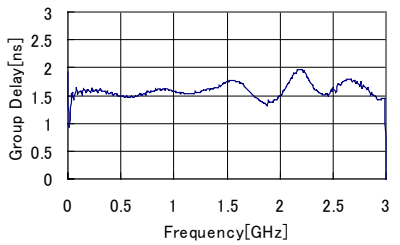
Sdd21 Amplitude / Frequency



Output waveform (667MHz Clock)

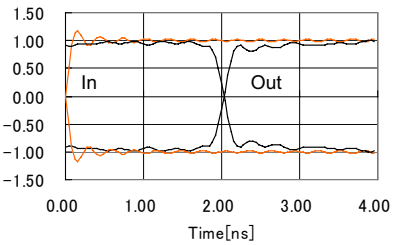


Group Delay

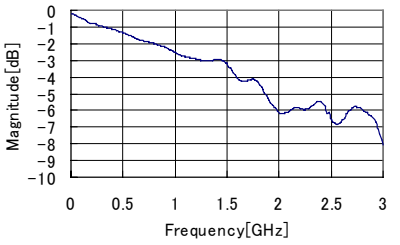


(4) CDAD2005

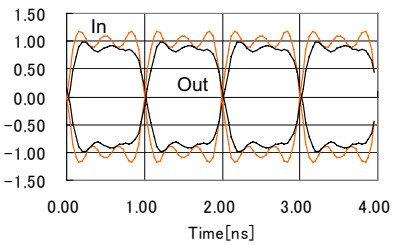
Output waveform (Step function)



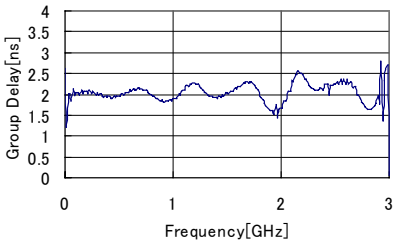
Sdd21 Amplitude / Frequency



Output waveform (500MHz Clock)



Group Delay



CDAD Surface-Mount High-Speed Differential Delay Lines

RoHS Compliance Status

1. Compliance Status

RoHS-compliant components are available. However, if RoHS-compliant components are not specified at the time of order, non-compliant stock items may be supplied until depleted.

2. Differentiating Compliant and Non-compliant Components

Compliant and Non-compliant Components will be differentiated by Lot Numbers.

Non-compliant Components: 2-digit year/month code

Compliant Components: S+2-digit year/month code (3-digit code)

3. Terminal Plating

Non-compliant Components: Base: 99% Ni/1% B, 1.2~1.6μm

External: 60% Sn/40% Pb, over 5μm

Compliant Components: Base: 100% Ni, 0.2~0.5μm

External: 100% Sn, 5~10μm