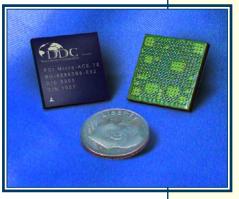
# Micro-ACE TE and PCI Micro-ACE TE

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vice Corporation

MODEL: BU-6484XB / 6486XB / 6584XB / 6586XB

This **Preliminary Product Brief** provides detailed functional capabilities for product currently in prototype production. These specifications are being provided to allow for electrical design, layout and operation.



.8 X .8 inches, 1 mm Ball Grid Array

## **FEATURES**

- World's smallest 1553 terminal
- Fully Compatible with Enhanced Mini-ACE Software and Architecture
- Available with PCI or Generic Processor Interface
- Extended Industrial Temperature Range: -40°C to +100°C
- Thermally Enhanced (TE) BGA package
- Options for 3.3 volt only, 5.0 volt only or mixed voltage operation
- 324 ball 1.0 mm pitch Ball Grid Array 0.64 in<sup>2</sup> Footprint

- 0.120" Max Height
- Fully Integrated 1553A/B Notice 2, 1760
- Highly Autonomous BC Architecture
- Built-In Controller with 20-Instruction Set
- Flexible RT Buffering
- Selective Message Monitor with Filtering
- 50% Rollover Interrupts for Stacks
   & Circular Buffers

### **DESCRIPTION**

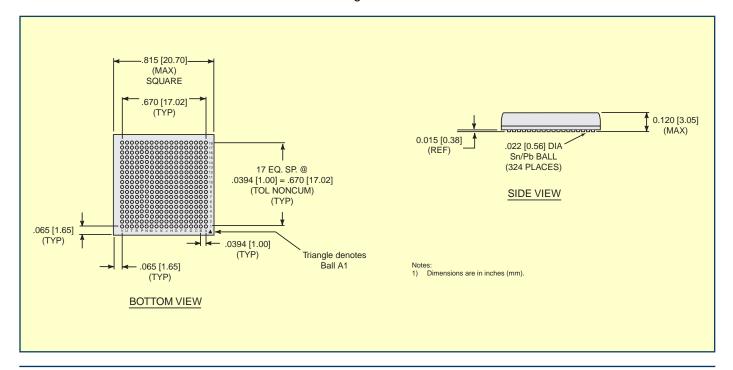
The Micro-ACE TE and PCI Micro-ACE TE are the world's smallest extended temperature range MIL-STD-1553 terminals. With a BGA package body of 0.64in², the Micro-ACE TE and PCI Micro-ACE TE are ideal for extended temperature range applications where PC board space is at a premium. The Micro-ACE TE and PCI Micro-ACE TE can be powered entirely by 3.3 volts, or they can be ordered with 5V transceivers for mixed 3.3V/5V operation.

The Micro-ACE TE and PCI Micro-ACE TE are fully software and architecturally compatible with DDC's Enhanced Mini-ACE and PCI Enhanced Mini-ACE series of devices. They integrate dual transceivers, protocol engine and up to 64K words of internal RAM. The PCI Micro-ACE TE makes it simple to connect to 32 Bit / 33 MHz PCI buses while the Micro-ACE TE's flexible generic processor interface allows direct connection with little or no glue logic to a variety of 8, 16 and 32-bit processors.

Advanced architecture is the key to the Micro-ACE TE's high performance. Advanced bus controller architecture gives the Micro-ACE TE and PCI Micro-ACE TE a high degree of flexibility and autonomy. This creates advantages in a number of areas: improving message scheduling control; minimizing host overhead for asynchronous message insertion; facilitating bulk data transfers and double buffering, message retry and bus switching strategies, and data logging and fault reporting. In addition, its remote terminal architecture provides flexibility in meeting all common MIL-STD-1553 protocols. RT data buffering and interrupt options offer robust support for synchronous and asynchronous messaging, ensure data sample consistency, and support bulk data transfers.

# μ-Ace TE BGA Outline Drawing

Figure 1



# World's Smallest Extended Industrial Temperature range MIL-STD-1553 Terminal

- Single 3.3V supply required for 3.3V transceiver versions
- 5 Volt-Tolerant Logic Signals (PCI signals are NOT 5V tolerant)
- Multiple thermal balls allow direct heat-sinking to PCB
- 3.3V transceivers have SLEEPIN input to reduce transceiver power further

#### Most Autonomous BC Architecture

- Built-in Message Control Engine
- Defined Set of 20 Instructions
- Control/Status Block for Individual Messages
- Minor and Major Frame Scheduling
- Asynchronous Message Insertion
- Conditional Branching and Subroutines
- General Purpose Queue: Message Status, Time Tag, Immediate Data, Indirect Data
- Fully User-definable Interrupts
- Legacy mode for compatability with ACE/Mini-ACE applications

#### **Remote Terminal Flexibility**

- Multiprotocol: Mil-STD-1553A/B, STANAG-3838
- Choice of Subaddress Single Message, Double Buffering\* or Circular Buffering; or Global Circular Buffering
- 50% and 100% Circular Buffer Rollover Interrupts
- Hardware or Software Programmable RT Address
- Programmable Command Illegalization
- Programmable Busy by Subaddress
- Interrupts on All Messages, or Individual Subaddresses and/or Mode codes

#### Remote terminal Flexibility - continued

- 32-entry Interrupt Status Queue
- Ball-strappable for RT AUTO-BOOT (MIL-STD-1760 Applications): Initialize to RT Mode with Busy bit SET Following Power-UP

#### **True Message Monitor**

- Selective Message Monitor Filter Based on RT Address, T/R bit, Subaddress
- Command and Data Stacks
- 50% and 100% Rollover Interrupts
- 32-Entry Interrupt Status Queue

#### **Processor Bus or PCI Interface Flexibility**

- Direct Interface to 8,16 or 32-bit Microprocessor or Microcontrollers
- Support for DMA Interface to External RAM\*
- PCI Micro-ACE TE has 33 MHz, 32-bit PCI target interface
- Supports 3.3V Logic Interface

#### **Extensive User Configurability**

- All devices can be used with external transceivers
- Software programmable divider to enable master 1553 clock of 10, 12, 16 or 20  $\rm MHz$
- RTBoot mode allows ball-selectable master 1553 clock divider

#### **Hardware Evaluation Tool**

- DDC Part# BU-64863B8-600: Daisy chain mechanical samples, with onboard die and ball pairs internally wired, for environmental (mechanical / thermal) integrity testing
- \* Not available for PCI Micro-ACE TE

All Micro-ACE TE devices are RT/MT/BC capable, and operate over the -40 to +100°C Extended Industrial Temperature Range. The selection matrix information below identifies the differences between the eight available Micro-ACE TE devices.

Part Number	Back End Interface	Logic voltage(Note 1)	Memory	RAM Voltage	Transceiver Voltage
BU-64840B3-E02	Generic Processor	3.3 V or 5V	4K X 16	Same as Logic	5.0V
BU-64843B8-E02		3.3 V	4K X 16	3.3V	3.3V
BU-64860B3-E02		3.3 V or 5V	64K x 17	5.0V	5.0V
BU-64863B8-E02		3.3 V	64K x 17	3.3V	3.3V
BU-65843B3-E02	PCI Target	3.3 V	4K X 16	3.3V	5.0V
BU-65843B8-E02		3.3V	4K x 16	3.3V	3.3V
BU-65864B3-E02		3.3V	64K x 17	5.0V	5.0V
BU-65863B8-E02		3.3V	64K x 17	3.3V	3.3V

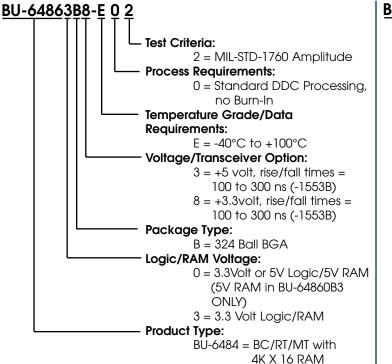
NOTE 1: All Non-PCI inputs are 5V tolerant when logic voltage is 3.3V

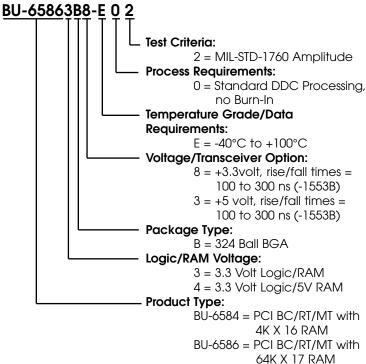
Specifications													
PARAMETER	MIN	TYP	MAX	UNITS	PARAMETER	MIN	TYP	MAX	UNITS				
POWER SUPPLY REQUIREMENTS Voltages/Tolerance +3.3V +5V (Transceiver, for BU-6XXXXB3-E02) +5V (RAM for BU-65864B3, BU-64860B3) CURRENT DRAIN BU-64843B8-E02, BU-65843B8-E02	3.15 4.75 4.5	3.3 5.0 5.0	3.45 5.25 5.5	V V V	POWER DISSIPATION Continued BU-64840B3-E02, BU-65843B3-E02 (3.3V logic, 5V transceiver, add .1W for BU-64860B3-E02,BU-65864B3-E02) Note 2 and 4 ldle 25% Duty Transmitter Cycle 50% Duty Transmitter Cycle			0.63 0.86 1.09	W W W				
(Note 1) (add 15 mA for BU-64863B8-E02, BU-65863B8-E02) +3.3V Idle w/ transceiver SLEEPIN asserted			54	mA	100% Duty Transmitter Cycle  CLOCK INPUTS PCI Clock Input: Frequency (BU-658XXB3, BU-658XXB8 only)			1.56	W				
Idle w/ transceiver SLEEPIN negated 25% Duty Transmitter Cycle 50% Duty Transmitter Cycle 100% Duty Transmitter Cycle			95 315 535 975	mA mA mA	Nominal Value 1553 Clock Input: Frequency Default is 16 MHz (Programmable fo 10, 12, 16 or 20 MHz)	or	10, 12, 16 or 2	33	MHz MHz				
BU-64840B3-E02, BU-65843B3-E02 (add 20 mA to +5V for BU-64860B3-E02, 65864B3-E02) Note 4 +5V (Ch. A, Ch. B) Idle 25% Duty Transmitter Cycle 50% Duty Transmitter Cycle 100% Duty Transmitter Cycle +3.3V (Logic)	1		100 216 332 565 40	mA mA mA mA	THERMAL Thermal Resistance, Junction-to-Ball, Hottest Die (OJB,) Note 3 324 Ball BGA Operating Thermal Balls Temperature Operating Junction Temperature Storage Temperature Lead Temperature (soldering, 10 sec.)	-40 -40 -65		15 +100 +150 +150 +300	°C/W °C °C °C °C				
POWER DISSIPATION (1553 Bus dissipation subtracted) BU-64843B8-E02, BU-65843B8-E02 (3.3V transceiver, Note 1 and 2) (add .05W for BU-BU-64863B8-E02, BU-65863B8-E02) Idle w/transceiver SLEEPIN asserted Idle w/transceiver SLEEPIN negated 25% Duty Transmitter Cycle 50% Duty Transmitter Cycle 100% Duty Transmitter Cycle			0.18 0.31 0.71 1.08 1.83	W W W W	PHYSICAL CHARACTERISTICS Package Body Size 324 ball BGA Weight	0.800 X 0.800 x 0.120 Typical 0.815 X 0.815 X 0.120 Max (ir (20.7 x 20.7 x 3.05) Max (mm 0.088 (2.5) oz (g)		lax (in.)					

#### Notes:

- 1. Current drain and power dissipation specs are based upon a small sampling of 3.3V transceivers and are subject to change.
- 2. Power dissipation is the input power minus the power delivered to the 1553 fault isolation resistors, the power delivered to the bus termination resistors and the copper losses in the transceiver isolation transformer and the bus coupling transformer.
- 3. The thermal resistance numbers indicated are preliminary.
- 4. See Micro-ACE TE Data Sheet for current drain and power dissipation numbers for 5V only operation

# Ordering Information





#### **Available Micro-ACE TE Devices:**

**BU-64840B3** = BC/RT/MT, 4K RAM X 16 RAM, 3 or 5V logic,

5V transceiver NOTE 1

**BU-64860B3** = BC/RT/MT, 64K RAM X 17 RAM, 3 or 5V logic,

5V RAM, 5V transceiver

**BU-64843B8** = BC/RT/MT, 4K RAM X 16 RAM, 3.3V logic,

3.3V transceiver NOTE 1

**BU-64863B8** = BC/RT/MT, 64K RAM X 17 RAM, 3.3V logic

and RAM, 3.3V transceiver

NOTE 1: See Application Note 37 for operating these devices in Simple System RT mode

#### **Available PCI Micro-ACE TE Devices:**

**BU-65843B3** = BC/RT/MT, 4K RAM X 16 RAM, 3.3V Logic

and RAM, 5V transceiver

**BU-65864B3** = BC/RT/MT, 64K RAM X 17 RAM, 3.3V Logic and

5V RAM, 5V transceiver

**BU-65843B8** = BC/RT/MT, 4K RAM X 16 RAM, 3.3V Logic

and RAM, 3.3V transceiver

**BU-65863B8** = BC/RT/MT, 64K RAM X 17 RAM, 3.3V logic

and RAM, 3.3V transceiver

**ORDERING INFORMATION for Daisy Chain Mechanical Sample BU-64863B8-600:** Micro-ACE TE 324 Ball BGA Daisy Chain Mechanical Sample, ball pairs internally wired, fully populated with silicon die

The information in this product brief is believed to be accurate; however, no responsibility is assumed by Data Device Corporation for its use, and no license or rights are granted by implication or otherwise in connection therewith. Specifications are subject to change without notice.





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BU-6486 = BC/RT/MT with

64K X 17 RAM

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