CYPRESS SEMICONDUCTOR

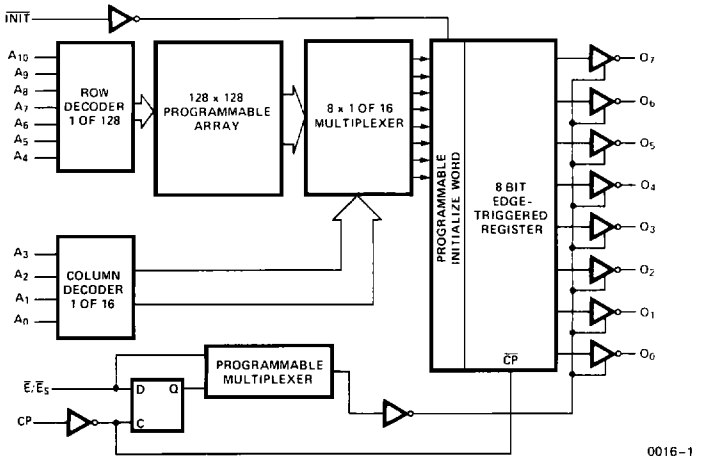
CY7C245

Reprogrammable 2048 x 8 Registered PROM

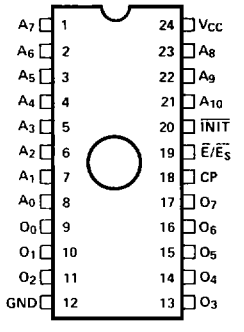
Features

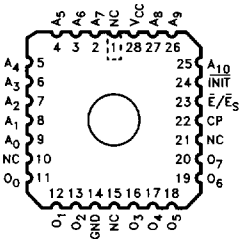
- Windowed for reprogrammability
- CMOS for optimum speed/power
- High speed
  - — 25 ns max set-up
  - — 12 ns clock to output
- Low power
  - — 330 mW (commercial) for −35 ns, −45 ns
  - — 660 mW (military)
- Programmable synchronous or asynchronous output enable
- On-chip edge-triggered registers
- Programmable asynchronous register ($\overline{INIT}$)
- EPROM technology, 100% programmable
- Slim, 300 mil, 24 pin plastic or hermetic DIP
- 5V ±10% V_{CC}, commercial and military
- TTL compatible I/O
- Direct replacement for bipolar PROMs
- Capable of withstanding greater than 2000V static discharge

Logic Block Diagram



Pin Configurations





Selection Guide

			7C245-25	7C245-35	7C245-45
Maximum Setup Time (ns)			25	35	45
Maximum Clock to Output (ns)			12	15	25
Maximum Operating Current (mA)	STD	Commercial	90	90	90
		Military		120	120
	L	Commercial		60	60

Product Characteristics

The CY7C245 is a high performance 2048 word by 8 bit electrically Programmable Read Only Memory packaged in a slim 300 mil plastic or hermetic DIP. The ceramic package may be equipped with an erasure window; when exposed to UV light the PROM is erased and can then be reprogrammed. The memory cells utilize proven EPROM floating gate technology and byte-wide intelligent programming algorithms.

The CY7C245 replaces bipolar devices and offers the advantages of lower power, reprogrammability, superior performance and high programming yield. The EPROM cell requires only 13.5V for the supervoltage and low current requirements allow for gang programming. The EPROM cells allow for each memory location to be tested 100%, as each location is written into, erased, and repeatedly exercized prior to encapsulation. Each PROM is also tested for AC performance to guarantee that after customer programming the product will meet AC specification limits.

The CY7C245 has an asynchronous initialize function ($\overline{INIT}$). This function acts as a 2049th 8-bit word loaded into the on-chip register. It is user programmable with any desired word or may be used as a PRESET or CLEAR function on the outputs.

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... −65°C to +150°C

Ambient Temperature with Power Applied ..... −55°C to +125°C

Supply Voltage to Ground Potential (Pin 24 to Pin 12) ..... −0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State ..... −0.5V to +7.0V

DC Input Voltage ..... −3.0V to +7.0V

DC Program Voltage (Pins 7, 18, 20) 13.0V

UV Erasure ..... 7258 Wsec/cm^2

Static Discharge Voltage ..... >2001V (Per MIL-STD-883 Method 3015)

Latchup Current ..... >200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ±10%
Military[7]	−55°C to +125°C	5V ±10%

Electrical Characteristics Over Operating Range[6]

Parameters	Description	Test Conditions		7C245L-35, 45		7C245-25		7C245-35, 45		Units
				Min.	Max.	Min.	Max.	Min.	Max.	
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = −4.0 mA, V_{IN} = V_{IH} or V_{IL}		2.4		2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 16 mA, V_{IN} = V_{IH} or V_{IL}			0.4		0.4		0.4	V
V_{IH}	Input HIGH Level	Guaranteed Input Logical HIGH Voltage for All Inputs[1]		2.0	V_{CC}	2.0	V_{CC}	2.0	V_{CC}	V
V_{IL}	Input LOW Level	Guaranteed Input Logical LOW Voltage for All Inputs[1]			0.8		0.8		0.8	V
I_{IX}	Input Leakage Current	GND ≤ V_{IN} ≤ V_{CC}		−10	+10	−10	+10	−10	+10	μA
V_{CD}	Input Clamp Diode Voltage	Note 5		Note 5						
I_{OZ}	Output Leakage Current	GND ≤ V_O ≤ V_{CC} Output Disabled[3]		−40	+40	−40	+40	−40	+40	μA
I_{OS}	Output Short Circuit Current	V_{CC} = Max., V_{OUT} = 0.0V[2]		−20	−90	−20	−90	−20	−90	mA
I_{CC}	Power Supply Current	GND ≤ V_{IN} ≤ V_{CC}, V_{CC} = Max.	Commercial		60		90		90	mA
			Military						120	

Capacitance[4]

Parameters	Description	Test Conditions	Max.	Units
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	5	pF
C_{OUT}	Output Capacitance		8	

Notes:

1. These are absolute voltages with respect to device ground pin and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment (see Notes on Testing).
2. For test purposes, not more than one output at a time should be shorted. Short circuit test duration should not exceed 30 seconds.
3. For devices using the synchronous enable, the device must be clocked after applying these voltages to perform this measurement.
4. Tested initially and after any design or process changes that may affect these parameters.
5. The CMOS process does not provide a clamp diode. However, the CY7C245 is insensitive to −3V dc input levels and −5V undershoot pulses of less than 10 ns (measured at 50% point).
6. See the last page of this specification for Group A subgroup testing information.
7. T_A is the "instant on" case temperature.

Switching Characteristics Over Operating Range[8]

Parameters	Description	7C245-25		7C245-35		7C245-45		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{SA}	Address Setup to Clock HIGH	25		35		45		ns
t_{HA}	Address Hold from Clock HIGH	0		0		0		ns
t_{CO}	Clock HIGH to Valid Output		12		15		25	ns
t_{PWC}	Clock Pulse Width	15		20		20		ns
t_{SES}	$\overline{E}_S$ Setup to Clock HIGH	12		15		15		ns
t_{HES}	$\overline{E}_S$ Hold from Clock HIGH	5		5		5		ns
t_{DI}	Delay from $\overline{INIT}$ to Valid Output		20		20		35	ns
t_{RI}	$\overline{INIT}$ Recovery to Clock HIGH	15		20		20		ns
t_{PWI}	$\overline{INIT}$ Pulse Width	15		20		25		ns
t_{COS}	Valid Output from Clock HIGH[1]		15		20		30	ns
t_{HZC}	Inactive Output from Clock HIGH[1, 3]		15		20		30	ns
t_{DOE}	Valid Output from $\overline{E}$ LOW[2]		15		20		30	ns
t_{HZE}	Inactive Output from $\overline{E}$ HIGH[2, 3]		15		20		30	ns

Notes:

1. Applies only when the synchronous ($\overline{E}_S$) function is used.
2. Applies only when the asynchronous ($\overline{E}$) function is used.
3. Transition is measured at steady state High level − 500 mV or steady state Low level + 500 mV on the output from the 1.5V level on the input with loads shown in *Figure 1b*.
4. Tests are performed with rise and fall times of 5 ns or less.
5. See *Figure 1a* for all switching characteristics except t_{HZ}.
6. See *Figure 1b* for t_{HZ}.
7. All device test loads should be located within 2" of device outputs.
8. See the last page of this specification for Group A subgroup testing information.

AC Test Loads and Waveforms[5, 6, 7]

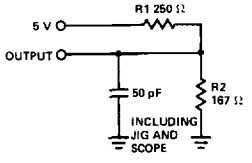


Figure 1a

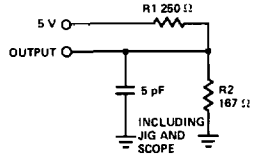


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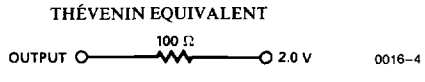
Figure 1b

Equivalent to:



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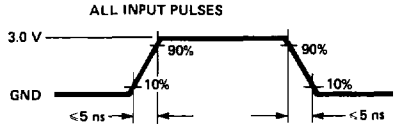

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Figure 2

Functional Description

The CY7C245 is a CMOS electrically Programmable Read Only Memory organized as 2048 words x 8-bits and is a pin-for-pin replacement for bipolar TTL fusible link PROMs. The CY7C245 incorporates a D-type, master-slave register on chip, reducing the cost and size of pipelined microprogrammed systems and applications where accessed PROM data is stored temporarily in a register. Additional flexibility is provided with a programmable synchronous ($\overline{E}_S$) or asynchronous ($\overline{E}$) output enable and asynchronous initialization ($\overline{INIT}$).

Upon power-up the state of the outputs will depend on the programmed state of the enable function ($\overline{E}_S$ or $\overline{E}$). If the synchronous enable ($\overline{E}_S$) has been programmed, the register will be in the set condition causing the outputs (O_0–O_7) to be in the OFF or high impedance state. If the asynchronous enable ($\overline{E}$) is being used, the outputs will come up in the OFF or high impedance state only if the enable ($\overline{E}$) input is at a HIGH logic level. Data is read by applying the memory location to the address inputs (A_0–A_{10}) and a logic LOW to the enable input. The stored data is accessed and loaded into the master flip-flops of the data register during the address set-up time. At the next LOW-to-HIGH transition of the clock (CP), data is transferred to the slave flip-flops, which drive the output buffers, and the accessed data will appear at the outputs (O_0–O_7).

If the asynchronous enable ($\overline{E}$) is being used, the outputs may be disabled at any time by switching the enable to a

Functional Description (Continued)

logic HIGH, and may be returned to the active state by switching the enable to a logic LOW.

If the synchronous enable ($\overline{E_S}$) is being used, the outputs will go to the OFF or high impedance state upon the next positive clock edge after the synchronous enable input is switched to a HIGH level. If the synchronous enable pin is switched to a logic LOW, the subsequent positive clock edge will return the output to the active state. Following a positive clock edge, the address and synchronous enable inputs are free to change since no change in the output will occur until the next low to high transition of the clock. This unique feature allows the CY7C245 decoders and sense amplifiers to access the next location while previously addressed data remains stable on the outputs.

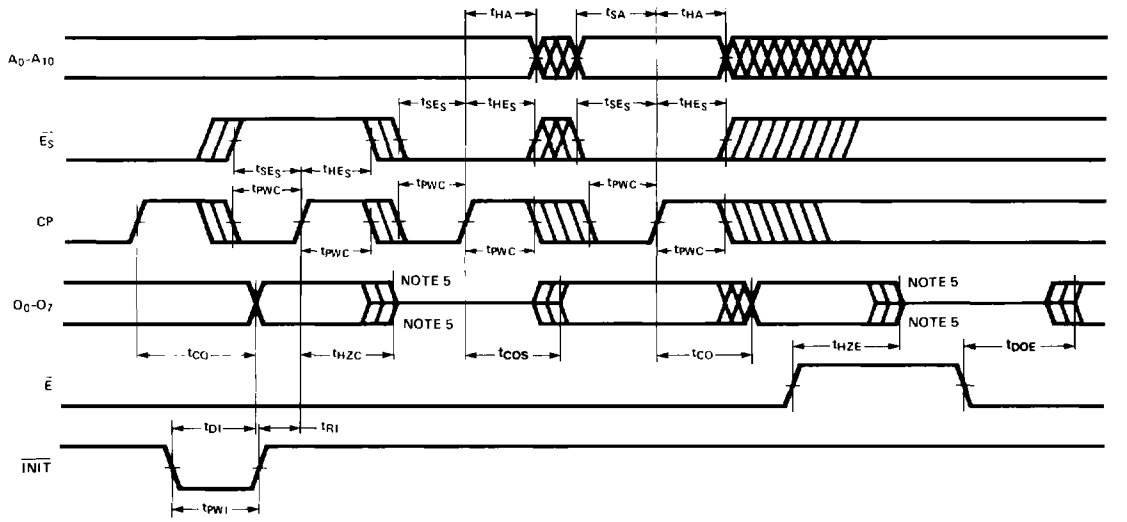
System timing is simplified in that the on-chip edge triggered register allows the PROM clock to be derived directly from the system clock without introducing race conditions. The on-chip register timing requirements are similar to those of discrete registers available in the market.

The CY7C245 has an asynchronous initialize input ($\overline{INIT}$). The initialize function is useful during power-up and time-out sequences and can facilitate implementation of other sophisticated functions such as a built-in "jump start" address. When activated the initialize control input causes the contents of a user programmed 2049th 8-bit word to be loaded into the on-chip register. Each bit is programmable and the initialize function can be used to load any desired combination of "1"s and "0"s into the register. In the unprogrammed state, activating $\overline{INIT}$ will generate a register CLEAR (all outputs LOW). If all the bits of the initialize word are programmed, activating $\overline{INIT}$ performs a register PRESET (all outputs HIGH).

Applying a LOW to the $\overline{INIT}$ input causes an immediate load of the programmed initialize word into the master and slave flip-flops of the register, independent of all other inputs, including the clock (CP). The initialize data will appear at the device outputs after the outputs are enabled by bringing the asynchronous enable ($\overline{E}$) LOW.

3

Switching Waveforms



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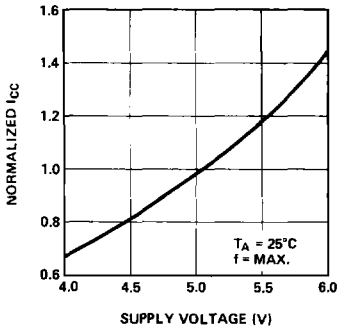
Notes on Testing

Incoming test procedures on these devices should be carefully planned, taking into account the high performance and output drive capabilities of the parts. The following notes may be useful.

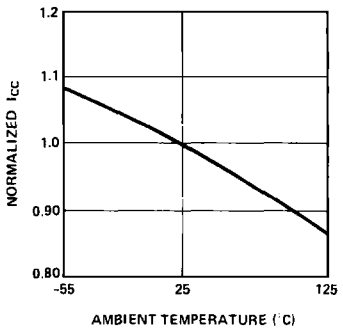
1. Ensure that adequate decoupling capacitance is employed across the device V_{CC} and ground terminals. Multiple capacitors are recommended, including a 0.1 μF or larger capacitor and a 0.01 μF or smaller capacitor placed as close to the device terminals as possible. Inadequate decoupling may result in large variations of power supply voltage, creating erroneous function or transient performance failures.
2. Do not leave any inputs disconnected (floating) during any tests.
3. Do not attempt to perform threshold tests under AC conditions. Large amplitude, fast ground current transients normally occur as the device outputs discharge the load capacitances. These transients flowing through the parasitic inductance between the device ground pin and the test system ground can create significant reductions in observable input noise immunity.
4. Output levels are measured at 1.5V reference levels.
5. Transition is measured at steady state HIGH level −500 mV or steady state LOW level +500 mV on the output from the 1.5V level on inputs with load shown in *Figure 1b*.

Typical DC and AC Characteristics

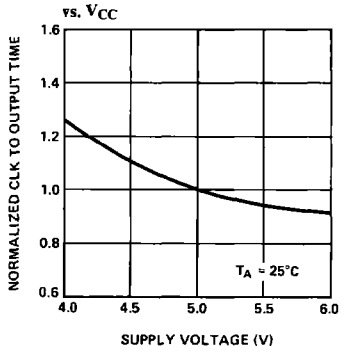
NORMALIZED SUPPLY CURRENT vs. SUPPLY VOLTAGE



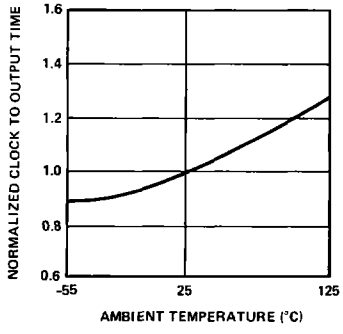
NORMALIZED SUPPLY CURRENT vs. AMBIENT TEMPERATURE



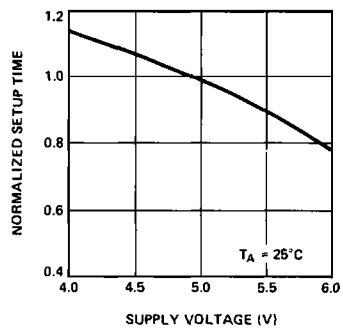
CLOCK TO OUTPUT TIME vs. V_{CC}



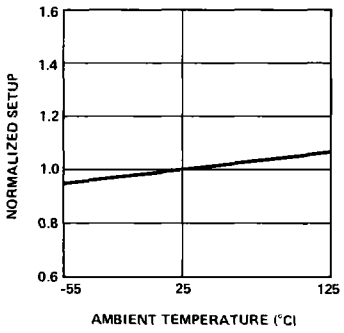
CLOCK TO OUTPUT TIME vs. TEMPERATURE



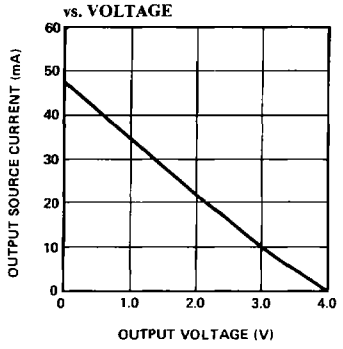
NORMALIZED SETUP TIME vs. SUPPLY VOLTAGE



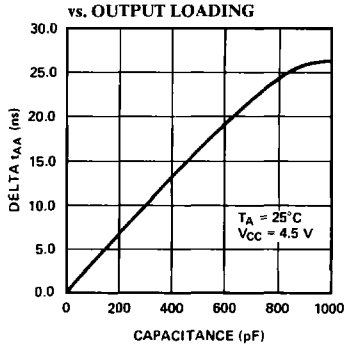
NORMALIZED SETUP TIME vs. TEMPERATURE



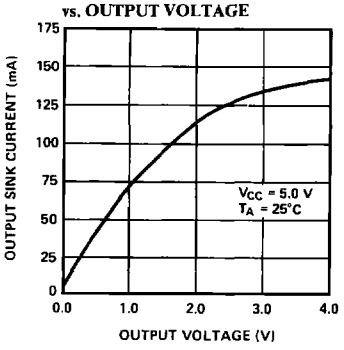
OUTPUT SOURCE CURRENT vs. VOLTAGE



TYPICAL ACCESS TIME CHANGE vs. OUTPUT LOADING



OUTPUT SINK CURRENT vs. OUTPUT VOLTAGE



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Erasure Characteristics

Wavelengths of light less than 4000 Angstroms begin to erase the 7C245. For this reason, an opaque label should be placed over the window if the PROM is exposed to sunlight or fluorescent lighting for extended periods of time.

The recommended dose for erasure is ultraviolet light with a wavelength of 2537 Angstroms for a minimum dose (UV intensity × exposure time) of 25 Wsec/cm^2. For an ultraviolet lamp with a 12 mW/cm^2 power rating the exposure time would be approximately 30–35 minutes. The 7C245 needs to be within 1 inch of the lamp during erasure. Permanent damage may result if the PROM is exposed to high intensity UV light for an extended period of time. 7258 Wsec/cm^2 is the recommended maximum dosage.

Device Programming

OVERVIEW:

There are three independent programmable functions contained in the 7C245 CMOS 2K x 8 Registered PROM; the 2K x 8 array, the initial byte, and the synchronous enable bit. All of the programming elements are "EPROM" cells, and are in an erased state when the device is shipped. This erased state manifests itself differently in each case. The erased state for ENABLE bit is the "ASYNCHRONOUS ENABLE" mode. The erased state for the "INITIAL BYTE" is all "0's" or "LOW". The "INITIAL BYTE" may be accessed operationally thru the use of the initialize function. The 2K x 8 array uses a differential memory cell, with differential sensing techniques. In the erased state the cell contains neither a one nor a zero. The erased state of this array may be verified by using the "BLANK CHECK ONES" and "BLANK CHECK ZEROS" function, see Table 3.

3

DC Programming Parameters T_A = 25°C

Table 1

Parameter	Description	Min.	Max.	Units
V_{PP}[1]	Programming Voltage	12.0	13.0	V
V_{CCP}	Supply Voltage	4.75	5.25	V
V_{IHP}	Input High Voltage	3.0		V
V_{ILP}	Input Low Voltage		0.4	V
V_{OH}[2]	Output High Voltage	2.4		V
V_{OL}[2]	Output Low Voltage		0.4	V
I_{PP}	Programming Supply Current		50	mA

AC Programming Parameters T_A = 25°C

Table 2

Parameter	Description	Min.	Max.	Units
t_{PP}	Programming Pulse Width	100	10,000	μs
t_{AS}	Address Setup Time	1.0		μs
t_{DS}	Data Setup Time	1.0		μs
t_{AH}	Address Hold Time	1.0		μs
t_{DH}	Data Hold Time	1.0		μs
t_R, t_F[3]	V_{PP} Rise and Fall Time	1.0		μs
t_{VD}	Delay to Verify	1.0		μs
t_{VP}	Verify Pulse Width	2.0		μs
t_{DV}	Verify Data Valid		1.0	μs
t_{DZ}	Verify HIGH to High Z		1.0	μs

Notes:

1. V_{CCP} must be applied prior to V_{PP}.
2. During verify operation.
3. Measured 10% and 90% points.

Mode Selection

Table 3

Mode		Pin Function					Outputs (9–11, 13–17)
	Read or Output Disable	A_2	CP	$\overline{E}/\overline{E}_S$	$\overline{INIT}$	A_1	
	Other	A_2	$\overline{PGM}$	$\overline{VFY}$	V_{PP}	A_1	
	Pin	(6)	(18)	(19)	20	(7)	
Read[2,3]		X	X	V_{IL}	V_{IH}	X	Data Out
Output Disable[5]		X	X	V_{IH}	V_{IH}	X	High Z
Program[1,4]		X	V_{ILP}	V_{IHP}	V_{PP}	X	Data In
Program Verify[1,4]		X	V_{IHP}	V_{ILP}	V_{PP}	X	Data Out
Program Inhibit[1,4]		X	V_{IHP}	V_{IHP}	V_{PP}	X	High Z
Intelligent Program[1,4]		X	V_{ILP}	V_{IHP}	V_{PP}	X	Data In
Program Synch Enable[4]		V_{IHP}	V_{ILP}	V_{IHP}	V_{PP}	V_{PP}	High Z
Program Initial Byte[4]		V_{ILP}	V_{ILP}	V_{IHP}	V_{PP}	V_{PP}	Data In
Blank Check Ones[1,4]		X	V_{PP}	V_{ILP}	V_{ILP}	X	Ones
Blank Check Zeros[1,4]		X	V_{PP}	V_{IHP}	V_{ILP}	X	Zeros

Notes:

1. X = Don't care but not to exceed V_{PP}.
2. During read operation, the output latches are loaded on a "0" to "1" transition of CP.
3. If the registered device is being operated in a synchronous mode, pin 19 must be LOW prior to the "0" to "1" transition on CP (18) that loads the register.
4. During programming and verification, all unspecified pins to be at V_{ILP}.
5. If the registered device is being operated in a synchronous mode, pin 19 must be HIGH prior to the "0" to "1" transition on CP (18) that loads the register.

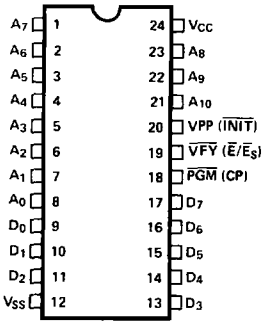

Figure 3. Programming Pinouts

The CY7C245 programming algorithm allows significantly faster programming than the "worst case" specification of 10 msec.

Typical programming time for a byte is less than 2.5 msec. The use of EPROM cells allows factory testing of programmed cells, measurement of data retention and erasure to ensure reliable data retention and functional performance. A flowchart of the algorithm is shown in *Figure 4.*

The algorithm utilizes two different pulse types: initial and overprogram. The duration of the $\overline{PGM}$ pulse (t_{PP}) is 0.1 msec which will then be followed by a longer overprogram pulse of 24 (0.1) (X) msec. X is an iteration counter and is equal to the NUMBER of the initial 0.1 msec pulses applied before verification occurs. Up to four 0.1 msec pulses are provided before the overprogram pulse is applied.

The entire sequence of program pulses and byte verifications is performed at V_{CCP} = 5.0V. When all bytes have been programmed all bytes should be compared (Read mode) to original data with V_{CC} = 5.0V.

Bit Map Data

Programmer	Address	RAM Data
Decimal	Hex	Contents
0	0	DATA
•	•	•
•	•	•
•	•	•
2047	7FF	DATA
2048	800	INIT BYTE
2049	801	CONTROL BYTE

Control Byte

00 Asynchronous output enable (default state)
01 Synchronous output enable

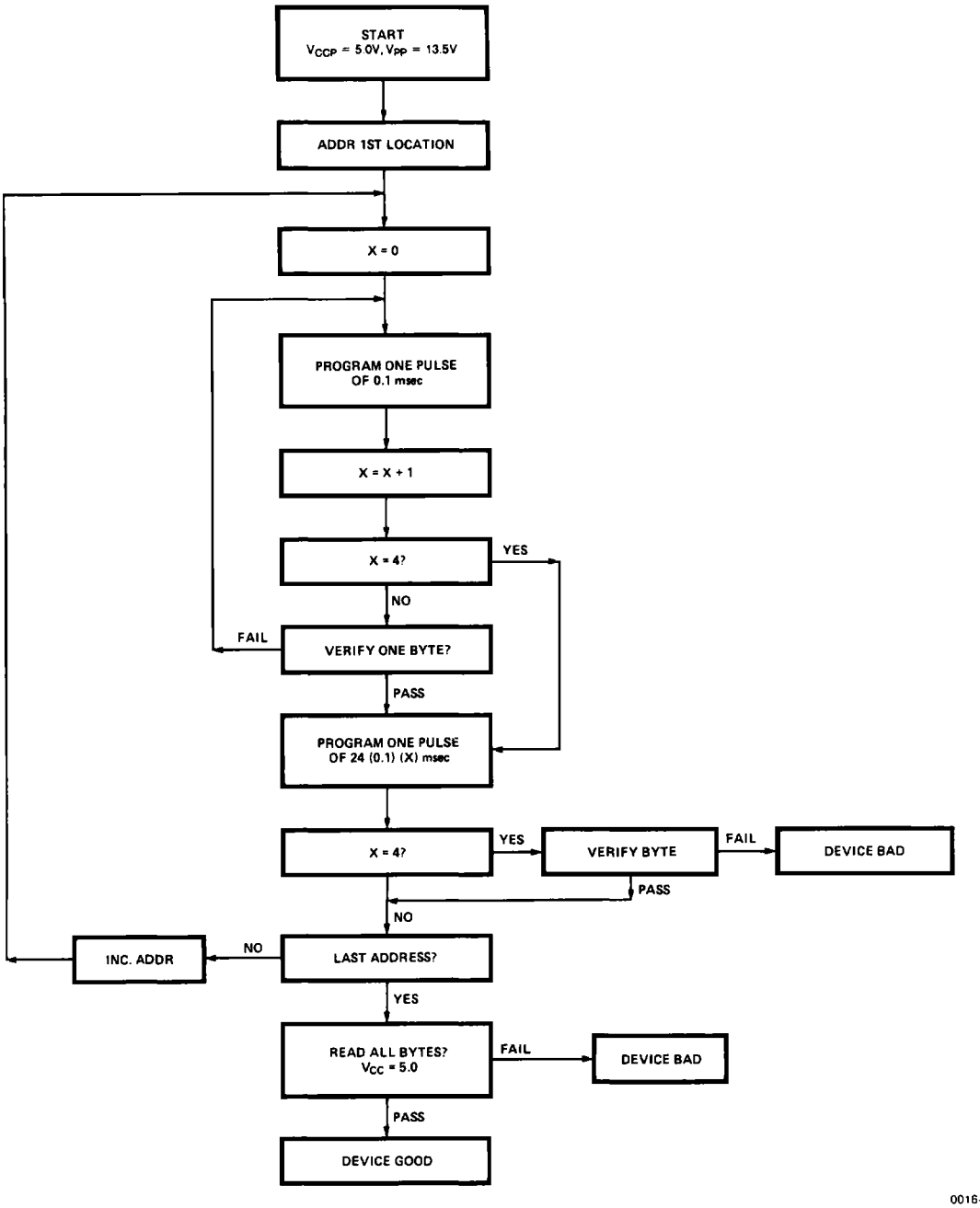

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Figure 4. Programming Flowchart

Programming Sequence 2K x 8 Array

Power the device for normal read mode operation with pin 18, 19 and 20 at V_{IH}. Per *Figure 5* take pin 20 to V_{PP}. The device is now in the program inhibit mode of operation with the output lines in a high impedance state; see *Figures 5* and *6*. Again per *Figure 5* address program and verify one byte of data. Repeat this for each location to be programmed.

If the brute force programming method is used, the pulse width of the program pulse should be 10 ms, and each location is programmed with a single pulse. Any location that fails to verify causes the device to be rejected.

If the intelligent programming technique is used, the program pulse width should be 100 μs. Each location is ultimately programmed and verified until it verifies correctly up to and including 4 times. When the location verifies, one additional programming pulse should be applied of duration 24X the sum of the previous programming pulses before advancing to the next address to repeat the process.

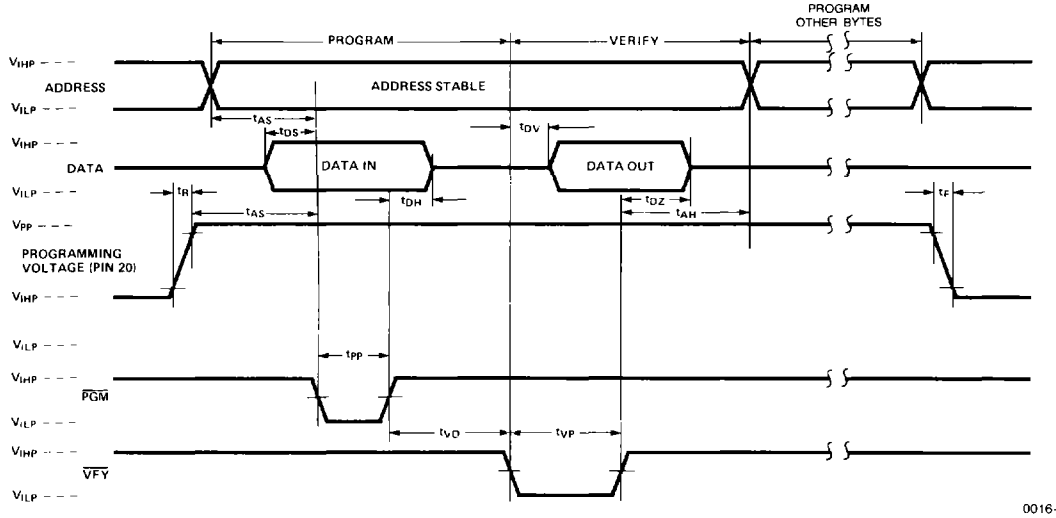

Figure 5. PROM Programming Waveforms

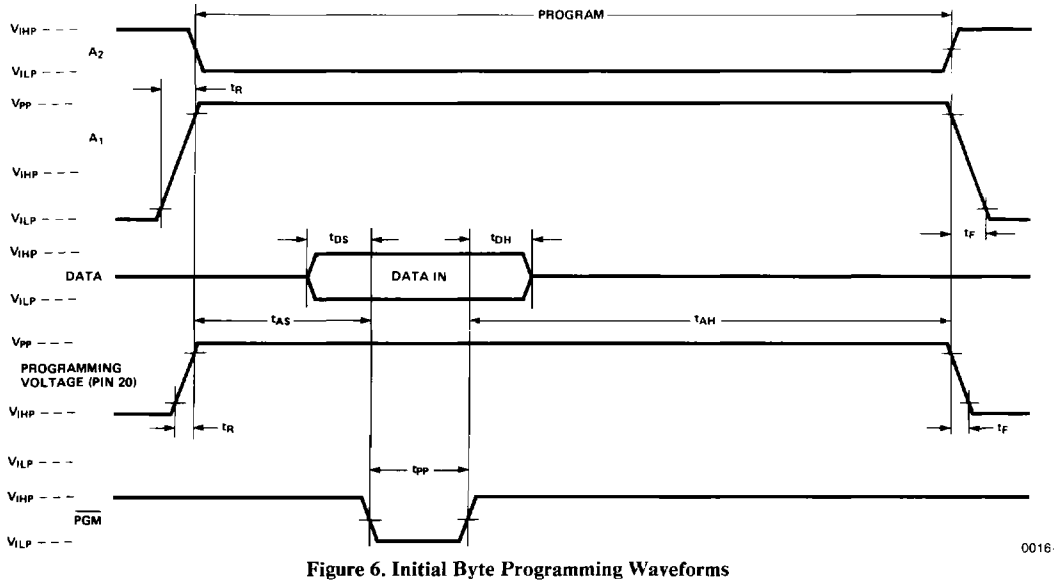

Figure 6. Initial Byte Programming Waveforms

Programming the Initialization Byte

The CY7C245 registered PROM has a 2049th byte of data used to initialize the value of the register. This initial byte is value "0" when the part is received. If the user desires to have a value other than "0" for register initialization, this must be programmed into the 2049th byte. This byte is programmed in a similar manner to the 2048 normal bytes in the array except for two considerations. First, since all of the normal addresses of the part are used up, a super voltage will be used to create additional effective addresses. The actual address has V_{PP} on A_1 pin 7, and V_{ILP} on A_2, pin 6, per Table 3. The programming and verification of "INITIAL BYTE" is accomplished operationally by performing an initialize function.

Programming Synchronous Enable

The CY7C245 provides for both a synchronous and asynchronous enable function. The device is delivered in an asynchronous mode of operation and only requires that the user alter the device if synchronous operation is required. The determination of the option is accomplished thru the use of an EPROM cell which is programmed only if synchronous operation is required. As with the INITIAL byte, this function is addressed thru the use of a supervoltage. Per Table 3, V_{PP} is applied to pin 7 (A_1) with pin 6 (A_2) at V_{IHP}. This addresses the cell that programs synchronous enable. Programming the cell is accomplished with a 10 ms program pulse on pin 18 ($\overline{PGM}$) but does not require any data as there is no choice as to how synchronous enable may be programmed, only if it is to be programmed.

3

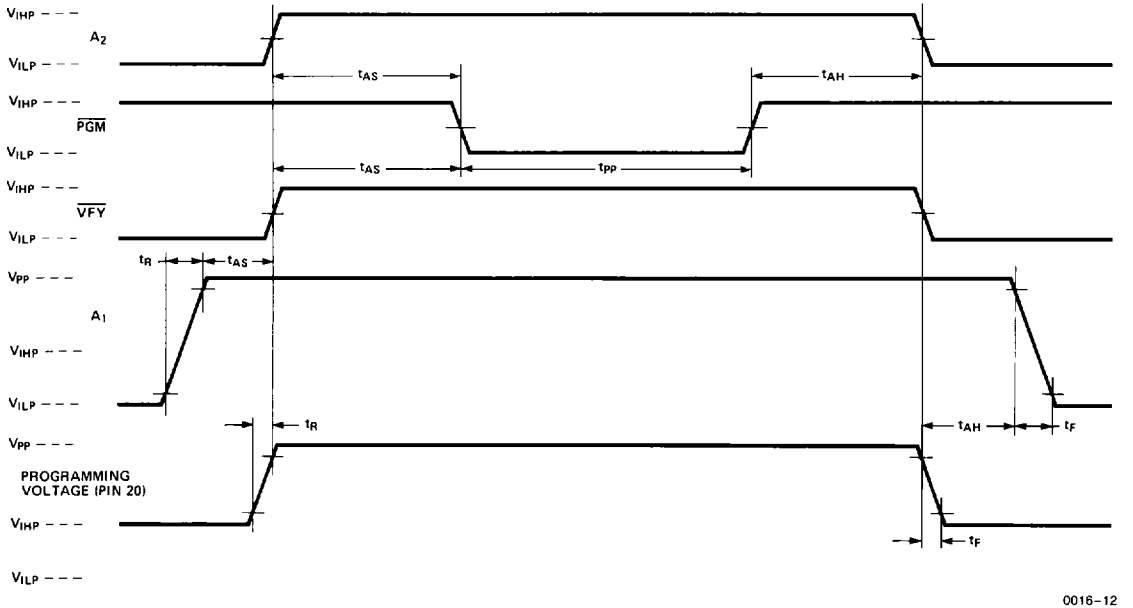

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Figure 7. Program Synchronous Enable

Verification of Synchronous Enable

Verification of the synchronous enable function is accomplished operationally. Power the device for read operation with pin 20 at V_{IH}, cause clock pin 18 to transition from V_{IL} to V_{IH}. The output should be in a High Z state. Take pin 20, $\overline{ENABLE}$, to V_{IL}. The outputs should remain in a high Z state. Transition the clock from V_{IL} to V_{IH}, the outputs should now contain the data that is present. Again set pin 19 to V_{IH}. The output should remain driven. Clocking pin 18 once more from V_{IL} to V_{IH} should place the outputs again in a High Z state.

Blank Check

A virgin device contains neither one's nor zero's because of the differential cell used for high speed. To verify that a PROM is unprogrammed, use the two blank check modes provided in Table 3. In both of these modes, address and read locations 0 thru 2047. A device is considered virgin if all locations are respectively "1's" and "0's" when addressed in the "BLANK ONES AND ZEROS" modes.

Because a virgin device contains neither ones nor zeros, it is necessary to program both one's and zero's. It is recommended that all locations be programmed to ensure that ambiguous states do not exist.

Ordering Information

Speed (ns)		I_{CC} mA	Ordering Code	Package Type	Operating Range
t_{SA}	t_{CO}				
25	12	90	CY7C245-25PC	P13	Commercial
			CY7C245-25WC	W14	
35	15	60	CY7C245L-35PC	P13	Commercial
			CY7C245L-35WC	W14	
		90	CY7C245-35PC	P13	
			CY7C245-35SC	S13	
			CY7C245-35WC	W14	
			CY7C245-35LC	L64	
		120	CY7C245-35DMB	D14	Military
			CY7C245-35QMB	Q64	
			CY7C245-35WMB	W14	
			CY7C245-35LMB	L64	

Speed (ns)		I_{CC} mA	Ordering Code	Package Type	Operating Range
t_{SA}	t_{CO}				
45	25	60	CY7C245L-45PC	P13	Commercial
			CY7C245L-45WC	W14	
		90	CY7C245-45PC	P13	
			CY7C245-45SC	S13	
			CY7C245-45WC	W14	
			CY7C245-45LC	L64	
		120	CY7C245-45WMB	W14	Military
			CY7C245-45LMB	L64	
			CY7C245-45DMB	D14	
			CY7C245-45QMB	Q64	

MILITARY SPECIFICATIONS
Group A Subgroup Testing

DC Characteristics

Parameters	Subgroups
V_{OH}	1,2,3
V_{OL}	1,2,3
V_{IH}	1,2,3
V_{IL}	1,2,3
I_{IX}	1,2,3
I_{OZ}	1,2,3
I_{CC}	1,2,3

Switching Characteristics

Parameters	Subgroups
t_{SA}	7,8,9,10,11
t_{HA}	7,8,9,10,11
t_{CO}	7,8,9,10,11

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