512K x 36/1M x 18 Flow-Thru SRAM with NoBL™ Architecture

Features

- **Pin-compatible and functionally equivalent to ZBT™ devices**
- **Supports 117-MHz bus operations with zero wait states**
  - **Data is transferred on every clock**
- **Internally self-timed output buffer control to eliminate the need to use asynchronous OE**
- **Registered inputs for flow-thru operation**
- **Byte Write capability**
- **Common I/O architecture**
- **Fast clock-to-output times**
  - **7.5 ns (for 117-MHz device)**
  - **8.5 ns (for 100-MHz device)**
  - **10.0ns (for 83-MHz device)**
- **Single 3.3V –5% and +10% power supply V_{DD}**
- **Separate V_{DDQ} for 3.3V or 2.5V I/O**
- **Clock enable (CEN) pin to suspend operation**
- **Synchronous self-timed writes**
- **Available in 100 TQFP and 119 BGA packages**
- **Burst capability – linear or interleaved burst order**
- **JTAG boundary scan for BGA packaging version**
- **Automatic power down available using ZZ mode or CE deselect**

Functional Description

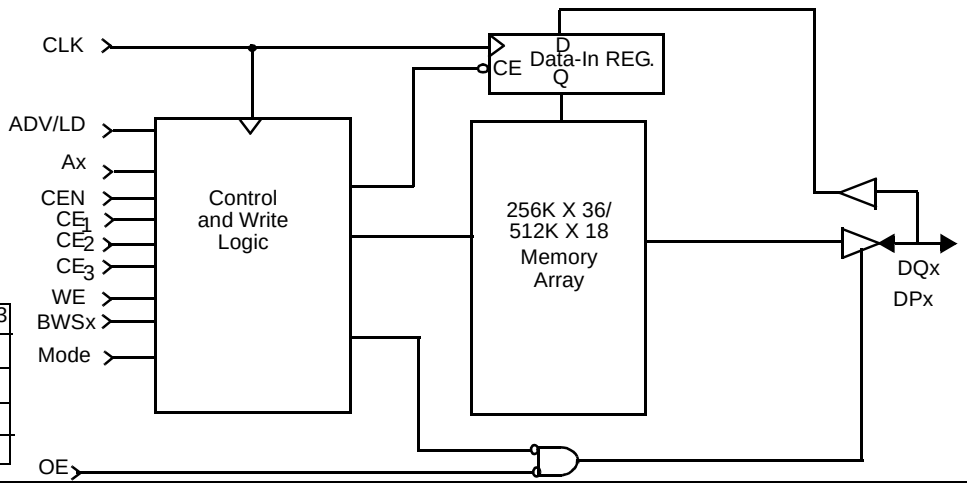
The CY7C1371B/CY7C1373B is 3.3V, 512K x 36 and 1M x 18 synchronous flow-thru burst SRAMs, respectively designed to support unlimited true back-to-back Read/Write operations without the insertion of wait states. The CY7C1371B/CY7C1373B is equipped with the advanced No Bus Latency™ (NoBL™) logic required to enable consecutive Read/Write operations with data being transferred on every clock cycle. This feature dramatically improves the throughput of data through the SRAM, especially in systems that require frequent Write/Read transitions.The CY7C1371B/CY7C1373B is pin compatible and functionally equivalent to ZBT devices.

All synchronous inputs pass through input registers controlled by the rising edge of the clock.The clock input is qualified by the Clock enable ($\overline{CEN}$) signal, which when deasserted suspends operation and extends the previous clock cycle. Maximum access delay from the clock rise is 7.5 ns (117-MHz device).

Write operations are controlled by the byte Write Selects ($\overline{BWS}_{a,b,c,d}$ for CY7C1371B and $\overline{BWS}_{a,b}$ for CY7C1373B) and a Write enable ($\overline{WE}$) input. All writes are conducted with on-chip synchronous self-timed Write circuitry. ZZ may be tied to LOW if it is not used.

Synchronous Chip enables ($\overline{CE}_1$, CE_2, $\overline{CE}_3$ on the TQFP, $\overline{CE}_1$ on the BGA) and an asynchronous Output enable ($\overline{OE}$) provide for easy bank selection and output three-state control. In order to avoid bus contention, the output drivers are synchronously three-stated during the data portion of a Write sequence.

Logic Block Diagram



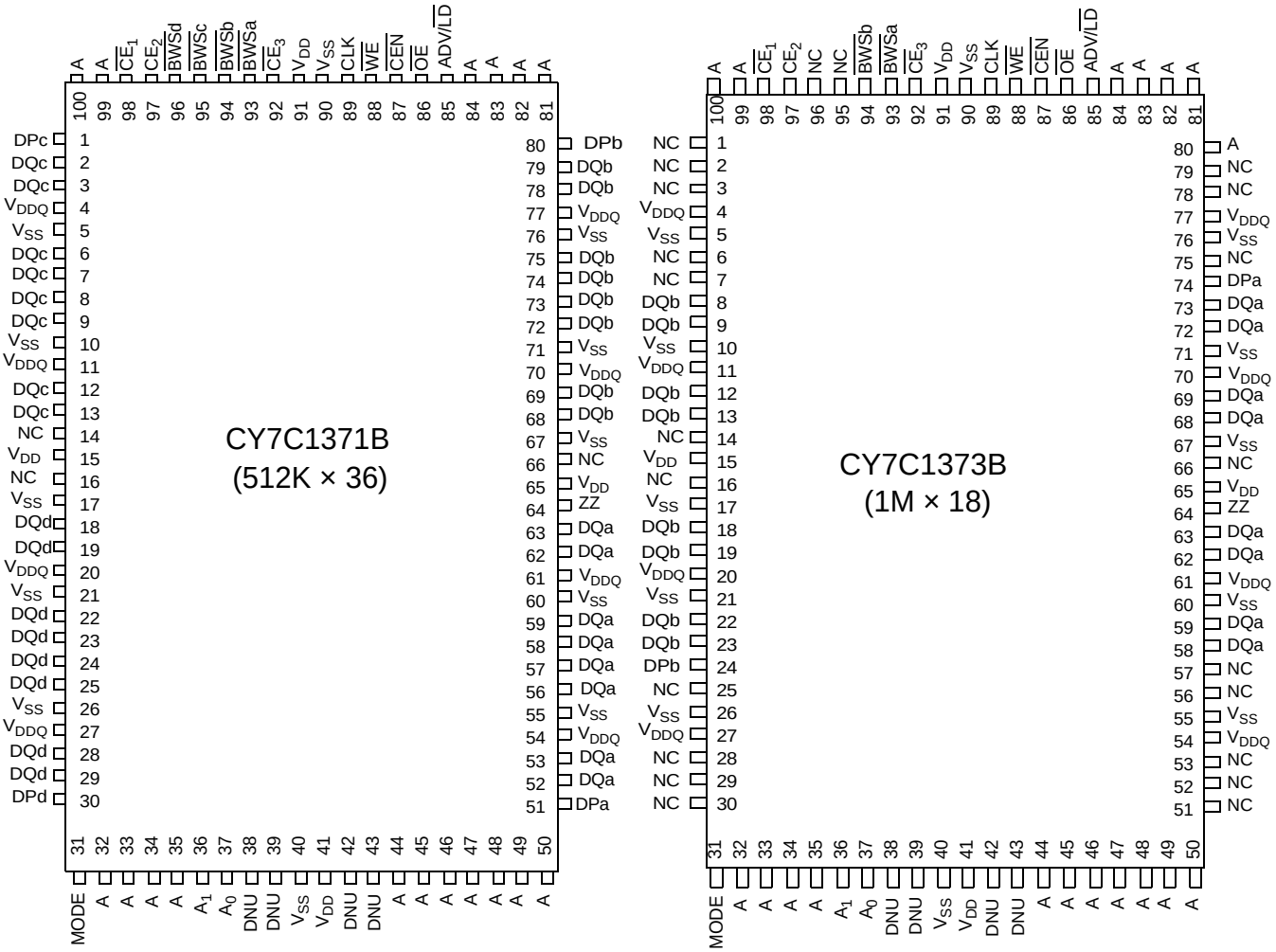
	CY7C1371	CY7C1373
AX	X = 18:0	X = 19:0
DQX	X= a, b, c, d	X = a, b
DPX	X = a, b, c, d	X = a, b
BWSX	X = a, b, c, d	X = a, b

Selection Guide

	117 MHz	100 MHz	83 MHz	Unit
Maximum Access Time	7.5	8.5	10.0	ns
Maximum Operating Current	250	225	185	mA
Maximum CMOS Standby Current	20	20	20	mA

Pin Configurations

100-pin TQFP Packages



Pin Configurations (continued)

119-ball BGA

CY7C1371B (512K × 36) – 7 × 17 BGA

	1	2	3	4	5	6	7
A	V_{DDQ}	A	A	A	A	A	V_{DDQ}
B	NC	CE_2	A	ADV/$\overline{LD}$	A	$\overline{CE_3}$	NC
C	NC	A	A	V_{DD}	A	A	NC
D	DQc	DPc	V_{SS}	NC	V_{SS}	DPb	DQb
E	DQc	DQc	V_{SS}	$\overline{CE1}$	V_{SS}	DQb	DQb
F	V_{DDQ}	DQc	V_{SS}	$\overline{OE}$	V_{SS}	DQb	V_{DDQ}
G	DQc	DQc	$\overline{BWSc}$	A	$\overline{BWSb}$	DQb	DQb
H	DQc	DQc	V_{SS}	$\overline{WE}$	V_{SS}	DQb	DQb
J	V_{DDQ}	V_{DD}	NC	V_{DD}	NC	V_{DD}	V_{DDQ}
K	DQd	DQd	V_{SS}	CLK	V_{SS}	DQa	DQa
L	DQd	DQd	$\overline{BWSd}$	NC	$\overline{BWSa}$	DQa	DQa
M	V_{DDQ}	DQd	V_{SS}	$\overline{CEN}$	V_{SS}	DQa	V_{DDQ}
N	DQd	DQd	V_{SS}	A1	V_{SS}	DQa	DQa
P	DQd	DPd	V_{SS}	A0	V_{SS}	DPa	DQa
R	NC	A	MODE	V_{DD}	NC	A	NC
T	NC	64M	A	A	A	32M	ZZ
U	V_{DDQ}	TMS	TDI	TCK	TDO	NC	V_{DDQ}

CY7C1373B (1M × 18) – 7 × 17 BGA

	1	2	3	4	5	6	7
A	V_{DDQ}	A	A	A	A	A	V_{DDQ}
B	NC	CE_2	A	ADV/$\overline{LD}$	A	$\overline{CE_3}$	NC
C	NC	A	A	V_{DD}	A	A	NC
D	DQb	NC	V_{SS}	NC	V_{SS}	DPa	NC
E	NC	DQb	V_{SS}	$\overline{CE1}$	V_{SS}	NC	DQa
F	V_{DDQ}	NC	V_{SS}	$\overline{OE}$	V_{SS}	DQa	V_{DDQ}
G	NC	DQb	$\overline{BWSb}$	A	V_{SS}	NC	DQa
H	DQb	NC	V_{SS}	$\overline{WE}$	V_{SS}	DQa	NC
J	V_{DDQ}	V_{DD}	NC	V_{DD}	NC	V_{DD}	V_{DDQ}
K	NC	DQb	V_{SS}	CLK	V_{SS}	NC	DQa
L	DQb	NC	V_{SS}	NC	$\overline{BWSa}$	DQa	NC
M	V_{DDQ}	DQb	V_{SS}	$\overline{CEN}$	V_{SS}	NC	V_{DDQ}
N	DQb	NC	V_{SS}	A1	V_{SS}	DQa	NC
P	NC	DPb	V_{SS}	A0	V_{SS}	NC	DQa
R	NC	A	MODE	V_{DD}	NC	A	NC
T	64M	A	A	32M	A	A	ZZ
U	V_{DDQ}	TMS	TDI	TCK	TDO	NC	V_{DDQ}

Pin Configurations (continued)

165-ball Bump FBGA

CY7C1371B (512K × 36) – 11 × 15 FBGA

	1	2	3	4	5	6	7	8	9	10	11
A	NC	A	$\overline{CE}_1$	$\overline{BWS}$c	$\overline{BWS}$b	$\overline{CE}_3$	$\overline{CEN}$	ADV/$\overline{LD}$	A	A	NC
B	NC	A	CE_2	$\overline{BWS}$d	$\overline{BWS}$a	CLK	$\overline{WE}$	$\overline{OE}$	A	A	128M
C	DPc	NC	V_{DDQ}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{DDQ}	NC	DPb
D	DQc	DQc	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQb	DQb
E	DQc	DQc	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQb	DQb
F	DQc	DQc	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQb	DQb
G	DQc	DQc	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQb	DQb
H	NC	V_{DD}	NC	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	NC	NC	ZZ
J	DQd	DQd	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQa	DQa
K	DQd	DQd	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQa	DQa
L	DQd	DQd	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQa	DQa
M	DQd	DQd	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQa	DQa
N	DPd	NC	V_{DDQ}	V_{SS}	NC	NC	NC	V_{SS}	V_{DDQ}	NC	DPa
P	NC	64M	A	A	TDI	A1	TDO	A	A	A	NC
R	MODE	32M	A	A	TMS	A0	TCK	A	A	A	A

CY7C1373B (1M × 18) – 11 × 15 FBGA

	1	2	3	4	5	6	7	8	9	10	11
A	NC	A	$\overline{CE}_1$	$\overline{BWS}$b	NC	$\overline{CE}_3$	$\overline{CEN}$	ADV/$\overline{LD}$	A	A	A
B	NC	A	CE_2	NC	$\overline{BWS}$a	CLK	$\overline{WE}$	$\overline{OE}$	A	A	128M
C	NC	NC	V_{DDQ}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{DDQ}	NC	DPa
D	NC	DQb	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	NC	DQa
E	NC	DQb	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	NC	DQa
F	NC	DQb	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	NC	DQa
G	NC	DQb	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	NC	DQa
H	NC	V_{DD}	NC	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	NC	NC	ZZ
J	DQb	NC	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQa	NC
K	DQb	NC	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQa	NC
L	DQb	NC	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQa	NC
M	DQb	NC	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQa	NC
N	DPb	NC	V_{DDQ}	V_{SS}	NC	NC	NC	V_{SS}	V_{DDQ}	NC	NC
P	NC	64M	A	A	TDI	A1	TDO	A	A	A	NC
R	MODE	32M	A	A	TMS	A0	TCK	A	A	A	A

Pin Definitions

Name	I/O Type	Description
A0 A1 A	Input-Synchronous	**Address inputs used to select one of the 532,288/1,048,576 address locations**. Sampled at the rising edge of the CLK.
$\overline{BWS}$a BWSb BWSc BWSd	Input-Synchronous	**Byte Write Select inputs, active LOW**. Qualified with $\overline{WE}$ to conduct Writes to the SRAM. Sampled on the rising edge of CLK. $\overline{BWS}$a controls DQa and DPa, $\overline{BWS}$b controls DQb and DPb, $\overline{BWS}$c controls DQc and DPc, $\overline{BWS}$d controls DQd and DPd.
$\overline{WE}$	Input-Synchronous	**Write enable input, active LOW**. Sampled on the rising edge of CLK if $\overline{CEN}$ is active LOW. This signal must be asserted LOW to initiate a Write sequence.
ADV/$\overline{LD}$	Input-Synchronous	Advance/Load input used to advance the on-chip address counter or load a new address. When HIGH (and $\overline{CEN}$ is asserted LOW) the internal burst counter is advanced. When LOW, a new address can be loaded into the device for an access. After being deselected, ADV/$\overline{LD}$ should be driven LOW in order to load a new address.
CLK	Input-Clock	**Clock input**. Used to capture all synchronous inputs to the device. CLK is qualified with $\overline{CEN}$. CLK is only recognized if $\overline{CEN}$ is active LOW.
$\overline{CE}_1$	Input-Synchronous	**Chip enable 1 input, active LOW**. Sampled on the rising edge of CLK. Used in conjunction with CE_2 and $\overline{CE}_3$ to select/deselect the device.
CE_2	Input-Synchronous	**Chip enable 2 input, active HIGH**. Sampled on the rising edge of CLK. Used in conjunction with $\overline{CE}_1$ and $\overline{CE}_3$ to select/deselect the device.
$\overline{CE}_3$	Input-Synchronous	**Chip enable 3 input, active LOW**. Sampled on the rising edge of CLK. Used in conjunction with $\overline{CE}_1$ and CE_2 to select/deselect the device.
$\overline{OE}$	Input-Asynchronous	**Output enable, active LOW**. Combined with the synchronous logic block inside the device to control the direction of the I/O pins. When LOW, the I/O pins are allowed to behave as outputs. When deasserted HIGH, I/O pins are three-stated, and act as input data pins. $\overline{OE}$ is masked during the data portion of a Write sequence, during the first clock when emerging from a deselected state and when the device has been deselected.
$\overline{CEN}$	Input-Synchronous	**Clock enable input, active LOW**. When asserted LOW the clock signal is recognized by the SRAM. When deasserted HIGH the clock signal is masked. Since deasserting $\overline{CEN}$ does not deselect the device, $\overline{CEN}$ can be used to extend the previous cycle when required.
DQa DQb DQc DQd	I/O-Synchronous	**Bidirectional Data I/O lines**. As inputs, they feed into an on-chip data register that is triggered by the rising edge of CLK. As outputs, they deliver the data contained in the memory location specified by $A_{[x]}$ during the previous clock rise of the Read cycle. The direction of the pins is controlled by $\overline{OE}$ and the internal control logic. When $\overline{OE}$ is asserted LOW, the pins can behave as outputs. When HIGH, DQa – DQd are placed in a three-state condition. The outputs are automatically three-stated during the data portion of a Write sequence, during the first clock when emerging from a deselected state, and when the device is deselected, regardless of the state of $\overline{OE}$. DQ a, b, c and d are eight-bits wide.
DPa DPb DPc DPd	I/O-Synchronous	**Bidirectional Data Parity I/O lines**. Functionally, these signals are identical to $DQ_{[31:0]}$. During Write sequences, DPa is controlled by $\overline{BWS}$a, DPb is controlled by $\overline{BWS}$b, DPc is controlled by $\overline{BWS}$c, and DPd is controlled by $\overline{BWS}$d. DP a, b, c and d are one-bit wide.
ZZ	Input-Asynchronous	**ZZ "sleep" input**. This active HIGH input places the device in a non-time critical "sleep" condition with data integrity preserved.
MODE	Input Pin	**Mode input**. Selects the burst order of the device. Tied HIGH selects the interleaved burst order. Pulled LOW selects the linear burst order. MODE should not change states during operation. When left floating MODE will default HIGH, to an interleaved burst order.
V_{DD}	Power Supply	Power supply inputs to the core of the device.
V_{DDQ}	I/O Power Supply	Power supply for the I/O circuitry.
V_{SS}	Ground	**Ground for the device**. Should be connected to ground of the system.
TDO	JTAG serial output Synchronous	**Serial data-out to the JTAG circuit**. Delivers data on the negative edge of TCK (BGA only).
TDI	JTAG serial input Synchronous	**Serial data-In to the JTAG circuit**. Sampled on the rising edge of TCK (BGA only).

Pin Definitions

Name	I/O Type	Description
TMS	Test Mode Select Synchronous	**This pin controls the Test Access Port (TAP) state machine**. Sampled on the rising edge of TCK (BGA only)
TCK	JTAG serial clock	Serial clock to the JTAG circuit (BGA only)
32M 64M 128M	–	**No connects**. Reserved for address expansion. Pins are not internally connected.
NC	–	**No connects**. Pins are not internally connected.
DNU	–	Do not use pins.

Functional Overview

The CY7C1371B/CY7C1373B is a synchronous flow-thru burst NoBL SRAM specifically designed to eliminate wait states during Write–Read transitions. All synchronous inputs pass through input registers controlled by the rising edge of the clock. The clock signal is qualified with the clock enable input signal ($\overline{CEN}$). If $\overline{CEN}$ is HIGH, the clock signal is not recognized and all internal states are maintained. All synchronous operations are qualified with $\overline{CEN}$. Maximum access delay from the clock rise (t_{CDV}) is 7.5 ns (117-MHz device).

Accesses can be initiated by asserting chip enable(s) ($\overline{CE_1}$, CE_2, $\overline{CE_3}$ on the TQFP, $\overline{CE_1}$ on the BGA) active at the rising edge of the clock. If the clock enable ($\overline{CEN}$) is active LOW and ADV/$\overline{LD}$ is asserted LOW, the address presented to the device will be latched. The access can be either a Read or Write operation, depending on the status of the Write enable ($\overline{WE}$). Byte Write Selects can be used to conduct byte Write operations.

Write operations are qualified by the $\overline{WE}$. All Writes are simplified with on-chip, synchronous, self-timed Write circuitry.

A synchronous chip enable ($\overline{CE_1}$, CE_2, and $\overline{CE_3}$ on the TQFP, CE_1 on the BGA) and an asynchronous $\overline{OE}$ simplify depth expansion. All operations (Reads, Writes, and Deselects) are pipelined. ADV/$\overline{LD}$ should be driven LOW once the device has been deselected in order to load a new address for the next operation.

Single Read Access

A Read access is initiated when the following conditions are satisfied at clock rise: (1) $\overline{CEN}$ is asserted LOW, (2) $\overline{CE_1}$, CE_2, and $\overline{CE_3}$ are ALL asserted active, (3) $\overline{WE}$ is deasserted HIGH, and 4) ADV/$\overline{LD}$ is asserted LOW. The address presented to the address inputs is latched into the Address register and presented to the memory core and control logic. The control logic determines that a Read access is in progress and allows the requested data to propagate to the output buffers. The data is available within 6.5 ns (133-MHz device) provided $\overline{OE}$ is active LOW. After the first clock of the Read access the output buffers are controlled by $\overline{OE}$ and the internal control logic. $\overline{OE}$ must be driven LOW in order for the device to drive out the requested data. On the subsequent clock, another operation (Read/Write/Deselect) can be initiated. When the SRAM is deselected at clock rise by one of the chip enable signals, its output will be three-stated immediately.

Burst Read Access

The CY7C1371B/CY7C1373B has an on-chip burst counter that allows the user the ability to supply a single address and conduct up to four Reads without reasserting the address inputs. ADV/$\overline{LD}$ must be driven LOW in order to load a new address into the SRAM, as described in the Single Read Access section above. The sequence of the burst counter is determined by the MODE input signal. A LOW input on MODE selects a linear burst mode, a HIGH selects an interleaved burst sequence. Both burst counters use A0 and A1 in the burst sequence, and will wrap-around when incremented sufficiently. A HIGH input on ADV/$\overline{LD}$ will increment the internal burst counter regardless of the state of chip enables inputs or $\overline{WE}$. $\overline{WE}$ is latched at the beginning of a burst cycle. Therefore, the type of access (Read or Write) is maintained throughout the burst sequence.

Single Write Access

Write access is initiated when the following conditions are satisfied at clock rise: (1) $\overline{CEN}$ is asserted LOW, (2) chip enable(s) asserted active, and (3) $\overline{WE}$ is asserted LOW. The address presented is loaded into the Address register. The Write signals are latched into the Control Logic block. The data lines are automatically three-stated regardless of the state of the $\overline{OE}$ input signal. This allows the external logic to present the data on DQ and DP.

On the next clock rise the data presented to DQ and DP (or a subset for byte Write operation) inputs is latched into the device and the Write is complete (see Write Cycle Description table for details). Additional accesses (Read/Write/Deselect) can be initiated on this cycle.

The data written during the Write operation is controlled by byte Write Select signals. The CY7C1371B/CY7C1373B provides byte Write capability that is described in the Write Cycle Description table. Asserting the $\overline{WE}$ input with the selected byte Write Select input will selectively write to only the desired bytes. Bytes not selected during a byte Write operation will remain unaltered. A synchronous self-timed Write mechanism has been provided to simplify the Write operations. Byte Write capability has been included in order to greatly simplify Read/Modify/Write sequences, which can be reduced to simple byte Write operations.

Because the CY7C1371B/CY7C1373B are common I/O devices, data should not be driven into the device while the outputs are active. The $\overline{OE}$ can be deasserted HIGH before presenting data to the DQ and DP inputs. Doing so will three-state the output drivers. As a safety precaution, DQ and

DP are automatically three-stated during the data portion of a Write cycle, regardless of the state of $\overline{OE}$.

Burst Write Access

The CY7C1371B/CY7C1373B has an on-chip burst counter that allows the user the ability to supply a single address and conduct up to four Write operations without reasserting the address inputs. ADV/$\overline{LD}$ must be driven LOW in order to load the initial address, as described in the Single Write Access section above. When ADV/$\overline{LD}$ is driven HIGH on the subsequent clock rise, the chip enables ($\overline{CE_1}$, CE_2, and $\overline{CE_3}$) and $\overline{WE}$ inputs are ignored and the burst counter is incremented. The correct $\overline{BWS_{a,b,c,d}}$/$\overline{BWS_{a,b}}$ inputs must be driven in each cycle of the burst Write in order to write the correct bytes of data.

Cycle Description Truth Table[1, 2, 3, 4, 5, 6]

Operation	Address Used	$\overline{CE}$	$\overline{CEN}$	ADV/LD	$\overline{WE}$	$\overline{BWS_X}$	CLK	Comments
Deselected	External	1	0	0	X	X	L–H	I/Os three-state following next recognized clock.
Suspend	–	X	1	X	X	X	L–H	Clock ignored, all operations suspended.
Begin Read	External	0	0	0	1	X	L–H	Address latched.
Begin Write	External	0	0	0	0	Valid	L–H	Address latched, data presented two valid clocks later.
Burst Read Operation	Internal	X	0	1	X	X	L–H	Burst Read operation. Previous access was a Read operation. Addresses incremented internally in conjunction with the state of MODE.
Burst Write Operation	Internal	X	0	1	X	Valid	L–H	Burst Write operation. Previous access was a Write operation. Addresses incremented internally in conjunction with the state of MODE. Bytes written are determined by $\overline{BWS_{a,b,c,d}}$/$\overline{BWS_{a,b}}$.

Interleaved Burst Sequence

First Address	Second Address	Third Address	Fourth Address
A[1:0]	A[1:0]	A[1:0]	A[1:0]
00	01	10	11
01	00	11	10
10	11	00	01
11	10	01	00

Linear Burst Sequence

First Address	Second Address	Third Address	Fourth Address
A[1:0]	A[1:0]	A[1:0]	A[1:0]
00	01	10	11
01	10	11	00
10	11	00	01
11	00	01	10

ZZ-Mode Electrical Characteristics

Parameter	Description	Test Conditions	Min.	Max.	Unit
I_{DDZZ}	Snooze mode standby current	$ZZ \geq V_{DD} - 0.2V$		20	mA
t_{ZZS}	Device operation to ZZ	$ZZ \geq V_{DD} - 0.2V$		$2t_{CYC}$	ns
t_{ZZREC}	ZZ recovery time	$ZZ \leq 0.2V$	$2t_{CYC}$		ns

Notes:
1. X = "Don't Care," 1 = Logic HIGH, 0 = Logic LOW, CE stands for ALL chip enables. CE = 0 stands for ALL chip enables active.
2. Write is defined by $\overline{WE}$ and $\overline{BWS_X}$. $\overline{BWS_X}$ = Valid signifies that the desired byte Write selects are asserted. See Write Cycle Description table for details.
3. The DQ and DP pins are controlled by the current cycle and the $\overline{OE}$ signal.
4. CEN = 1 inserts wait states.
5. Device will power-up deselected and I/Os in a three-state condition, regardless of $\overline{OE}$.
6. $\overline{OE}$ assumed LOW.

Sleep Mode

The ZZ input pin is an asynchronous input. Asserting ZZ places the SRAM in a power conservation “sleep” mode. Two clock cycles are required to enter into or exit from this “sleep” mode. While in this mode, data integrity is guaranteed. Accesses pending when entering the “sleep” mode are not considered valid nor is the completion of the operation guaranteed. The device must be deselected prior to entering the “sleep” mode. $\overline{CE}$s, $\overline{ADSP}$, and $\overline{ADSC}$ must remain inactive for the duration of t_{ZZREC} after the ZZ input returns LOW.

Write Cycle Descriptions[1, 2]

Function (CY7C1371B)	$\overline{WE}$	$\overline{BWSd}$	$\overline{BWSc}$	$\overline{BWSb}$	$\overline{BWSa}$
Read	1	X	X	X	X
Write ∠ No Bytes Written	0	1	1	1	1
Write Byte 0 – (DQa and DPa)	0	1	1	1	0
Write Byte 1 – (DQb and DPb)	0	1	1	0	1
Write Bytes 1, 0	0	1	1	0	0
Write Byte 2 – (DQc and DPc)	0	1	0	1	1
Write Bytes 2, 0	0	1	0	1	0
Write Bytes 2, 1	0	1	0	0	1
Write Bytes 2, 1, 0	0	1	0	0	0
Write Byte 3 – (DQb and DPd)	0	0	1	1	1
Write Bytes 3, 0	0	0	1	1	0
Write Bytes 3, 1	0	0	1	0	1
Write Bytes 3, 1, 0	0	0	1	0	0
Write Bytes 3, 2	0	0	0	1	1
Write Bytes 3, 2, 0	0	0	0	1	0
Write Bytes 3, 2, 1	0	0	0	0	1
Write All Bytes	0	0	0	0	0

Function (CY7C1373B)	$\overline{WE}$	$\overline{BWSb}$	$\overline{BWSa}$
Read	1	x	x
Write – No Bytes Written	0	1	1
Write Byte 0 – (DQa and DPa)	0	1	0
Write Byte 1 – (DQb and DPc)	0	0	1
Write Both Bytes	0	0	0

IEEE 1149.1 Serial Boundary Scan (JTAG)

The CY7C1371B/CY7C1373B incorporates a serial boundary scan Test Access Port (TAP) in the BGA package only. The TQFP package does not offer this functionality. This port operates in accordance with IEEE Standard 1149.1–1900, but does not have the set of functions required for full 1149.1 compliance. These functions from the IEEE specification are excluded because their inclusion places an added delay in the critical speed path of the SRAM. Note that the TAP controller functions in a manner that does not conflict with the operation of other devices using 1149.1 fully compliant TAPs. The TAP operates using JEDEC standard 2.5V I/O logic levels.

Disabling the JTAG Feature

It is possible to operate the SRAM without using the JTAG feature. To disable the TAP controller, TCK must be tied LOW (V_{SS}) to prevent clocking of the device. TDI and TMS are internally pulled up and may be unconnected. They may alternately be connected to V_{DD} through a pull-up resistor. TDO should be left unconnected. Upon power-up, the device will come up in a reset state which will not interfere with the operation of the device.

Test Access Port – Test Clock

The test clock is used only with the TAP controller. All inputs are captured on the rising edge of TCK. All outputs are driven from the falling edge of TCK.

Test Mode Select

The TMS input is used to give commands to the TAP controller and is sampled on the rising edge of TCK. It is allowable to leave this pin unconnected if the TAP is not used. The pin is pulled up internally, resulting in a logic HIGH level.

Test Data In (TDI)

The TDI pin is used to serially input information into the registers and can be connected to the input of any of the registers. The register between TDI and TDO is chosen by the instruction that is loaded into the TAP instruction register. For information on loading the instruction register, see the TAP Controller State Diagram. TDI is internally pulled up and can be unconnected if the TAP is unused in an application. TDI is connected to the most-significant bit (MSB) on any register.

Test Data Out (TDO)

The TDO output pin is used to serially clock data-out from the registers. The output is active depending upon the current state of the TAP state machine (See TAP Controller State diagram). The output changes on the falling edge of TCK. TDO is connected to the least-significant bit (LSB) of any register.

Performing a TAP Reset

A Reset is performed by forcing TMS HIGH (V_{DD}) for five rising edges of TCK. This RESET does not affect the operation of the SRAM and may be performed while the SRAM is operating. At power-up, the TAP is reset internally to ensure that TDO comes up in a High-Z state.

TAP Registers

Registers are connected between the TDI and TDO pins and allow data to be scanned into and out of the SRAM test circuitry. Only one register can be selected at a time through the instruction registers. Data is serially loaded into the TDI pin on the rising edge of TCK. Data is output on the TDO pin on the falling edge of TCK.

Instruction Register

Three-bit instructions can be serially loaded into the instruction register. This register is loaded when it is placed between the TDI and TDO pins as shown in the TAP Controller Block diagram. Upon power-up, the instruction register is loaded with the IDCODE instruction. It is also loaded with the IDCODE instruction if the controller is placed in a reset state as described in the previous section.

When the TAP controller is in the CaptureIR state, the two least significant bits are loaded with a binary “01” pattern to allow for fault isolation of the board level serial test path.

Bypass Register

To save time when serially shifting data through registers, it is sometimes advantageous to skip certain states. The bypass register is a single-bit register that can be placed between TDI and TDO pins. This allows data to be shifted through the SRAM with minimal delay. The bypass register is set LOW (V_{SS}) when the BYPASS instruction is executed.

Boundary Scan Register

The boundary scan register is connected to all the I/O pins on the SRAM. Several no connect (NC) pins are also included in the scan register to reserve pins for higher density devices. The ×36 configuration has a 70-bit-long register, and the ×18 configuration has a 51-bit-long register.

The boundary scan register is loaded with the contents of the RAM I/O ring when the TAP controller is in the Capture-DR state. It is then placed between the TDI and TDO pins when the controller is moved to the Shift-DR state. The EXTEST, SAMPLE/PRELOAD and SAMPLE Z instructions can be used to capture the contents of the I/O ring.

The Boundary Scan Order tables show the order in which the bits are connected. Each bit corresponds to one of the bumps on the SRAM package. The MSB of the register is connected to TDI, and the LSB is connected to TDO.

Identification (ID) Register

The ID register is loaded with a vendor-specific, 32-bit code during the Capture-DR state when the IDCODE command is loaded in the instruction register. The IDCODE is hardwired into the SRAM and can be shifted out when the TAP controller is in the Shift-DR state. The ID register has a vendor code and other information described in the Identification Register Definitions table.

TAP Instruction Set

Eight different instructions are possible with the three-bit instruction register. All combinations are listed in the Instruction Code table. Three of these instructions are listed as RESERVED and should not be used. The other five instructions are described in detail below.

The TAP controller used in this SRAM is not fully compliant with the 1149.1 convention because some of the mandatory 1149.1 instructions are not fully implemented. The TAP controller cannot be used to load address, data, or control signals into the SRAM, and cannot preload the I/O buffers. The SRAM does not implement the 1149.1 commands EXTEST or

INTEST or the PRELOAD portion of SAMPLE/PRELOAD; rather it performs a capture of the I/O ring when these instructions are executed.

Instructions are loaded into the TAP controller during the Shift-IR state when the instruction register is placed between TDI and TDO (during this state, instructions are shifted through the instruction register through the TDI and TDO pins). To execute the instruction once it is shifted in, the TAP controller needs to be moved into the Update-IR state.

EXTEST

EXTEST is a mandatory 1149.1 instruction that is to be executed whenever the instruction register is loaded with all 0s. EXTEST is not implemented in the TAP controller, and therefore this device is not compliant with the 1149.1 standard.

The TAP controller does recognize an all-0 instruction. When an EXTEST instruction is loaded into the instruction register, the SRAM responds as if a SAMPLE/PRELOAD instruction has been loaded. There is one difference between the two instructions: unlike the SAMPLE/PRELOAD instruction, EXTEST places the SRAM outputs in a High-Z state.

IDCODE

The IDCODE instruction causes a vendor-specific, 32-bit code to be loaded into the instruction register. It also places the instruction register between the TDI and TDO pins and allows the IDCODE to be shifted out of the device when the TAP controller enters the Shift-DR state. The IDCODE instruction is loaded into the instruction register upon power-up or whenever the TAP controller is given a test logic reset state.

SAMPLE Z

The SAMPLE Z instruction causes the boundary scan register to be connected between the TDI and TDO pins when the TAP controller is in a Shift-DR state. It also places all SRAM outputs into a High-Z state.

SAMPLE/PRELOAD

SAMPLE/PRELOAD is a 1149.1-mandatory instruction. The PRELOAD portion of this instruction is not implemented, so the TAP controller is not fully 1149.1 compliant.

When the SAMPLE/PRELOAD instructions loaded into the instruction register and the TAP controller in the Capture-DR state, a snapshot of data on the I/O pins is captured in the boundary scan register.

The user must be aware that the TAP controller clock can only operate at a frequency up to 10 MHz, while the SRAM clock operates more than an order of magnitude faster. Because there is a large difference in the clock frequencies, it is possible that during the Capture-DR state, an input or output will undergo a transition. The TAP may then try to capture a signal while in transition (metastable state). This will not harm the device, but there is no guarantee as to the value that will be captured. Repeatable results may not be possible.

To guarantee that the boundary scan register will capture the correct value of a signal, the SRAM signal must be stabilized long enough to meet the TAP controller's capture set-up plus hold times (TCS and TCH). The SRAM clock input might not be captured correctly if there is no way in a design to stop (or slow) the clock during a SAMPLE/PRELOAD instruction. If this is an issue, it is still possible to capture all other signals and simply ignore the value of the CK and CK# captured in the boundary scan register.

Once the data is captured, it is possible to shift out the data by putting the TAP into the Shift-DR state. This places the boundary scan register between the TDI and TDO pins.

Note that since the PRELOAD part of the command is not implemented, putting the TAP into the Update to the Update-DR state while performing a SAMPLE/PRELOAD instruction will have the same effect as the Pause-DR command.

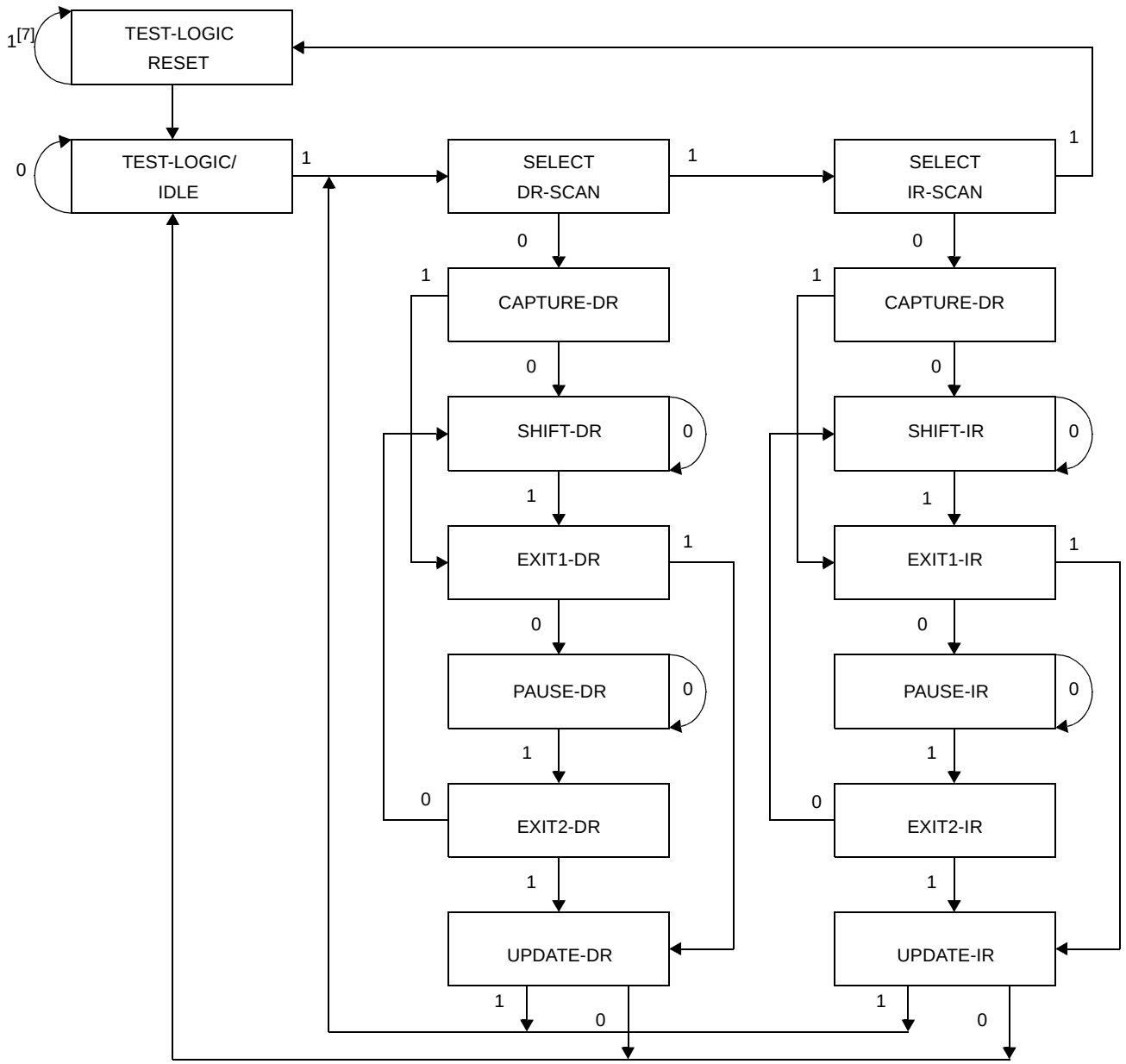
Bypass

When the BYPASS instruction is loaded in the instruction register and the TAP is placed in a Shift-DR state, the bypass register is placed between the TDI and TDO pins. The advantage of the BYPASS instruction is that it shortens the boundary scan path when multiple devices are connected together on a board.

Reserved

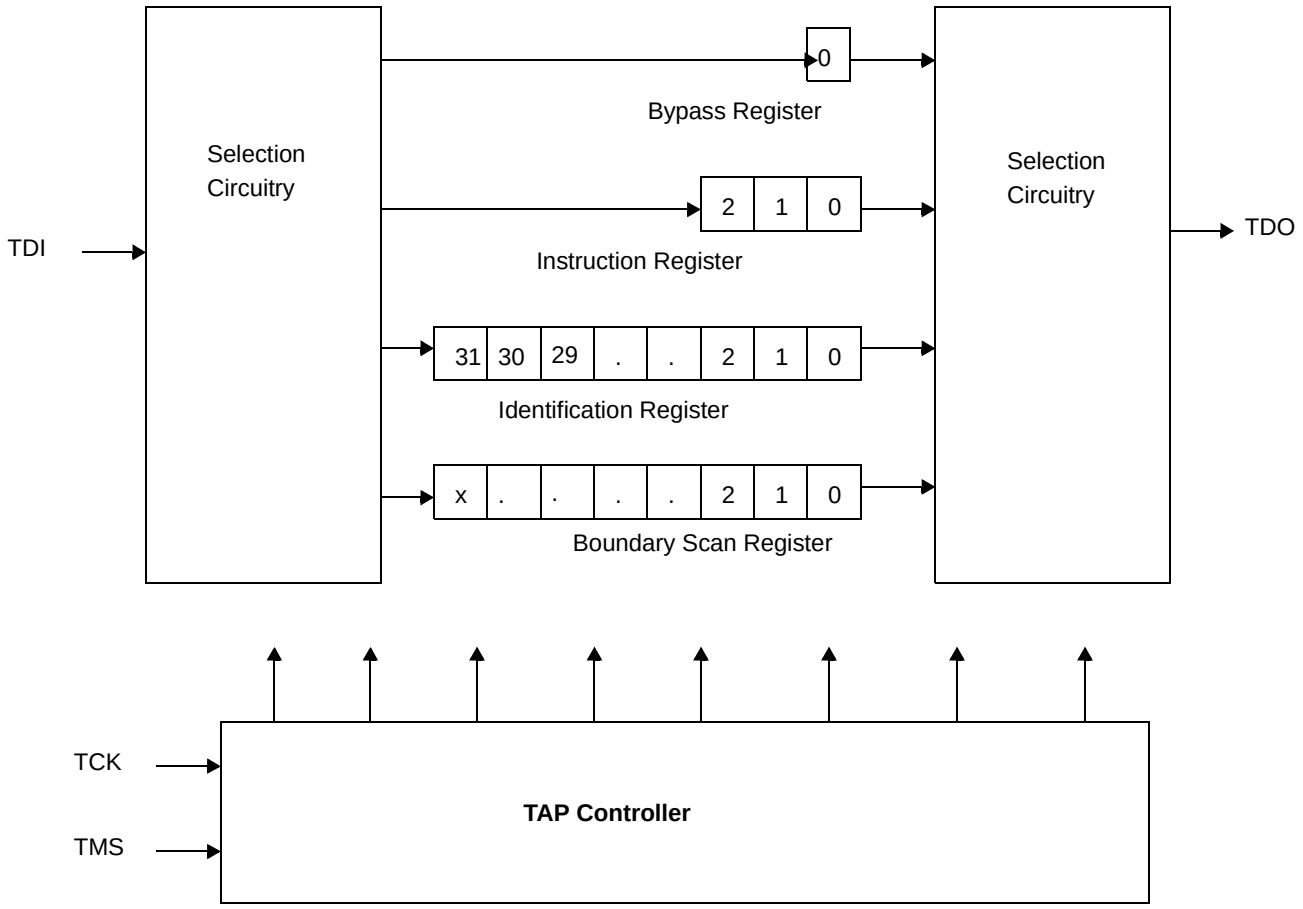
These instructions are not implemented but are reserved for future use. Do not use these instructions.

TAP Controller State Diagram



Note:
7. The 0/1 next to each state represents the value at TMS at the rising edge of TCK.

TAP Controller Block Diagram



TAP Electrical Characteristics Over the Operating Range[8, 9]

Parameter	Description	Test Conditions	Min.	Max.	Unit
V_{OH1}	Output HIGH Voltage	I_{OH} = –4.0 mA	2.4		V
V_{OH2}	Output HIGH Voltage	I_{OH} = –100 µA	V_{DD} – 0.2		V
V_{OL1}	Output LOW Voltage	I_{OL} = 8.0 mA		0.4	V
V_{OL2}	Output LOW Voltage	I_{OL} = 100 µA		0.2	V
V_{IH}	Input HIGH Voltage		1.7	V_{DD} + 0.3	V
V_{IL}	Input LOW Voltage		–0.5	0.7	V
I_X	Input Load Current	$GND \le V_I \le V_{DDQ}$	–5	5	µA

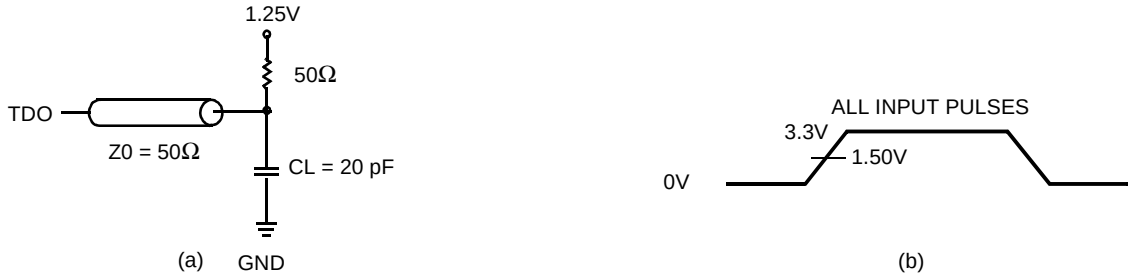
Notes:
8. All voltage referenced to Ground.
9. Overshoot: V_{IH} (AC) $\le$ V_{DD} + 1.5V for t $\le$ $t_{TCYC}/2$; undershoot: V_{IL} (AC) $\le$ 0.5V for t $\le$ $t_{TCYC}/2$; power-up: V_{IH} < 2.6V and V_{DD} < 2.4V and V_{DDQ} < 1.4V for t < 200 ms.

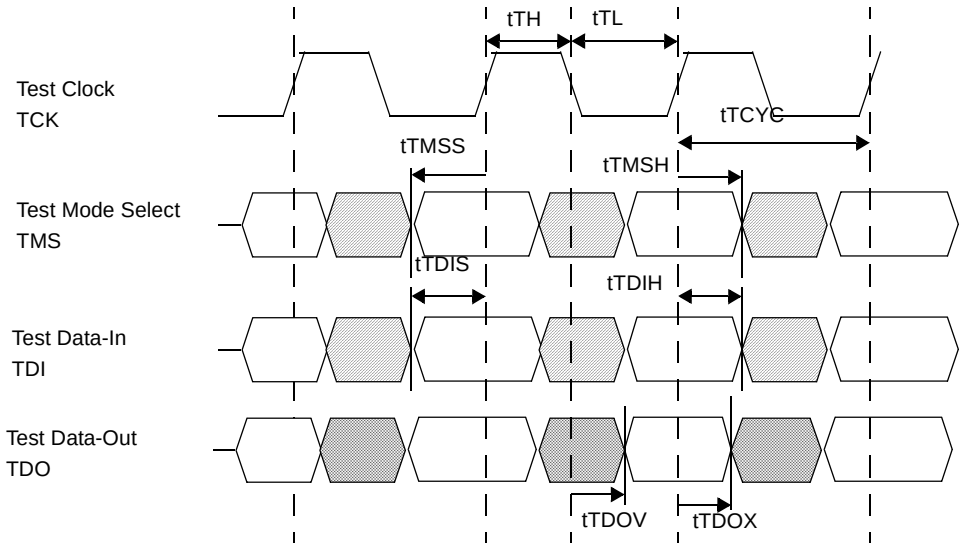
TAP AC Switching Characteristics Over the Operating Range[10, 11]

Parameter	Description	Min.	Max.	Unit
t_{TCYC}	TCK Clock Cycle Time	100		ns
t_{TF}	TCK Clock Frequency		10	MHz
t_{TH}	TCK Clock HIGH	40		ns
t_{TL}	TCK Clock LOW	40		ns
Set-up Times				
t_{TMSS}	TMS Set-up to TCK Clock Rise	10		ns
t_{TDIS}	TDI Set-up to TCK Clock Rise	10		ns
t_{CS}	Capture Set-up to TCK Rise	10		ns
Hold Times				
t_{TMSH}	TMS Hold after TCK Clock Rise	10		ns
t_{TDIH}	TDI Hold after Clock Rise	10		ns
t_{CH}	Capture Hold after Clock Rise	10		ns
Output Times				
t_{TDOV}	TCK Clock LOW to TDO Valid		20	ns
t_{TDOX}	TCK Clock HIGH to TDO Invalid	0		ns

Notes:
10. t_{CS} and t_{CH} refer to the set-up and hold time requirements of latching data from the boundary scan register.
11. Test conditions are specified using the load in TAP AC test conditions. t_R/t_F = 1 ns.

TAP Timing and Test Conditions





Identification Register Definitions

Instruction Field	512K x 36	1M x 18	Description
Revision Number (31:28)	0000	0000	Reserved for version number.
Device Depth (27:23)	00111	01000	Defines depth of SRAM. 512K or 1M
Device Width (22:18)	00100	00011	Defines with of the SRAM. x36 or x18
Cypress Device ID (17:12)	000000	000000	Reserved for future use.
Cypress JEDEC ID (11:1)	00011100100	00011100100	Allows unique identification of SRAM vendor.
ID Register Presence (0)	1	1	Indicate the presence of an ID register.

Scan Register Sizes

Register Name	Bit Size (x18)	Bit Size (x36)
Instruction	3	3
Bypass	1	1
ID	32	32
Boundary Scan	51	70

Identification Codes

Instruction	Code	Description
EXTEST	000	**Captures the I/O ring contents**. Places the boundary scan register between the TDI and TDO. Forces all SRAM outputs to High-Z state. This instruction is not 1149.1-compliant.
IDCODE	001	Loads the ID register with the vendor ID code and places the register between TDI and TDO. This operation does not affect SRAM operation.
SAMPLE Z	010	**Captures the I/O contents**. Places the boundary scan register between TDI and TDO. Forces all SRAM output drivers to a High-Z state.
RESERVED	011	Do Not Use: This instruction is reserved for future use.
SAMPLE/PRELOAD	100	**Captures the I/O ring contents**. Places the boundary scan register between TDI and TDO. Does not affect the SRAM operation. This instruction does not implement 1149.1 preload function and is therefore not 1149.1-compliant.
RESERVED	101	**Do Not Use**. This instruction is reserved for future use.
RESERVED	110	**Do Not Use**. This instruction is reserved for future use.
BYPASS	111	**Places the bypass register between TDI and TDO**. This operation does not affect SRAM operation.

Boundary Scan Order

CY7C1371B (512K × 36)						CY7C1373B (1M × 18)					
Bit #	Signal Name	Bump ID	Bit #	Signal Name	Bump ID	Bit #	Signal Name	Bump ID	Bit #	Signal Name	Bump ID
1	A	2R	36	CE3	6B	1	A	2R	36	DQb	2E
2	A	3T	37	BWSa	5L	2	A	2T	37	DQb	2G
3	A	4T	38	BWSb	5G	3	A	3T	38	DQb	1H
4	A	5T	39	BWSc	3G	4	A	5T	39	SN	5R
5	A	6R	40	BWSd	3L	5	A	6R	40	DQb	2K
6	A	3B	41	CE2	2B	6	A	3B	41	DQb	1L
7	A	5B	42	CE1	4E	7	A	5B	42	DQb	2M
8	DPa	6P	43	A	3A	8	DQa	7P	43	DQb	1N
9	DQa	7N	44	A	2A	9	DQa	6N	44	DPb	2P
10	DQa	6M	45	DPc	2D	10	DQa	6L	45	MODE	3R
11	DQa	7L	46	DQc	1E	11	DQa	7K	46	A	2C
12	DQa	6K	47	DQc	2F	12	NC	7T	47	A	3C
13	DQa	7P	48	DQc	1G	13	DQa	6H	48	A	5C
14	DQa	6N	49	DQc	2H	14	DQa	7G	49	A	6C
15	DQa	6L	50	DQc	1D	15	DQa	6F	50	A1	4N
16	DQa	7K	51	DQc	2E	16	DQa	7E	51	A0	4P
17	NC	7T	52	DQc	2G	17	DPa	6D			
18	DQb	6H	53	DQc	1H	18	A	6T			
19	DQb	7G	54	SN	5R	19	A	6A			
20	DQb	6F	55	DQd	2K	20	A	5A			
21	DQb	7E	56	DQd	1L	21	A	4G			
22	DQb	6D	57	DQd	2M	22	A	4A			
23	DQb	7H	58	DQd	1N	23	ADV/$\overline{LD}$	4B			
24	DQb	6G	59	DQd	2P	24	OE	4F			
25	DQb	6E	60	DQd	1K	25	CEN	4M			
26	DPb	7D	61	DQd	2L	26	WE	4H			
27	A	6A	62	DQd	2N	27	CLK	4K			
28	A	5A	63	DPd	1P	28	CE3	6B			
29	A	4G	64	MODE	3R	29	BWSa	5L			
30	A	4A	65	A	2C	30	BWSb	3G			
31	ADV/$\overline{LD}$	4B	66	A	3C	31	CE2	2B			
32	$\overline{OE}$	4F	67	A	5C	32	CE1	4E			
33	$\overline{CEN}$	4M	68	A	6C	33	A	3A			
34	$\overline{WE}$	4H	69	A1	4N	34	A	2A			
35	CLK	4K	70	A0	4P	35	DQb	1D			

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... –55°C to +150°C

Ambient Temperature with Power Applied..... –55°C to +125°C

Supply Voltage on V_{DD} Relative to GND..... –0.5V to +4.6V

DC Voltage Applied to Outputs in High-Z State[13]..... –0.5V to V_{DDQ} + 0.5V

DC Input Voltage[13]..... –0.5V to V_{DDQ} + 0.5V

Current into Outputs (LOW)..... 20 mA

Static Discharge Voltage..... > 1500V (per MIL-STD-883, Method 3015)

Latch-up Current..... > 200 mA

Operating Range

Range	Ambient Temperature[12]	V_{DD}	V_{DDQ}
Commercial	0°C to +70°C	3.3V – 5%/ +10%	2.5V – 5% 3.3V + 10%
Industrial	–40°C to +85°C		

Electrical Characteristics Over the Operating Range[14]

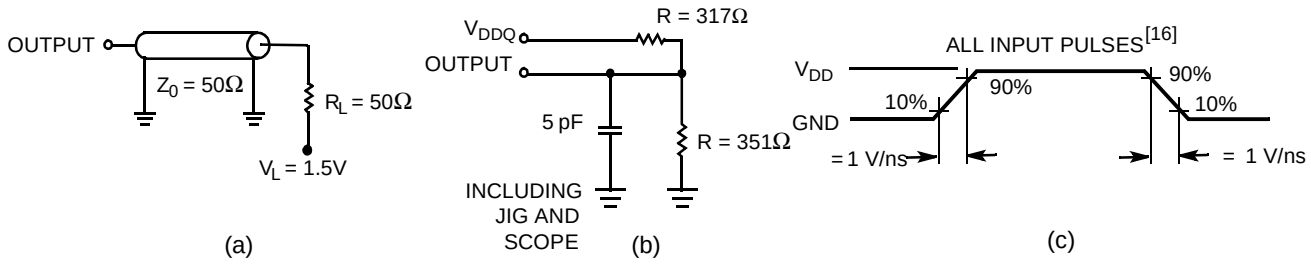
Parameter	Description	Test Conditions		Min.	Max.	Unit
V_{DD}	Power Supply Voltage			3.135	3.63	V
V_{DDQ}	I/O Supply Voltage			2.375	V_{DD}	V
V_{OH}	Output HIGH Voltage	V_{DD} = Min., I_{OH} = –1.0 mA	V_{DDQ} = 2.5V	2.0		V
		V_{DD} = Min., I_{OH} = –4.0 mA	V_{DDQ} = 3.3V	2.4		V
V_{OL}	Output LOW Voltage	V_{DD} = Min., I_{OL} = 1.0 mA	V_{DDQ} = 2.5V		0.4	V
		V_{DD} = Min., I_{OL} = 8.0 mA	V_{DDQ} = 3.3V		0.4	V
V_{IH}	Input HIGH Voltage		V_{DDQ} = 3.3V	2		V
			V_{DDQ} = 2.5V	1.7		V
V_{IL}	Input LOW Voltage		V_{DDQ} = 3.3V	–0.3	0.8	V
			V_{DDQ} = 2.5V	–0.3	0.7	V
I_X	Input Load Current	GND ≤ V_I ≤ V_{DDQ}			5	µA
	Input Current of MODE			–30	30	µA
	Input Current of ZZ	Input = V_{SS}		–30	30	µA
I_{OZ}	Output Leakage Current	GND ≤ V_I ≤ V_{DDQ}, Output Disabled			5	µA
I_{DD}	V_{DD} Operating Supply	V_{DD} = Max., I_{OUT} = 0 mA, f = f_{MAX} = $1/t_{CYC}$	8.5-ns cycle, 117 MHz		250	mA
			10-ns cycle, 100 MHz		225	mA
			12-ns cycle, 83 MHz		185	mA
I_{SB1}	Automatic CE Power-Down Current—TTL Inputs	Max. V_{DD}, Device Deselected, V_{IN} ≥ V_{IH} or V_{IN} ≤ V_{IL} f = f_{MAX} = $1/t_{CYC}$	8.5-ns cycle, 117 MHz		100	mA
			10-ns cycle, 100 MHz		90	mA
			12-ns cycle, 83 MHz		75	mA
I_{SB2}	Automatic CE Power-Down Current—CMOS Inputs	Max. V_{DD}, Device Deselected, V_{IN} ≤ 0.3V or V_{IN} ≥ V_{DDQ} ∠ 0.3V, f = 0	All speed grades		20	mA
I_{SB3}	Automatic CE Power-Down Current—CMOS Inputs	Max. V_{DD}, Device Deselected, or V_{IN} ≤ 0.3V or V_{IN} ≥ V_{DDQ} ∠ 0.3V f = f_{MAX} = $1/t_{CYC}$	8.5-ns cycle, 117 MHz		90	mA
			10-ns cycle, 100 MHz		75	mA
			12-ns cycle, 83 MHz		60	mA
I_{SB4}	Automatic CS Power-Down Current—TTL Inputs	Max. V_{DD}, Device Deselected, V_{IN} ≥ V_{IH} or V_{IN} ≤ V_{IL}, f = 0	All speeds		50	mA

Notes:
12. T_A is the case temperature.
13. Minimum voltage equals –2.0V for pulse durations of less than 20 ns.
14. The load used for V_{OH} and V_{OL} testing is shown in figure (b) of AC Test Loads.

Capacitance[15]

Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{DD} = V_{DDQ} = 2.5V	3	pF
C_{CLK}	Clock Input Capacitance		3	pF
$C_{I/O}$	I/O Capacitance		3	pF

AC Test Loads and Waveforms



Thermal Resistance[15]

Description	Test Conditions	Θ_{JA} (Junction to Ambient)	Θ_{JC} (Junction to Case)	Unit
119 BGA	Still Air, soldered on a 114.3 × 101.6 × 1.57 mm3, two-layer board	41.54	6.33	°C/W
165 FBGA		44.51	2.38	°C/W
100-pin TQFP	Still Air, soldered on a 4.25 × 1.125 inch, four-layer printed circuit board	25	9	°C/W

Notes:
15. Tested initially and after any design or process change that may affect these parameters.
16. Input waveform should have a slew rate of 1 V/ns.

Switching Characteristics Over the Operating Range[17]

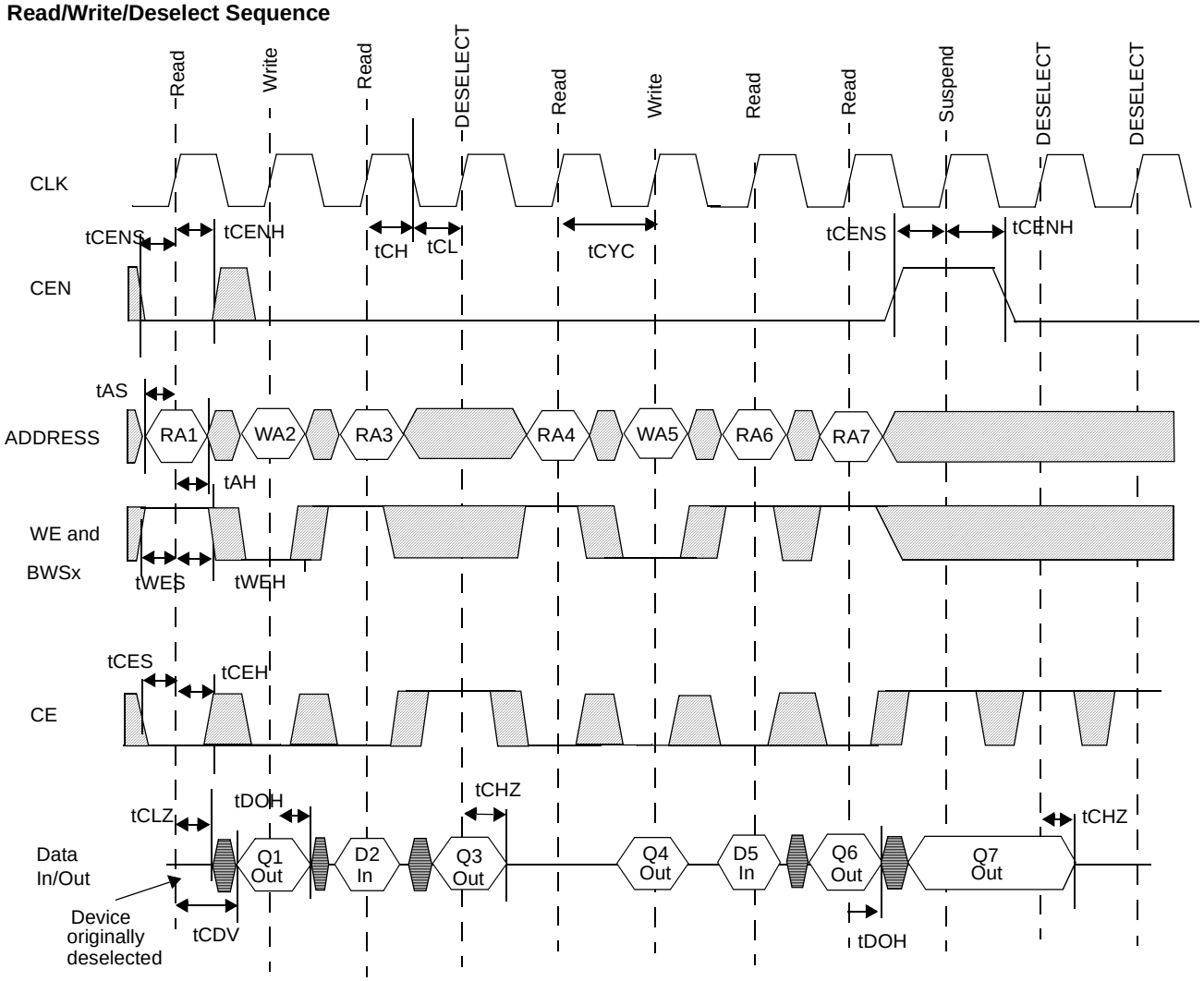
Parameter	Description	-117		-100		-83		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Clock								
t_{CYC}	Clock Cycle Time	8.5		10.0		12.0		ns
t_{CH}	Clock HIGH	2.3		2.5		3.0		ns
t_{CL}	Clock LOW	2.3		2.5		3.0		ns
Output Times								
t_{CO}	Data Output Valid After CLK Rise		7.5		8.5		10.0	ns
t_{EOV}	$\overline{OE}$ LOW to Output Valid[15, 18, 20]		3.4		3.8		4.2	ns
t_{DOH}	Data Output Hold After CLK Rise	1.3		1.3		1.3		ns
t_{CHZ}	Clock to High-Z[15, 17, 18, 19, 20]		3.0		3.0		3.0	ns
t_{CLZ}	Clock to Low-Z[15, 17, 18, 19, 20]	1.3		1.3		1.3		ns
t_{EOHZ}	$\overline{OE}$ HIGH to Output High-Z[17, 18, 20]		4.0		4.0		4.0	ns
t_{EOLZ}	$\overline{OE}$ LOW to Output Low-Z[17, 18, 20]	0		0		0		ns
Set-Up Times								
t_{AS}	Address Set-Up Before CLK Rise	1.5		1.5		1.5		ns
t_{DS}	Data Input Set-Up Before CLK Rise	1.5		1.5		1.5		ns
t_{CENS}	$\overline{CEN}$ Set-Up Before CLK Rise	1.5		1.5		1.5		ns
t_{WES}	$\overline{WE}$, $\overline{BWS_X}$ Set-Up Before CLK Rise	1.5		1.5		1.5		ns
t_{ALS}	ADV/$\overline{LD}$ Set-Up Before CLK Rise	1.5		1.5		1.5		ns
t_{CES}	Chip Select Set-Up	1.5		1.5		1.5		ns
Hold Times								
t_{AH}	Address Hold After CLK Rise	0.5		0.5		0.5		ns
t_{DH}	Data Input Hold After CLK Rise	0.5		0.5		0.5		ns
t_{CENH}	$\overline{CEN}$ Hold After CLK Rise	0.5		0.5		0.5		ns
t_{WEH}	$\overline{WE}$, $\overline{BW_X}$Hold After CLK Rise	0.5		0.5		0.5		ns
t_{ALH}	ADV/$\overline{LD}$ Hold after CLK Rise	0.5		0.5		0.5		ns
t_{CEH}	Chip Select Hold After CLK Rise	0.5		0.5		0.5		ns

Notes:

17. Unless otherwise noted, test conditions assume signal transition time of 2.5 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH} and load capacitance. Shown in (a), (b) and (c) of AC Test Loads.
18. t_{CHZ}, t_{CLZ}, t_{EOV}, t_{EOLZ}, and t_{EOHZ} are specified with AC test conditions shown in part (a) of AC Test Loads. Transition is measured ± 200 mV from steady-state voltage.
19. At any given voltage and temperature, t_{EOHZ} is less than t_{EOLZ} and t_{CHZ} is less than t_{CLZ} to eliminate bus contention between SRAMs when sharing the same data bus. These specifications do not imply a bus contention condition, but reflect parameters guaranteed over worst case user conditions. Device is designed to achieve High-Z prior to Low-Z under the same system conditions.
20. This parameter is sampled and not 100% tested.

Switching Waveforms

Read/Write/Deselect Sequence

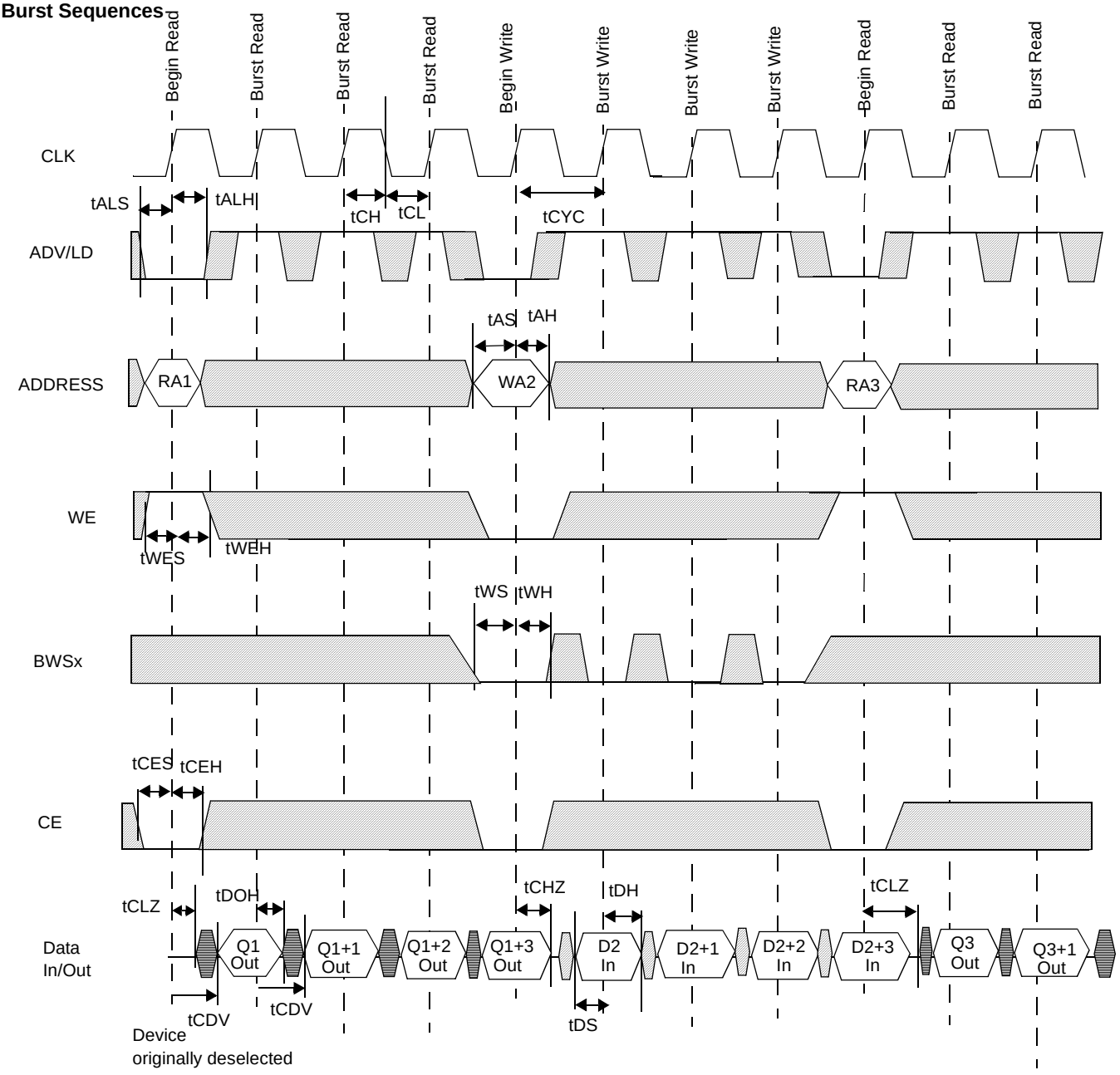


The combination of WE and BWSx (x = a, b, c, d) to define a Write cycle (see Write Cycle Description table). CE is the combination of CE1, CE2, and CE3. All chip selects need to be active in order to select the device. Any chip select can deselect the device. RAx stands for Read Address X, WA stands for Write Address X, Dx stands for Data-in X, Qx stands for Data-out X.

= Don't Care = Undefined

Switching Waveforms (continued)

Burst Sequences

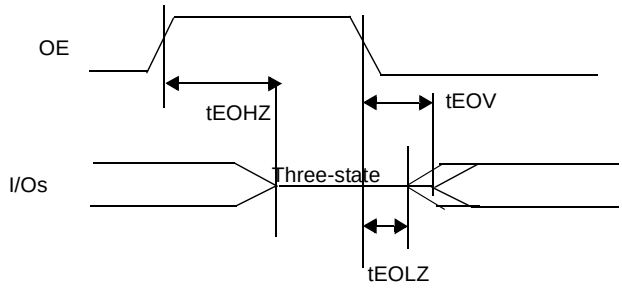


The combination of WE and BWSx (x = a, b, c, d) define a Write cycle (see Write Cycle Description table). CE is the combination of CE1, CE2, and CE3. All chip enables need to be active in order to select the device. Any chip enable can deselect the device. RAx stands for Read Address X, WA stands for Write Address X, Dx stands for Data-in for location X, Qx stands for Data-out for location X. CEN held LOW. During burst writes, byte writes can be conducted by asserting the appropriate BWSx input signals. Burst order determined by the state of the MODE input. CEN held LOW. OE held LOW.

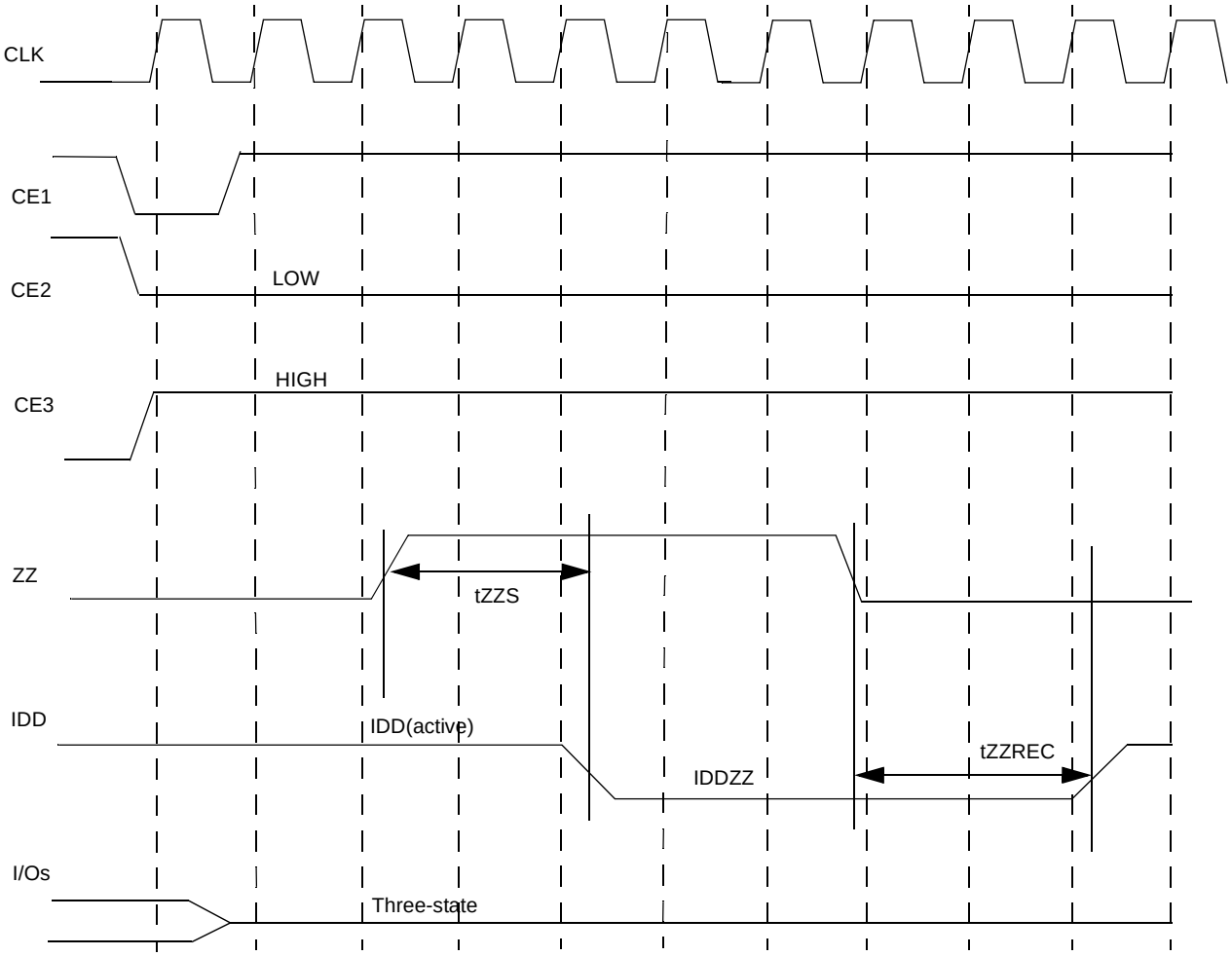
= Don't Care = Undefined

Switching Waveforms (continued)

$\overline{OE}$ Timing



ZZ Mode Timing[21, 22]



Notes:
21. Device must be deselected when entering ZZ mode. See Cycle Descriptions Table for all possible signal conditions to deselect the device.
22. I/Os are in three-state when exiting ZZ sleep mode.

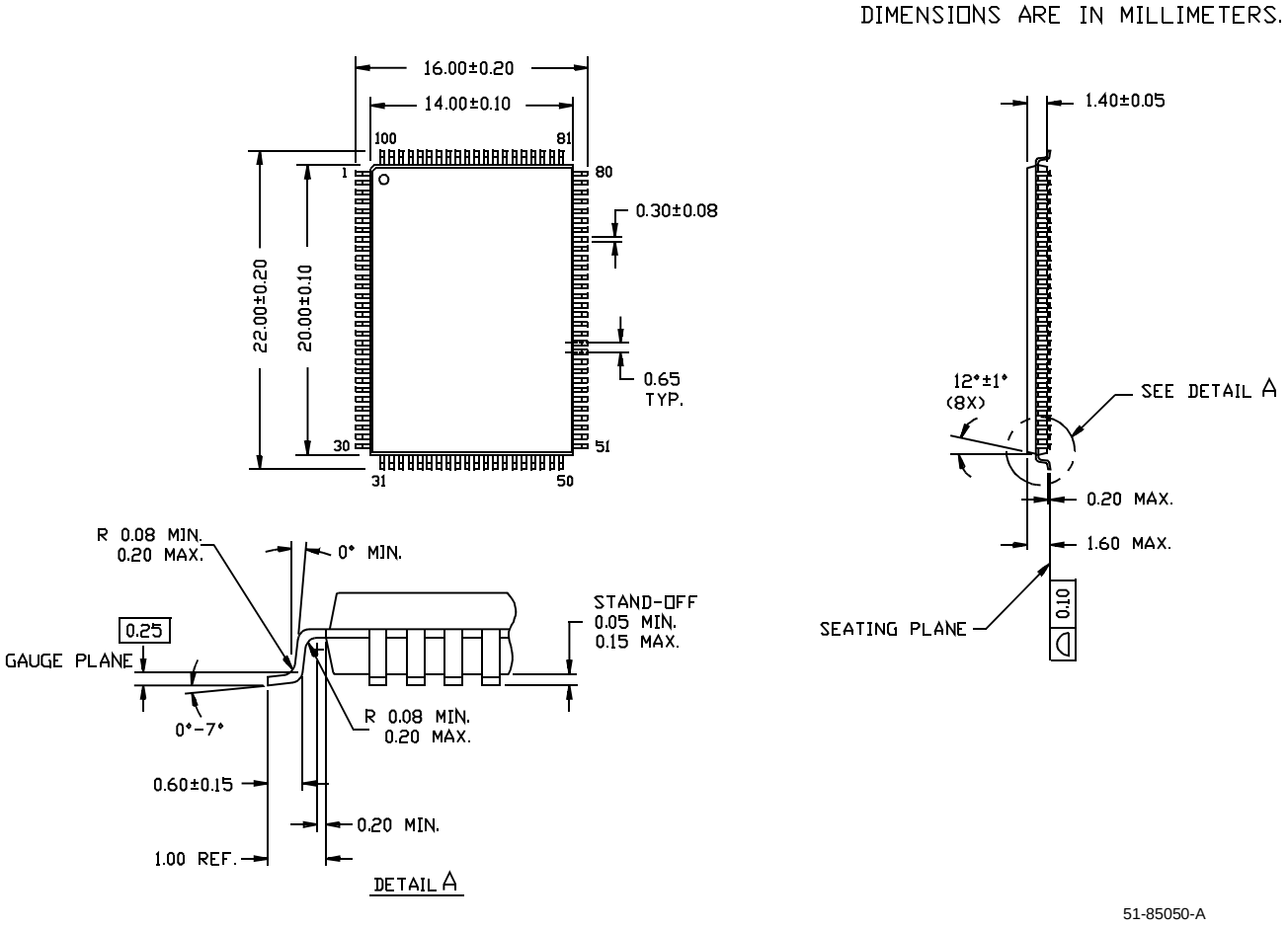
Ordering Information

Speed (MHz)	Ordering Code	Package Name	Package Type	Operating Range
117	CY7C1371B-117AC CY7C1373B-117AC	A101	100-lead Thin Quad Flat Pack	Commercial
	CY7C1371B-117BGC CY7C1373B-117BGC	BG119	119 PBGA	
	CY7C1371B-117BZC CY7C1373B-117BZC	BB165A	165 FBGA	
100	CY7C1371B-100AC CY7C1373B-100AC	A101	100-lead Thin Quad Flat Pack	
	CY7C1371B-100BGC CY7C1373B-100BGC	BG119	119 PBGA	
	CY7C1371B-100BZC CY7C1373B-100BZC	BB165A	165 FBGA	
83	CY7C1371B-83AC	A101	100-lead Thin Quad Flat Pack	
100	CY7C1371B-100AI CY7C1373B-100AI	A101	100-lead Thin Quad Flat Pack	Industrial
	CY7C1371B-100BGI CY7C1373B-100BGI	BG119	119 PBGA	
	CY7C1371B-100BZI CY7C1373B-100BZI	BB165A	165 FBGA	

Shaded areas contain advance information.

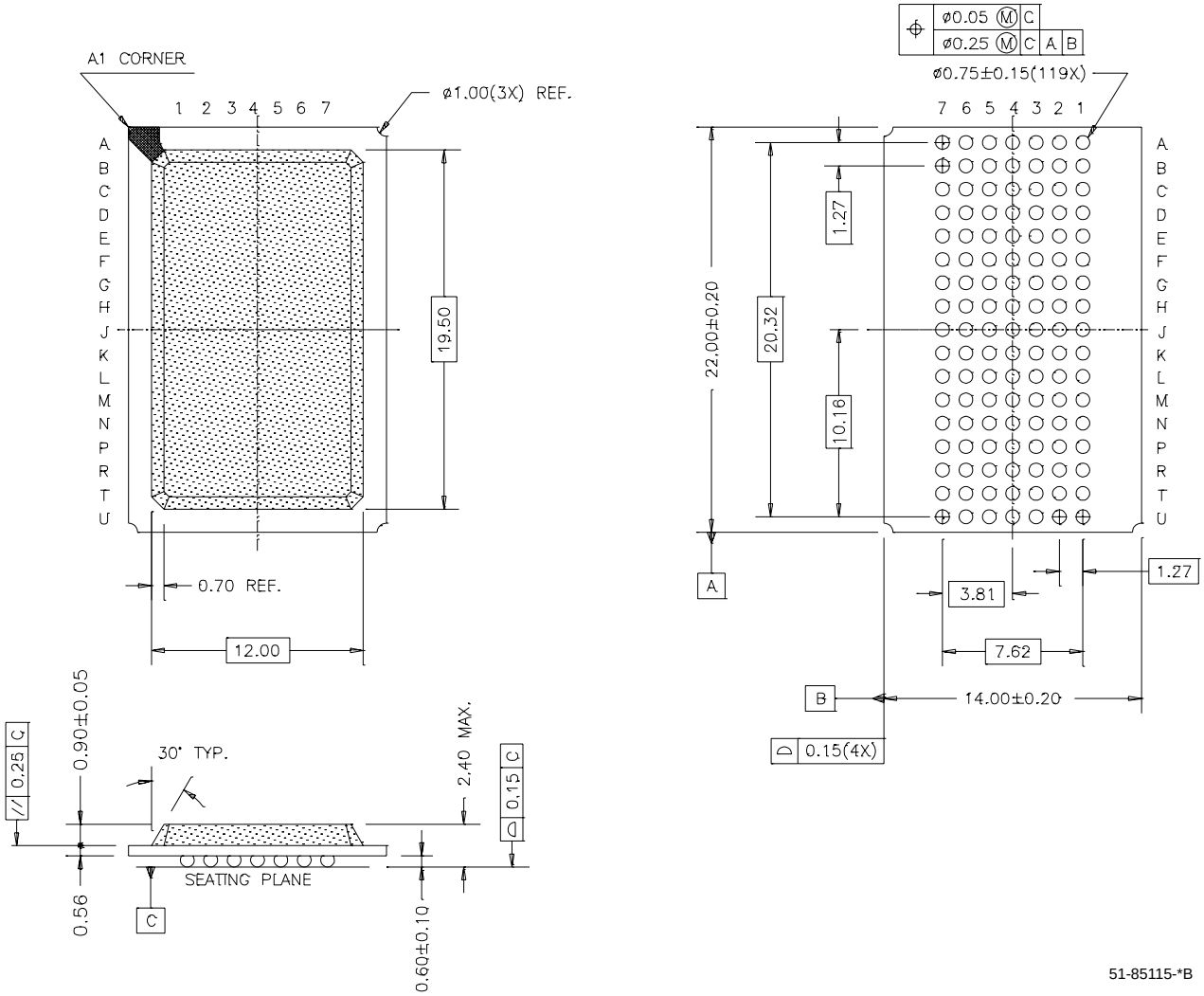
Package Diagrams

100-Pin Thin Plastic Quad Flatpack (14 x 20 x 1.4 mm) A101



Package Diagrams (continued)

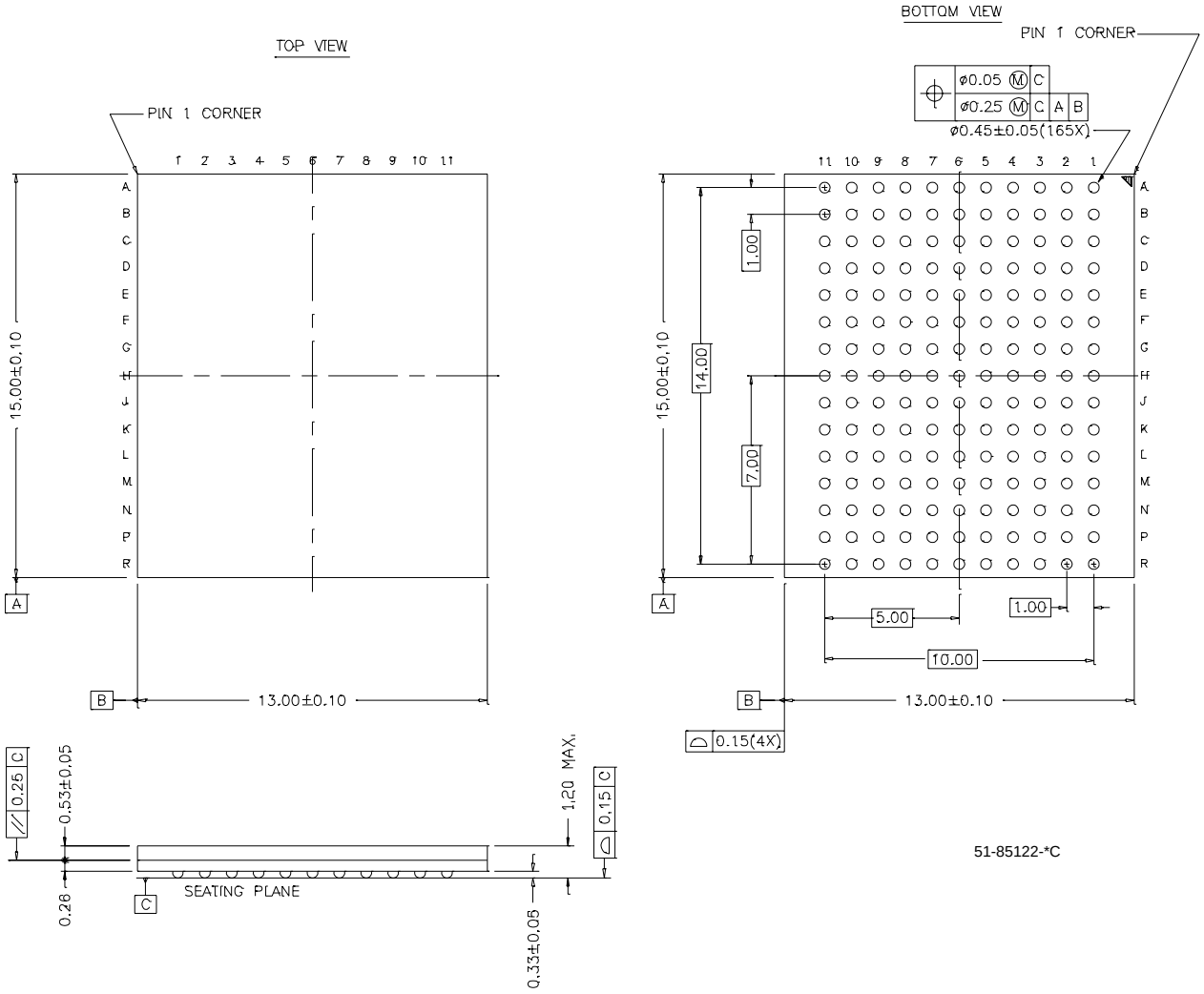
119-Lead PBGA (14 x 22 x 2.4 mm) BG119



51-85115-*B

Package Diagrams (continued)

165-Ball FBGA (13 x 15 x 1.2 mm) BB165A



Document History Page

Document Title: CY7C1371B/CY7C1373B 512K x 36/1M x 18 Flow-Thru SRAM with NoBL™ Architecture Document Number: 38-05198				
REV.	**ECN NO.**	**ISSUE DATE**	**ORIG. OF CHANGE**	**DESCRIPTION OF CHANGE**
**	112250	03/01/02	DSG	Change from Spec number: 38-01071 to 38-05198
*A	115733	06/20/02	CJM	1) Updated Boundary Scan Order 2) Changed t_{DOH} from 1.5 to 1.3 ns all speeds 3) Updated Ordering Information
*B	121533	11/19/02	DSG	Updated package diagrams 51-85115 (BG119) to rev. *B and 51-85122 (BB165A) to rev. *C