

T-46-23-08



CYPRESS SEMICONDUCTOR

CY7C123

256 x 4 Static R/W RAM

Features

- 256 x 4 static RAM for control store in high-speed computers
- CMOS for optimum speed/power
- High speed
 - 7 ns (commercial)
 - 10 ns (military)
- Low power
 - 660 mW (commercial)
 - 825 mW (military)
- Separate inputs and outputs
- 5-volt power supply $\pm 10\%$ tolerance both commercial and military
- TTL-compatible inputs and outputs
- 24 pins
- 300-mil package

Functional Description

The CY7C123 is a high-performance CMOS static RAM organized as 256 words by 4 bits. Easy memory expansion is provided by an active LOW chip select one (\overline{CS}_1) input, an active HIGH chip select two (CS_2) input, and three-state outputs.

Writing to the device is accomplished when the chip select one (\overline{CS}_1) and write enable (\overline{WE}) inputs are both LOW and the chip select two input is HIGH. Data on the four data inputs (D_0 through D_3) is written into the memory location specified on the address pins (A_0 through A_7). The outputs are preconditioned so that the write data is present at the outputs when the write cycle is complete. This precondition operation ensures minimum write recovery times by eliminating the "write recovery glitch."

Reading the device is accomplished by taking the chip select one (\overline{CS}_1) and output enable (\overline{OE}) inputs LOW, while the write enable (\overline{WE}) and chip select two (CS_2) inputs remain HIGH. Under these conditions, the contents of the memory location specified on the address pins will appear on the four output pins (O_0 through O_3).

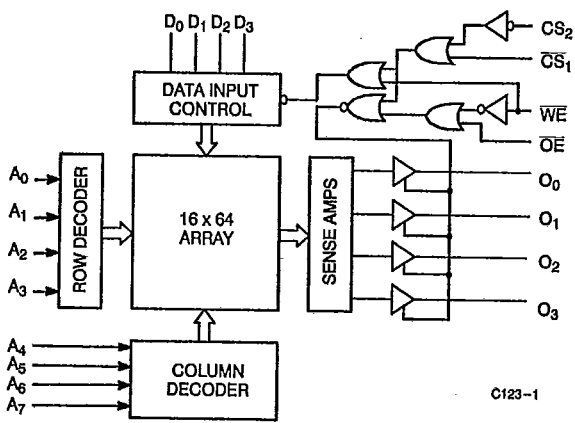
The output pins remain in high-impedance state when chip select one (\overline{CS}_1) or output enable (\overline{OE}) is HIGH, or write enable (\overline{WE}) or chip select two (CS_2) is LOW.

A die coat is used to insure alpha immunity.

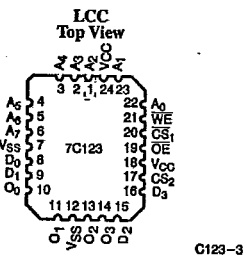
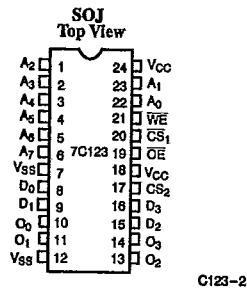


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Logic Block Diagram



Pin Configurations



Selection Guide

		7C123-7	7C123-9	7C123-10	7C123-12	7C123-15
Maximum Access Time (ns)	Commercial	7	9		12	
	Military			10	12	15
Maximum Operating Current (mA)	Commercial	120	120		120	
	Military			150	150	150



Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature - 65°C to +150°C
 Ambient Temperature with Power Applied - 55°C to +125°C
 Supply Voltage to Ground Potential (Pins 24 and 18 to Pins 7 and 12)^[1] - 0.5V to +7.0V
 DC Voltage Applied to Outputs in High Z State^[1] - 0.5V to +7.0V
 DC Input Voltage^[1] - 0.5V to + 7.0V

Output Current into Outputs (Low) 20 mA
 Latch-Up Current >200 mA

Operating Range

Range	Ambient Temperature ^[2]	V _{CC}
Commercial	0°C to + 70°C	5V ± 10%
Military	- 55°C to + 125°C	5V ± 10%

Electrical Characteristics Over the Operating Range^[3]

Parameters	Description	Test Conditions	7C123-7 7C123-9		7C123-10 7C123-15		7C123-12		Units	
			Min.	Max.	Min.	Max.	Min.	Max.		
V _{OH}	Output HIGH Voltage	V _{CC} = Min., I _{OH} = - 5.2 mA	2.4		2.4		2.4		V	
V _{OL}	Output LOW Voltage	V _{CC} = Min., I _{OL} = 8.0 mA		0.4		0.4		0.4	V	
V _{IH}	Input HIGH Voltage		2.2	V _{CC}	2.2	V _{CC}	2.2	V _{CC}	V	
V _{IL}	Input LOW Voltage ^[1]		- 0.8	+0.8	- 0.8	+0.8	- 0.8	+0.8	V	
I _{IX}	Input Load Current	V _{SS} ≤ V _I ≤ V _{CC}	- 10	+10	- 10	+10	- 10	+10	µA	
I _{OZ}	Output Current (High Z)	V _{SS} ≤ V _{OUT} ≤ V _{CC} , Output Disabled	- 10	+10	- 10	+10	- 10	+10	µA	
I _{CC}	Power Supply Current	V _{CC} = Max., I _{OUT} = 0 mA, f = f _{MAX} = 1/t _{RC}	Commercial		120				120	mA
			Military				150		150	mA

Capacitance^[4]

Parameters	Description	Test Conditions	Max.	Units
C _{IN}	Input Capacitance	T _A = 25°C, f = 1 MHz, V _{CC} = 5.0V	8	pF
C _{OUT}	Output Capacitance		8	pF

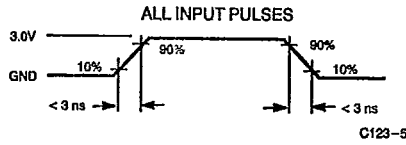
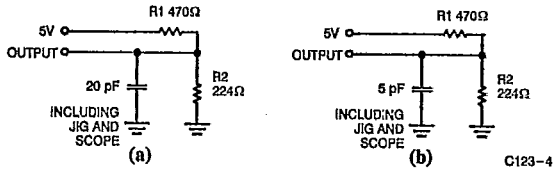
Logic Table^[5]

Inputs					Outputs	Mode
OE	CS ₁	CS ₂	WE	D ₀ - D ₃		
X	H	X	X	X	High Z	Not Selected
X	X	L	X	X	High Z	Not Selected
L	L	H	H	X	O ₀ - O ₃	Read Stored Data
X	L	H	L	L	High Z	Write "0"
X	L	H	L	H	High Z	Write "1"
H	L	H	H	X	High Z	Output Disabled

- Notes:
- V_{IL(Min)} = -3.0V for pulse durations of less than 20 ns.
 - T_A is the "instant on" case temperature.
 - See the last page of this specification for Group A subgroup testing information.
 - Tested initially and after any design or process changes that may affect these parameters.
 - H = High Voltage, L = Low Voltage, X = Don't Care, and High Z = High Impedance.



AC Test Loads and Waveforms



Equivalent to: THEVENIN EQUIVALENT
 OUTPUT — 152Ω — 1.62V

Switching Characteristics Over the Operating Range^[3]

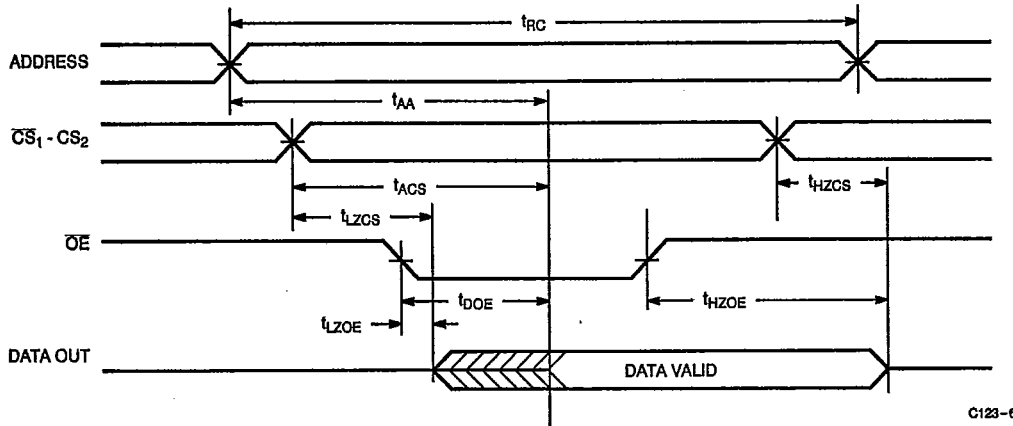
Parameters	Description	7C123-7		7C123-9		7C123-10		7C123-12		7C123-15		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE												
t _{RC}	Read Cycle Time	7		9		10		12		15		ns
t _{AA}	Address to Data Valid		7		9		10		12		15	ns
t _{ACS}	Chip Select to Data Valid		7		8		8		8		10	ns
t _{DOE}	OE LOW to Data Valid		7		8		8		8		10	ns
t _{HZCS}	Chip Select to High Z ^[6, 7]		5		6		6		6.5		8	ns
t _{HZOE}	OE HIGH to High Z ^[6]		5		6		6		6.5		8	ns
t _{LZCS}	Chip Select to Low Z ^[7]	2		2		2		2		2		ns
t _{LZOE}	OE LOW to Low Z	2		2		2		2		2		ns
WRITE CYCLE												
t _{WC}	Write Cycle Time	7		9		10		12		15		ns
t _{HZWE}	WE LOW to High Z ^[6]		5.5		6		6		7		8	ns
t _{LZWE}	WE HIGH to Low Z	2		2		2		2		2		ns
t _{PWE}	WE Pulse Width	5		6.5		7		8		11		ns
t _{SD}	Data Set-Up to Write End	5		6		7		8		11		ns
t _{HD}	Data Hold from Write End	1		1		1		1		1		ns
t _{SA}	Address Set-Up to Write Start	0.5		1		1		2		2		ns
t _{HA}	Address Hold from Write End	1.5		1.5		2		2		2		ns
t _{SCS}	CS LOW to Write End	5		6.5		7		8		11		ns
t _{AW}	Address Set-Up to Write End	5.5		7.5		8		10		13		ns

Notes:
 6. Transition is measured at steady state HIGH level - 500 mV or steady state LOW level +500 mV on the output from 1.5V level on the input with load shown in part (b) of AC Test Loads.
 7. At any given temperature and voltage condition, t_{HZCS} is less than t_{LZCS} for any given device.

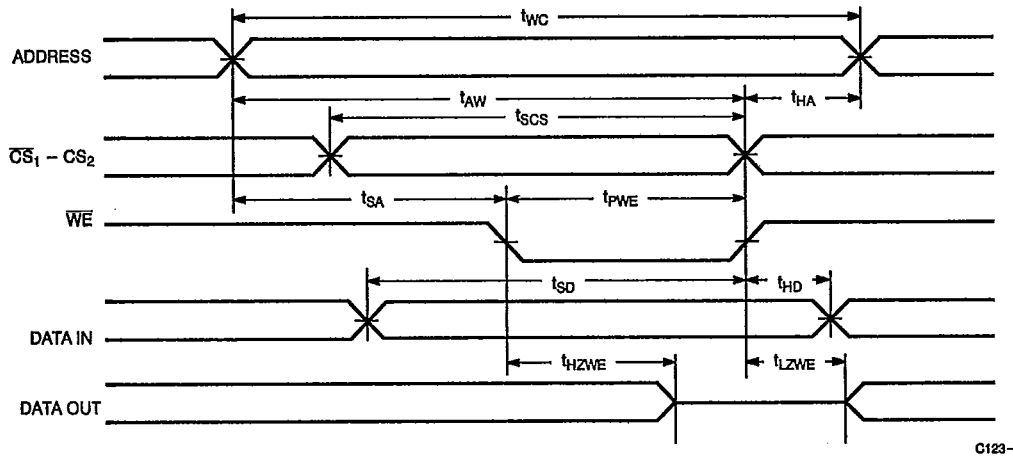


Switching Waveforms

Read Cycle [8, 9]



Write Cycle [7, 8]



Notes:

8. Measurements are referenced to 1.5V unless otherwise stated.

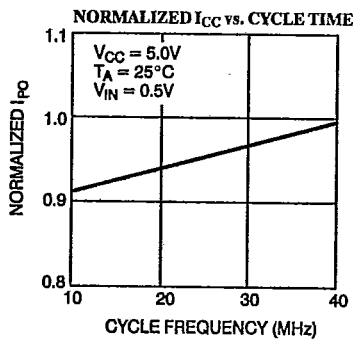
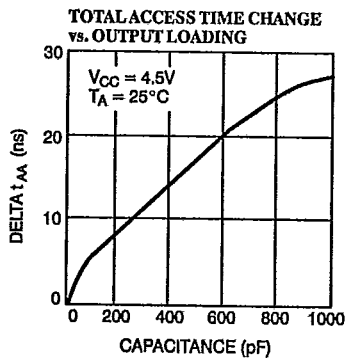
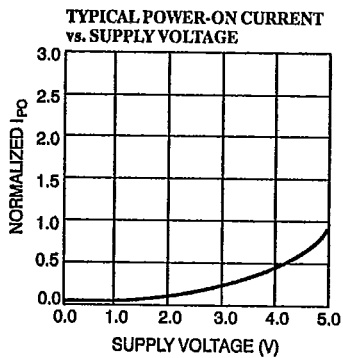
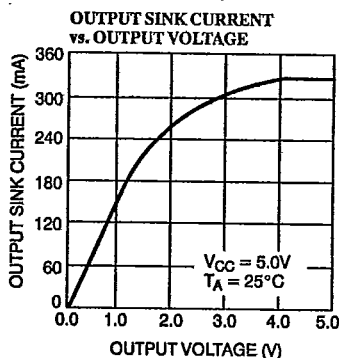
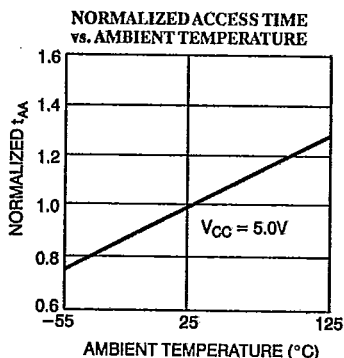
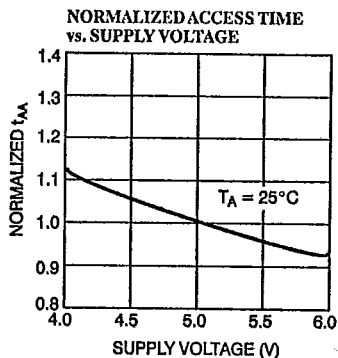
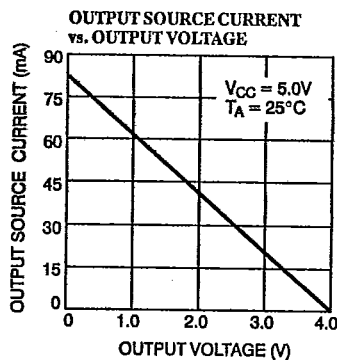
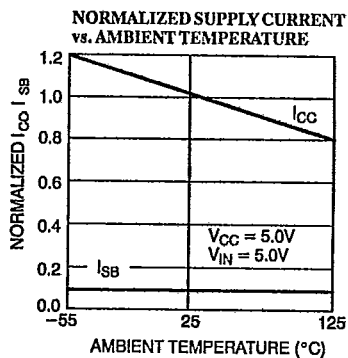
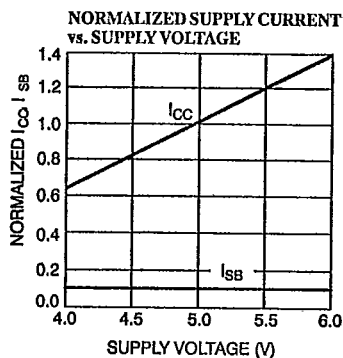
9. Timing diagram represents one solution that results in an optimum cycle time. Timing may be changed in various applications as long as the worst case limits are not violated.



Typical DC and AC Characteristics



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Ordering Information

Speed (ns)	Ordering Code	Package Type	Operating Range
7	CY7C123-7PC	P13A	Commercial
	CY7C123-7VC	V13	
	CY7C123-7DC	D14	
	CY7C123-7LC	L53	
9	CY7C123-9PC	P13A	Commercial
	CY7C123-9VC	V13	
	CY7C123-9DC	D14	
	CY7C123-9LC	L53	
10	CY7C123-10DMB	D14	Military
	CY7C123-10LMB	L53	
	CY7C123-10KMB	K73	
12	CY7C123-12PC	P13A	Commercial
	CY7C123-12VC	V13	
	CY7C123-12DC	D14	
	CY7C123-12LC	L53	
	CY7C123-12DMB	D14	Military
	CY7C123-12LMB	L53	
	CY7C123-12KMB	K73	
15	CY7C123-15DMB	D14	Military
	CY7C123-15LMB	L53	
	CY7C123-15KMB	K73	

MILITARY SPECIFICATIONS
Group A Subgroup Testing

DC Characteristics

Parameters	Subgroups
V _{OH}	1, 2, 3
V _{OL}	1, 2, 3
V _{IH}	1, 2, 3
V _{IL Max.}	1, 2, 3
I _{IX}	1, 2, 3
I _{OZ}	1, 2, 3
I _{CC}	1, 2, 3

Switching Characteristics

Parameters	Subgroups
READ CYCLE	
t _{RC}	7, 8, 9, 10, 11
t _{AA}	7, 8, 9, 10, 11
t _{ACS}	7, 8, 9, 10, 11
t _{DOE}	7, 8, 9, 10, 11
WRITE CYCLE	
t _{WC}	7, 8, 9, 10, 11
t _{PWE}	7, 8, 9, 10, 11
t _{SD}	7, 8, 9, 10, 11
t _{HD}	7, 8, 9, 10, 11
t _{SA}	7, 8, 9, 10, 11
t _{HA}	7, 8, 9, 10, 11
t _{SCS}	7, 8, 9, 10, 11
t _{AW}	7, 8, 9, 10, 11

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