CY101E383

ECL/TTL/ECL Translator and High-Speed Bus Driver

Features

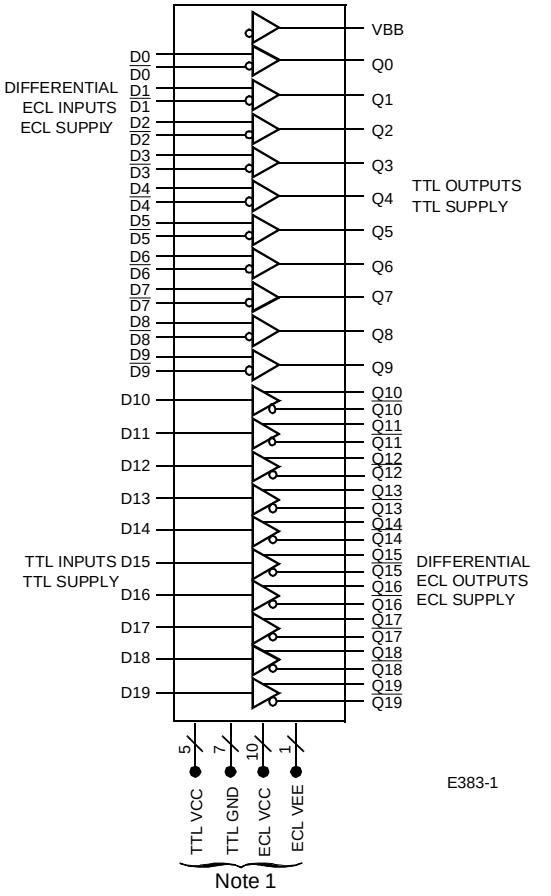
- **BiCMOS for optimum speed/power**
- **High speed (max.)**
  - **— 3.0 ns t_{PD} TTL-to-ECL**
  - **— 4 ns t_{PD} ECL-to-TTL**
- **Low skew < ± 1 ns**
- **Can operate on single +5V supply**
- **Full-duplex ECL/TTL data transmission**
- **Internal 2 kΩ ECL pull-down resistors on each ECL output**
- **80-pin PQFP package**
- **84-pin PLCC package**
- **V_{BB} ECL reference voltage output**
- **Single- or dual-supply operation**
- **Capable of greater than 2001V ESD**
- **ECL cable/twisted pair driver**

Functional Description

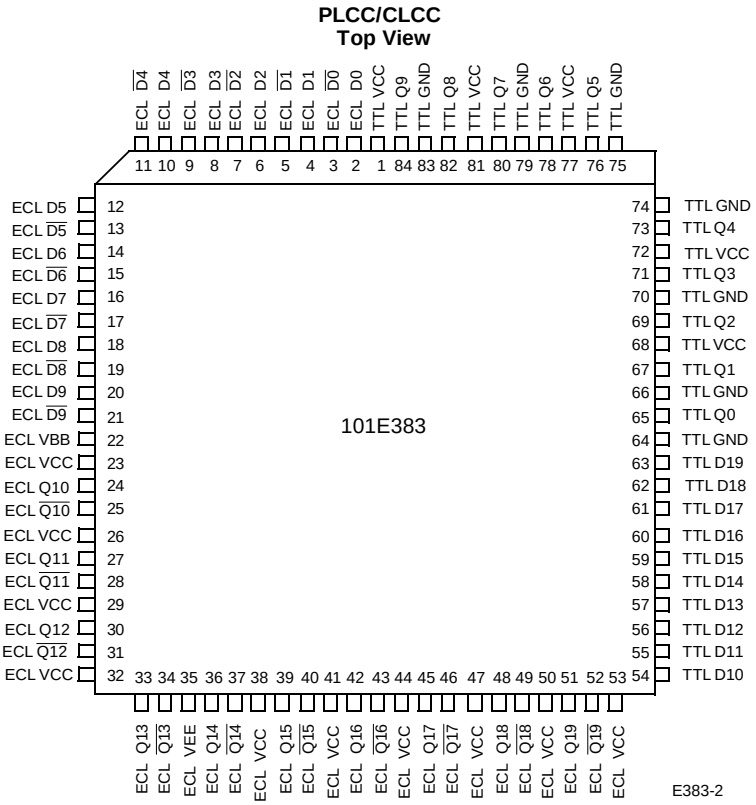
The CY101E383 is a new-generation TTL-to-ECL and ECL-to-TTL logic level translator designed for high-performance systems. The device contains ten independent TTL-to-ECL and ten independent ECL-to-TTL translators for high-speed full-duplex data transmission, mixed logic, and bus applications. The CY101E383 is especially suited to drive ECL backplanes between TTL boards. The CY101E383 is implemented with differential ECL I/O to provide balanced low noise operation over controlled impedance buses between TTL and/or ECL subsystems. In addition, the device has internal output 2 kΩ pull-down resistors tied to VEE to decrease the number of external components. For system testing purposes or for driving light loads, the 2 kΩ is used as the only termination thereby eliminating up to 20 external resistors. The part meets standard 100K logic levels with the internal pull-down while driving 50Ω to −2V.

The device is designed with ample ground pins to reduce bounce, and has separate ECL and TTL power/ground pins to reduce noise coupling between logic families. The parts can operate in single- or dual-supply configurations while maintaining absolute and 100K level swings. The translators are offered in a standard 100K ECL-compatible version with −5.2V or −4.5V power supply. The TTL I/O is fully TTL compatible. The CY101E383 is packaged in 84-pin surface-mountable PLCCs and CLCCs. To save board space, an 80-pin PQFP package with 25-mil-lead pitch is available.

Logic Block Diagram



Pin Configurations

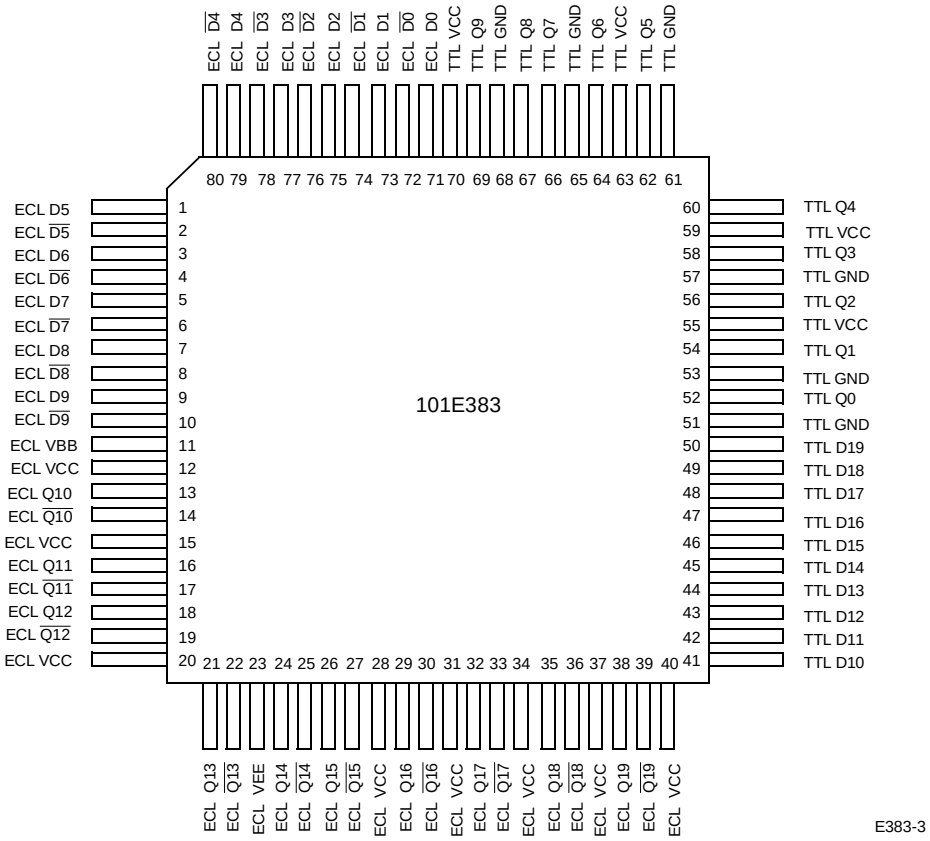


Note:

1. The PQFP package has one less each TTL V_{CC} and TTL GND pin and two less ECL V_{CC} pins.

Pin Configurations (continued)

PQFP
Top View



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Selection Guide

	101E383–3
Maximum Propagation Delay Time (ns) (TTL to ECL)	3
Maximum Propagation Delay Time (ns) (ECL to TTL)	4
Maximum Operating Current (mA) Sum of I_{EE} and I_{CC}	300

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... –65°C to +150°C

Ambient Temperature with Power Applied ..... –55°C to +125°C

TTL Supply Voltage to Ground Potential ..... –0.5V to +7.0V

TTL DC Input Voltage ..... –3.0V to +7.0V

ECL Supply Voltage V_{EE} to ECL V_{CC} ..... –7.0V to +0.5V

ECL Input Voltage ..... V_{EE} to +0.5V

ECL Output Current ..... –50 mA

Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015)

Latch-Up Current ..... >200 mA

Operating Range

Range	I/O	Version	Ambient Temperature	ECL V_{EE}	TTL V_{CC}
Commercial	100K	101E	0°C to +85°C	–4.2V to –5.46V	5V ± 5%

ECL Electrical Characteristics Over the Operating Range[2]

Parameter	Description	Test Conditions	Temperature[3]	101E383 Min.	101E383 Max.	Unit
V_{OH}	Output HIGH Voltage	101E, R_L = 50Ω to –2V V_{IN} = V_{IH} Min. or V_{IL} Max.	T_A = 0°C to 85°C	–1065	–700	mV
V_{OL}	Output LOW Voltage	101E, R_L = 50Ω to –2V V_{IN} = V_{IH} Min. or V_{IL} Max.	T_A = 0°C to 85°C	–1900	–1600	mV
V_{IH}	Input HIGH Voltage	101E	T_A = 0°C to 85°C	–1165	–700	mV
V_{IL}	Input LOW Voltage	101E	T_A = 0°C to 85°C	–1900	–1475	mV
V_{BB}	Output Reference Voltage	101E[4]	T_A = 0°C to 85°C	–1.5	–1.15	V
V_{CM}[5]	Common Mode Voltage	±V_{CM} with respect to V_{BB}			1.0	V
V_{DIFF}	Input Voltage Differential	Required for Full Output Swing		150		mV
I_{IH}	Input HIGH Current	V_{IN} = V_{IH} Max.			220	µA
I_{IL}	Input LOW Current	V_{IN} = V_{IL} Min.		–0.5	170	µA
R_{PD}	Pull-Down Resistor	Connected from All ECL Outputs to V_{EE}	T_A = 0°C to 85°C	1.6	3.0	kΩ
I_{EE}	Supply Current (All inputs and outputs open)				–180	mA

TTL Electrical Characteristics Over the Operating Range[2]

Parameter	Description	Test Conditions	101E383 Min.	101E383 Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = –3.2 mA	2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Max., I_{OL} = 16.0 mA		0.5	V
V_{IH}	Input HIGH Voltage[6]		2.0		V
V_{IL}	Input LOW Voltage[5]			0.8	V
V_{CD}	Input Clamp Diode Voltage	I_{IN} = –10 mA	–1.5		V
I_{OS}[7]	Output Short-Circuit Current	V_{CC} = Max., V_{OUT} = 0.5V[8]	–180	–40	mA
I_{IX}	Input Load Current[9]	GND ≤ V_I ≤ V_{CC}	–250	+20	µA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max., I_{OUT} = 0 mA, f = f max.		120	mA

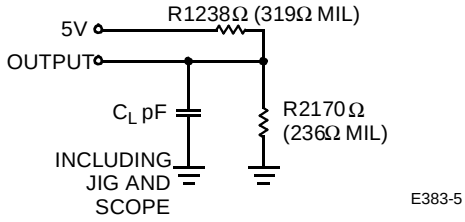
Capacitance[7]

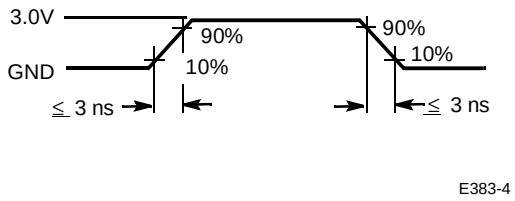
Parameter	Description	Max.	Unit
C_{IN}[7]	Input Capacitance	4	pF
C_{OUT}[7]	Output Capacitance	5	pF

Notes:

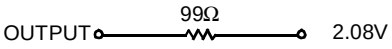
2. See AC Test Load and Waveform for test conditions.
3. Commercial grade is specified as ambient temperature with transverse air flow greater than 500 linear feet per minute.
4. Max. I_{BB} = –1 mA.
5. The internal gain of the CY101E383 guarantees that the output voltage will not change for common mode signals to ±1V. Therefore, input C_{MRR} is infinite within the common mode range.
6. These are absolute values with respect to device ground.
7. Characterized initially and after any design or process changes that may affect these parameters.
8. Not more than one output should be tested at a time. Duration of the short should not be more than one second.
9. I/O pin leakage is the worst case of I_{IX} (where X = H or L).

TTL AC Test Load and Waveform[10]

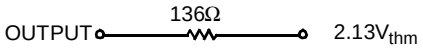




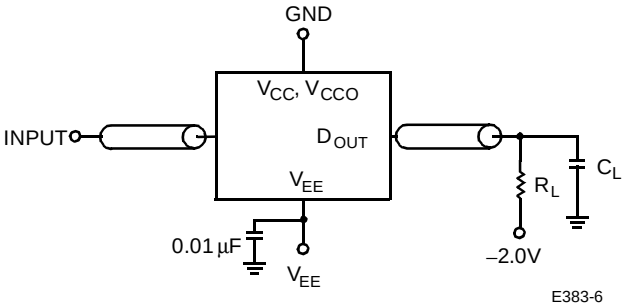
Equivalent to: THÉVENIN EQUIVALENT (Commercial)

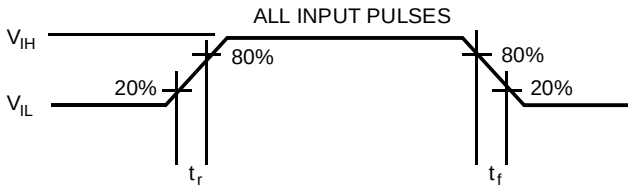


THÉVENIN EQUIVALENT (Military)



ECL AC Test Load and Waveform[11, 12, 13, 14, 15]





ECL-to-TTL Switching Characteristics Over the Operating Range

Parameter	Description	Test Conditions	101E383–3		Unit
			Min.	Max.	
t_{PLH}	Propagation Delay Time	D_n, $\overline{D}_n$ to Q_n	1	4	ns
t_{PHL}	Propagation Delay Time	D_n, $\overline{D}_n$ to Q_n	1	4	ns

TTL-to-ECL Switching Characteristics Over the Operating Range

Parameter	Description	Test Conditions	101E383–3		Unit
			Min.	Max.	
t_{PLH}	Propagation Delay Time	D_n to Q_n, $\overline{Q}_n$	1	3	ns
t_{PHL}	Propagation Delay Time	D_n to Q_n, $\overline{Q}_n$	1	3	ns
t_R[7]	Output Rise Time	20% to 80%	0.35	1.7	ns
t_R[7]	Output Fall Time	20% to 80%	0.35	1.7	ns

Skew Time Switching Characteristics[7] (Same test conditions as TTL-to-ECL and ECL-to-TTL Electrical Characteristics)

Symbol	Characteristic	Test Conditions	Min.	Max.	Unit
t_{SKT}[7]	Data Skew Time ECL-to-TTL	$TTLQ_n$ to $TTLQ_{n+m}$		1	ns
t_{SKE}[7]	Data Skew Time TTL-to-ECL	$ECLQ_n$, $\overline{Q}_n$ to $ECLQ_{n+m}$, $\overline{Q}_{n+m}$		1	ns

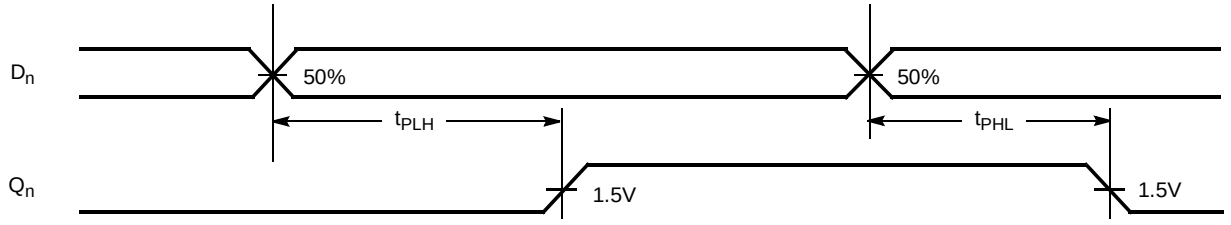
Skew Time Switching Characteristics[7] (Same test conditions as TTL-to-ECL and ECL-to-TTL Electrical Characteristics)

Symbol	Characteristic	Test Conditions	Min.	Max.	Unit

10. TTL test conditions assume signal transition times of 3 ns or less, timing reference levels of 1.5 V, input pulse levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH}, and C_L = 10 pF.
11. V_{IL}=–1.7V, V_{IH}=–0.9V.
12. ECL R_L = 50Ω, C_L < 5 pF (includes fixture and stray capacitance).
13. All coaxial cables should be 50Ω with equal lengths. The delay of the coaxial cables should be “nulled” out of the measurement.
14. $t_r = t_f$ = 0.7 ns
15. All timing measurements are made from the 50% point of all waveforms.

Switching Waveforms

ECL-to-TTL Timing



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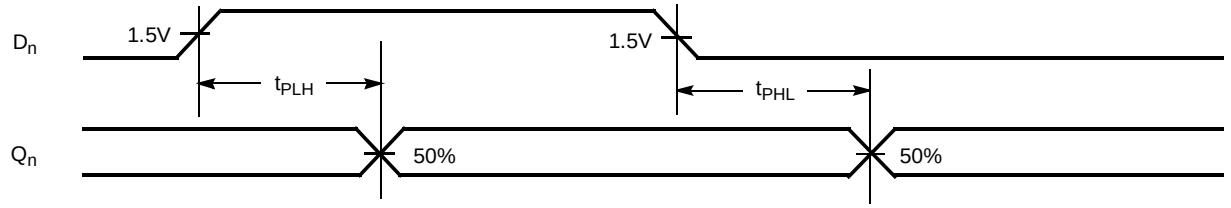
TTL-to-ECL Timing



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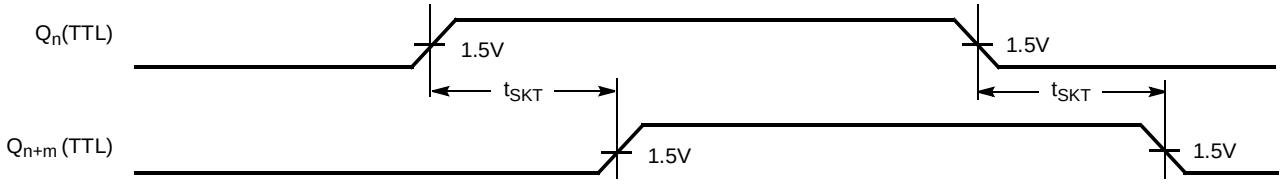
Skew Test (t_{SKT}) TTL_{An}-to-TTL_{Qn+m}



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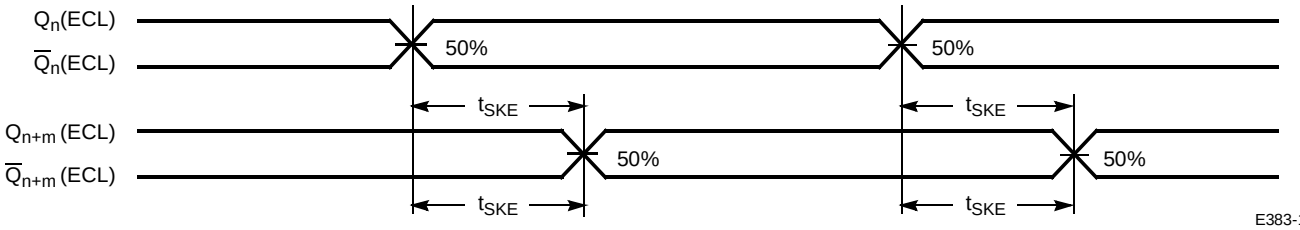
Skew Test (t_{SKE}) ECL_{Qn}, $\overline{Q}_n$-to-ECL_{Qn+m}, $\overline{Q}_{n+m}$



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ECL-to-TTL Truth Table

Inputs		Outputs
ECL D_n	ECL $\overline{D}_n$	TTL Q_n
Open[16]	Open[16]	L
L	H	L
H	L	H

TTL-to-ECL Truth Table

Inputs	Outputs	
TTL D_n	ECL Q_n	ECL $\overline{Q}_n$
L	L	H
H	H	L

Nominal Voltages

The CY101E383 can be used in dual ±5V or single +5V supply systems. The supply pins should be connected as shown in *Tables 1* and 2. This connection technique involves shifting up all ECL supply pins by 5V. When operating in single-supply systems, the ECL termination voltage level must also be shifted up by adding 5V. For example, if the termination is 50 ohms to –2V in a dual-supply system, the single +5V system should have 50 ohms to +3V. If the termination is a thévenin type, then the resistor tied to ground is now at +5V and the resistor tied to –5V is now at ground potential. Consideration should be given to the power supply so that adequate bypassing is made to isolate the ECL output switching noise from the supply. Having separate TTL and ECL +5V supply lines will help to reduce the noise.

Table 1. CY101E383 Nominal Voltages Applied in 100K System

Supply Pin	Single-Supply System	Dual-Supply System
TTL V_{CC}	+5.0V	+5.0V
TTL GND	0.0V	0.0V
ECL V_{CC}	+5.0V	0.0V
ECL V_{EE}	0.0V	–4.5V

Table 2. CY101E383 Nominal Voltages Applied in 101K System

Supply Pin	Single-Supply System	Dual-Supply System
TTL V_{CC}	+5.0V	+5.0V
TTL GND	0.0V	0.0V
ECL V_{CC}	+5.0V	0.0V
ECL V_{EE}	0.0V	–5.2V

Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
3	CY101E383–3JC	J83	84-Lead Plastic Leaded Chip Carrier	Commercial
	CY101E383–3NC	N80	80-Lead Plastic Quad Flatpack	

Note:
16. The ECL inputs will pull to a known logic level if left open.

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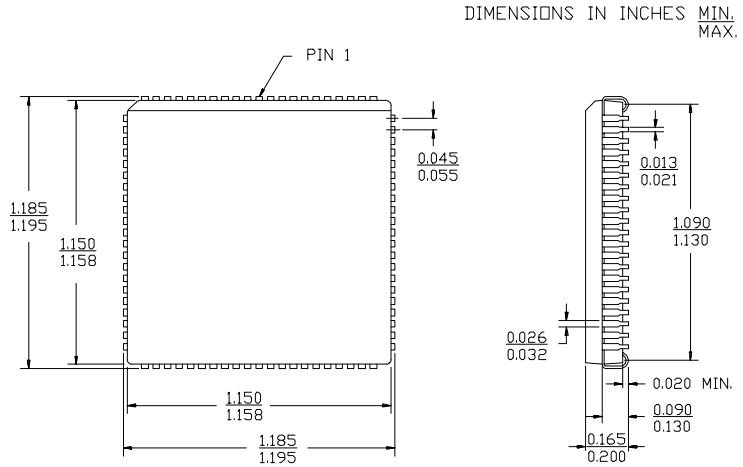
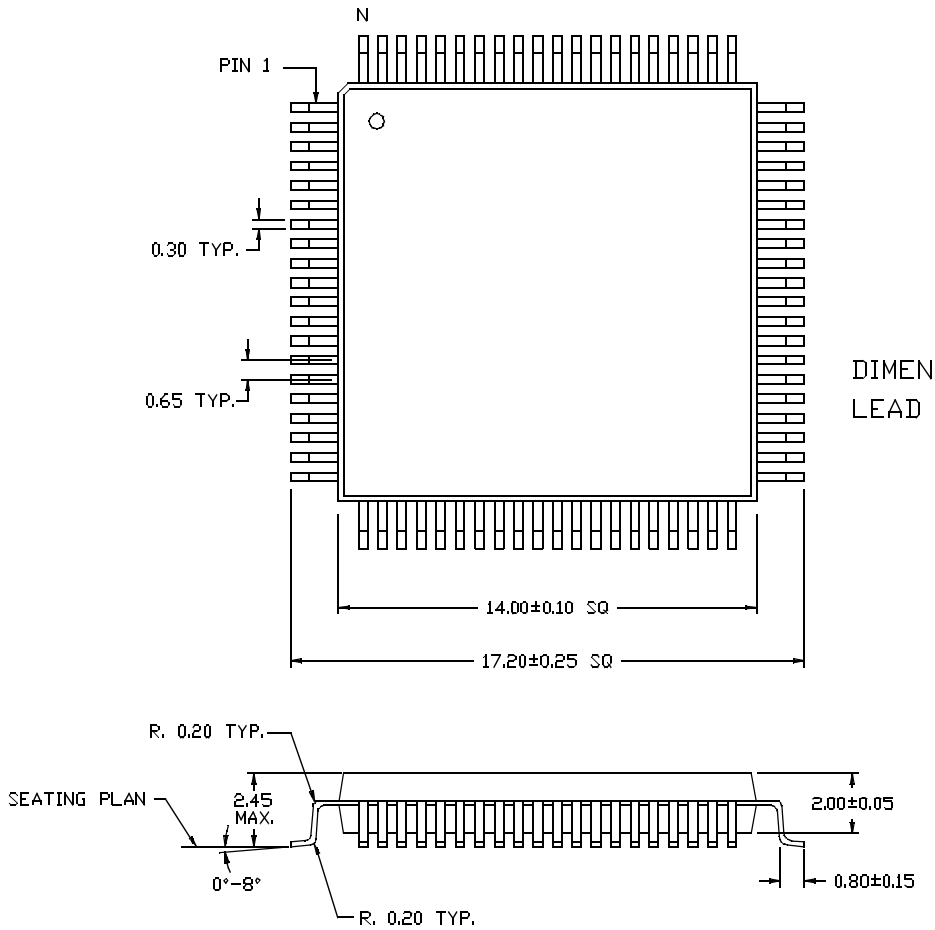
Package Diagrams

84-Lead Plastic Leaded Chip Carrier J83



Package Diagrams (continued)

80-Lead Plastic Quad Flatpack N80



DIMENSIONS ARE IN MILLIMETERS
LEAD COPLANARITY 0.102 MAX.

Package Diagrams (continued)

84-Pin Ceramic Leaded Chip Carrier Y84