



CY54/74FCT240T CY54/74FCT244T

8-Bit Buffers/Line Drivers

Features

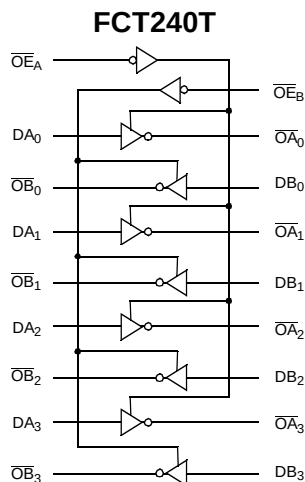
- Function, pinout, and drive compatible with FCT and F logic
- FCT-D speed at 3.6 ns max. (Com'I), FCT-C speed at 4.1 ns max. (Com'I)
- Reduced V_{OH} (typically = 3.3V) versions of equivalent FCT functions
- Edge-rate control circuitry for significantly improved noise characteristics
- Power-off disable feature
- ESD > 2000V
- Matched rise and fall times
- Fully compatible with TTL input and output logic levels
- Extended commercial range of -40°C to $+85^{\circ}\text{C}$
- Sink current 64 mA (Com'I), 48 mA (Mil)
Source current 32 mA (Com'I), 12 mA (Mil)

Functional Description

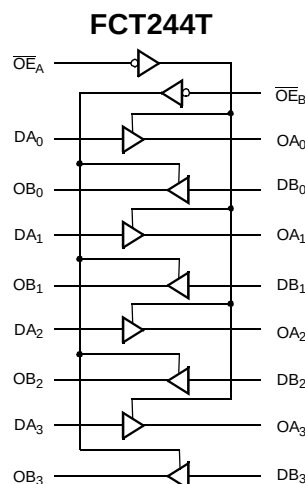
The FCT240T and FCT244T are octal buffers and line drivers designed to be employed as memory address drivers, clock drivers, and bus-oriented transmitters/receivers. The devices provide speed and drive capabilities equivalent to their fastest bipolar logic counterparts while reducing power consumption. The input and output voltage levels allow direct interface with TTL, NMOS, and CMOS devices without external components.

The outputs are designed with a power-off disable feature to allow for live insertion of boards.

Logic Block Diagram

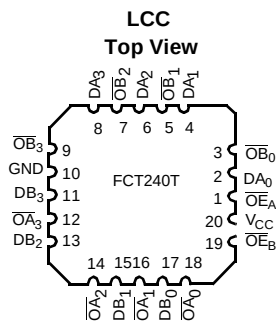


FCT240T-1

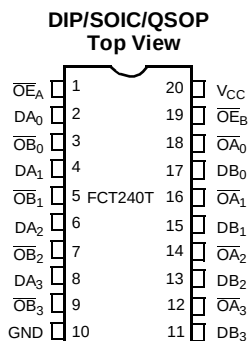


FCT240T-4

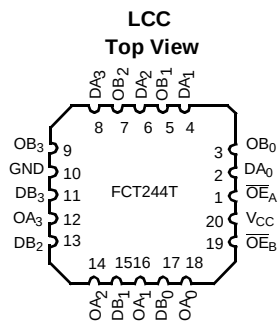
Pin Configurations



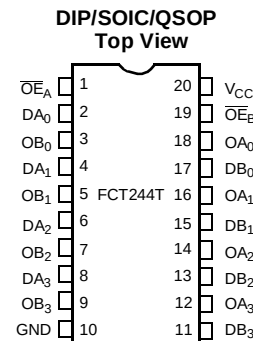
FCT240T-2



FCT240T-3



FCT240T-5



FCT240T-6



Function Table FCT240T^[1]

Inputs			Output
$\overline{OE}_A$	$\overline{OE}_B$	D	
L	L	L	H
L	L	H	L
H	H	X	Z

Maximum Ratings^[2, 3]

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature -65°C to +150°C

Ambient Temperature with

Power Applied..... -65°C to +135°C

Supply Voltage to Ground Potential -0.5V to +7.0V

DC Input Voltage..... -0.5V to +7.0V

DC Output Voltage..... -0.5V to +7.0V

DC Output Current (Maximum Sink Current/Pin)..... 120 mA

Function Table FCT244T^[1]

Inputs			Output
$\overline{OE}_A$	$\overline{OE}_B$	D	
L	L	L	L
L	L	H	H
H	H	X	Z

Power Dissipation..... 0.5W

Static Discharge Voltage >2001V
(per MIL-STD-883, Method 3015)

Operating Range

Range	Speed	Ambient Temperature	V _{CC}
Commercial	DT	0°C to +70°C	5V ± 5%
Commercial	T, AT, CT	-40°C to +85°C	5V ± 5%
Military ^[4]	All	-55°C to +125°C	5V ± 10%

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions		Min.	Typ. ^[5]	Max.	Unit
V _{OH}	Output HIGH Voltage	V _{CC} =Min., I _{OH} =-32 mA	Com'l	2.0			V
		V _{CC} =Min., I _{OH} =-15 mA	Com'l	2.4	3.3		V
		V _{CC} =Min., I _{OH} =-12 mA	Mil	2.4	3.3		V
V _{OL}	Output LOW Voltage	V _{CC} =Min., I _{OL} =64 mA	Com'l		0.3	0.55	V
		V _{CC} =Min., I _{OL} =48mA	Mil		0.3	0.55	V
V _{IH}	Input HIGH Voltage			2.0			V
V _{IL}	Input LOW Voltage					0.8	V
V _H	Hysteresis ^[6]	All inputs			0.2		V
V _{IK}	Input Clamp Diode Voltage	V _{CC} =Min., I _{IN} =-18 mA			-0.7	-1.2	V
I _I	Input HIGH Current	V _{CC} =Max., V _{IN} =V _{CC}				5	μA
I _{IH}	Input HIGH Current	V _{CC} =Max., V _{IN} =2.7V				±1	μA
I _{IL}	Input LOW Current	V _{CC} =Max., V _{IN} =0.5V				±1	μA
I _{OZH}	Off State HIGH-Level Output Current	V _{CC} = Max., V _{OUT} = 2.7V				10	μA
I _{OZL}	Off State LOW-Level Output Current	V _{CC} = Max., V _{OUT} = 0.5V				-10	μA
I _{OS}	Output Short Circuit Current ^[7]	V _{CC} =Max., V _{OUT} =0.0V		-60	-120	-225	mA
I _{OFF}	Power-Off Disable	V _{CC} =0V, V _{OUT} =4.5V				±1	μA

Notes:

1. H = HIGH Voltage Level. L = LOW Voltage Level. X = Don't Care.
2. Unless otherwise noted, these limits are over the operating free-air temperature range.
3. Unused inputs must always be connected to an appropriate logic voltage level, preferably either V_{CC} or ground.
4. T_A is the "instant on" case temperature.
5. Typical values are at V_{CC}=5.0V, T_A=+25°C ambient.
6. This parameter is guaranteed but not tested.
7. Not more than one output should be shorted at a time. Duration of short should not exceed one second. The use of high-speed test apparatus and/or sample and hold techniques are preferable in order to minimize internal chip heating and more accurately reflect operational values. Otherwise prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parametric tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

Capacitance^[6]

Parameter	Description	Typ. ^[5]	Max.	Unit
C _{IN}	Input Capacitance	5	10	pF
C _{OUT}	Output Capacitance	9	12	pF

Power Supply Characteristics

Parameter	Description	Test Conditions	Typ. ^[5]	Max.	Unit
I _{CC}	Quiescent Power Supply Current	V _{CC} =Max., V _{IN} ≤0.2V, V _{IN} ≥V _{CC} -0.2V	0.1	0.2	mA
ΔI _{CC}	Quiescent Power Supply Current (TTL inputs)	V _{CC} =Max., V _{IN} =3.4V, ^[8] f ₁ =0, Outputs Open	0.5	2.0	mA
I _{CCD}	Dynamic Power Supply Current ^[9]	V _{CC} =Max., One Input Toggling, 50% Duty Cycle, Outputs Open, $\overline{OE}_1=\overline{OE}_2=GND$, V _{IN} ≤0.2V or V _{IN} ≥V _{CC} -0.2V	0.06	0.12	mA/MHz
I _C	Total Power Supply Current ^[10]	V _{CC} =Max., 50% Duty Cycle, Outputs Open, One Bit Toggling at f ₁ =10 MHz, $\overline{OE}_1=\overline{OE}_2=GND$, V _{IN} ≤0.2V or V _{IN} ≥V _{CC} -0.2V	0.7	1.4	mA
		V _{CC} =Max., 50% Duty Cycle, Outputs Open, One Bit Toggling at f ₁ =10 MHz, $\overline{OE}_1=\overline{OE}_2=GND$, V _{IN} =3.4V or V _{IN} =GND	1.0	2.4	mA
		V _{CC} =Max., 50% Duty Cycle, Outputs Open, Eight Bits Toggling at f ₁ =2.5 MHz, $\overline{OE}_1=\overline{OE}_2=GND$, V _{IN} ≤0.2V or V _{IN} ≥V _{CC} -0.2V	1.3	2.6 ^[11]	mA
		V _{CC} =Max., 50% Duty Cycle, Outputs Open, Eight Bits Toggling at f ₁ =2.5 MHz, $\overline{OE}_1=\overline{OE}_2=GND$, V _{IN} =3.4V or V _{IN} =GND	3.3	10.6 ^[11]	mA

Notes:

8. Per TTL driven input (V_{IN}=3.4V); all other inputs at V_{CC} or GND.
9. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
10. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
 $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_0/2 + f_1 N_1)$
 I_{CC} = Quiescent Current with CMOS input levels
 ΔI_{CC} = Power Supply Current for a TTL HIGH input (V_{IN}=3.4V)
 D_H = Duty Cycle for TTL inputs HIGH
 N_T = Number of TTL inputs at D_H
 I_{CCD} = Dynamic Current caused by an input transition pair (HLH or LHL)
 f_0 = Clock frequency for registered devices, otherwise zero
 f_1 = Input signal frequency
 N_1 = Number of inputs changing at f₁
 All currents are in milliamps and all frequencies are in megahertz.
11. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.

Switching Characteristics Over the Operating Range

Parameter	Description	FCT240T				FCT240AT				Unit	Fig. No. ^[13]
		Military		Commercial		Military		Commercial			
		Min. ^[12]	Max.	Min. ^[12]	Max.	Min. ^[12]	Max.	Min. ^[12]	Max.		
t _{PLH} t _{PHL}	Propagation Delay Data to Input	1.5	9.0	1.5	8.0	1.5	5.1	1.5	4.8	ns	1, 2
t _{PZH} t _{PZL}	Output Enable Time	1.5	10.5	1.5	10.0	1.5	6.5	1.5	6.2	ns	1, 7, 8
t _{PHZ} t _{PLZ}	Output Disable Time	1.5	10.0	1.5	9.5	1.5	5.9	1.5	5.6	ns	1, 7, 8

Parameter	Description	FCT240CT				FCT240DT		Unit	Fig. No. ^[13]
		Military		Commercial		Commercial			
		Min. ^[12]	Max.	Min. ^[12]	Max.	Min. ^[12]	Max.		
t _{PLH} t _{PHL}	Propagation Delay Data to Input	1.5	4.7	1.5	4.3	1.5	3.6	ns	1, 2
t _{PZH} t _{PZL}	Output Enable Time	1.5	5.7	1.5	5.0	1.5	4.8	ns	1, 7, 8
t _{PHZ} t _{PLZ}	Output Disable Time	1.5	4.6	1.5	4.5	1.5	4.0	ns	1, 7, 8

Parameter	Description	FCT244T				FCT244AT				Unit	Fig. No. ^[13]
		Military		Commercial		Military		Commercial			
		Min. ^[12]	Max.	Min. ^[12]	Max.	Min. ^[12]	Max.	Min. ^[12]	Max.		
t _{PLH} t _{PHL}	Propagation Delay Data to Input	1.5	7.0	1.5	6.5	1.5	5.1	1.5	4.6	ns	1, 3
t _{PZH} t _{PZL}	Output Enable Time	1.5	8.5	1.5	8.0	1.5	6.5	1.5	6.2	ns	1, 7, 8
t _{PHZ} t _{PLZ}	Output Disable Time	1.5	7.5	1.5	7.0	1.5	5.9	1.5	5.6	ns	1, 7, 8

Parameter	Description	FCT244CT				FCT244DT		Unit	Fig. No. ^[13]
		Military		Commercial		Commercial			
		Min. ^[12]	Max.	Min. ^[12]	Max.	Min. ^[12]	Max.		
t _{PLH} t _{PHL}	Propagation Delay Data to Input	1.5	4.6	1.5	4.1	1.5	3.6	ns	1, 3
t _{PZH} t _{PZL}	Output Enable Time	1.5	6.5	1.5	5.8	1.5	4.8	ns	1, 7, 8
t _{PHZ} t _{PLZ}	Output Disable Time	1.5	5.7	1.5	5.2	1.5	4.0	ns	1, 7, 8

Shaded areas contain preliminary information.

Notes:

12. Minimum limits are guaranteed but not tested on Propagation Delays.

13. See "Parameter Measurement Information" in the General Information section.



Ordering Information—FCT240T

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
3.6	CY74FCT240DTQC	Q5	20-Lead (150-Mil) QSOP	Commercial
	CY74FCT240DTSOC	S5	20-Lead (300-Mil) Molded SOIC	
4.3	CY74FCT240CTSOC	S5	20-Lead (300-Mil) Molded SOIC	Commercial
	CY74FCT240CTQC	Q5	20-Lead (150-Mil) QSOP	
4.8	CY74FCT240ATPC	P5	20-Lead (300-Mil) Molded DIP	Commercial
	CY74FCT240ATSOC	S5	20-Lead (300-Mil) Molded SOIC	
	CY74FCT240ATQC	Q5	20-Lead (150-Mil) QSOP	
5.1	CY54FCT240ATDMB	D6	20-Lead (300-Mil) CerDIP	Military
8.0	CY74FCT240TSOC	S5	20-Lead (300-Mil) Molded SOIC	Commercial
	CY74FCT240TQC	Q5	20-Lead (150-Mil) QSOP	
9.0	CY54FCT240TDMB	D6	20-Lead (300-Mil) CerDIP	Military

Ordering Information—FCT244T

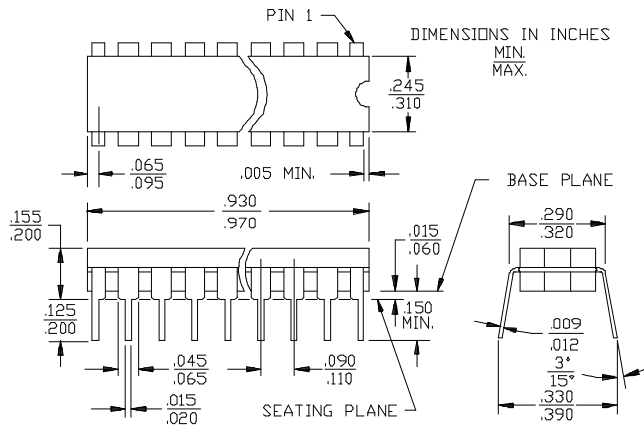
Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
3.6	CY74FCT244DTQC	Q5	20-Lead (150-Mil) QSOP	Commercial
	CY74FCT244DTSOC	S5	20-Lead (300-Mil) Molded SOIC	
4.1	CY74FCT244CTSOC	S5	20-Lead (300-Mil) Molded SOIC	Commercial
	CY74FCT244CTQC	Q5	20-Lead (150-Mil) QSOP	
4.6	CY54FCT244CTDMB	D6	20-Lead (300-Mil) CerDIP	Military
4.6	CY74FCT244ATPC	P5	20-Lead (300-Mil) Molded DIP	Commercial
	CY74FCT244ATSOC	S5	20-Lead (300-Mil) Molded SOIC	
	CY74FCT244ATQC	Q5	20-Lead (150-Mil) QSOP	
5.1	CY54FCT244ATDMB	D6	20-Lead (300-Mil) CerDIP	Military
	CY54FCT244ATLMB	L61	20-Pin Square Leadless Chip Carrier	
6.5	CY74FCT244TSOC	S5	20-Lead (300-Mil) Molded SOIC	Commercial
	CY74FCT244TQC	Q5	20-Lead (150-Mil) QSOP	
7.0	CY54FCT244TDMB	D6	20-Lead (300-Mil) CerDIP	Military
	CY54FCT244TLMB	L61	20-Pin Square Leadless Chip Carrier	

Shaded areas contain preliminary information.

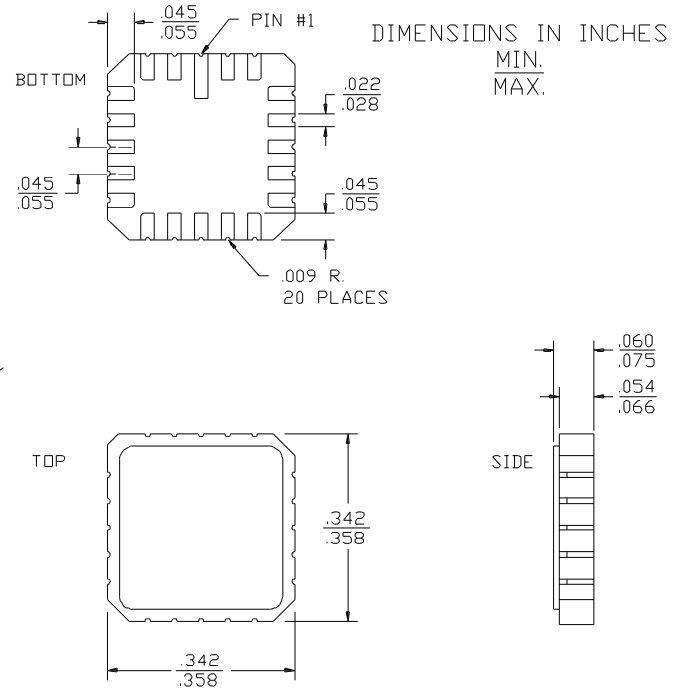
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Package Diagrams

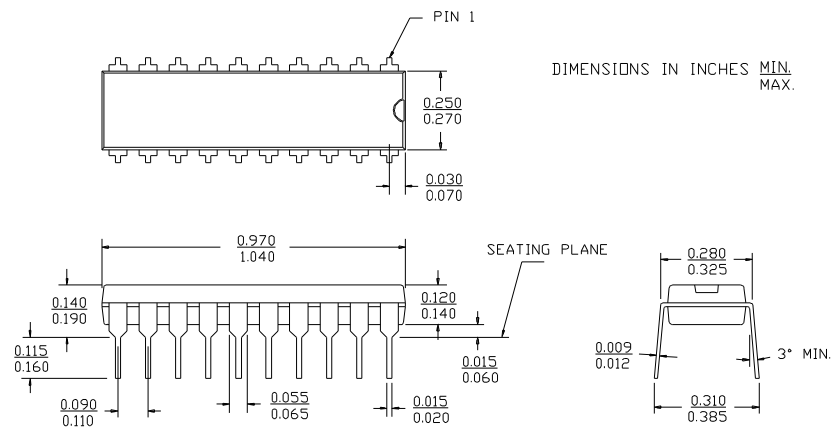
20-Lead (300-Mil) CerDIP D6
MIL-STD-1835 D-8 Config.A



20-Pin Square Leadless Chip Carrier L61
MIL-STD-1835 C-2A

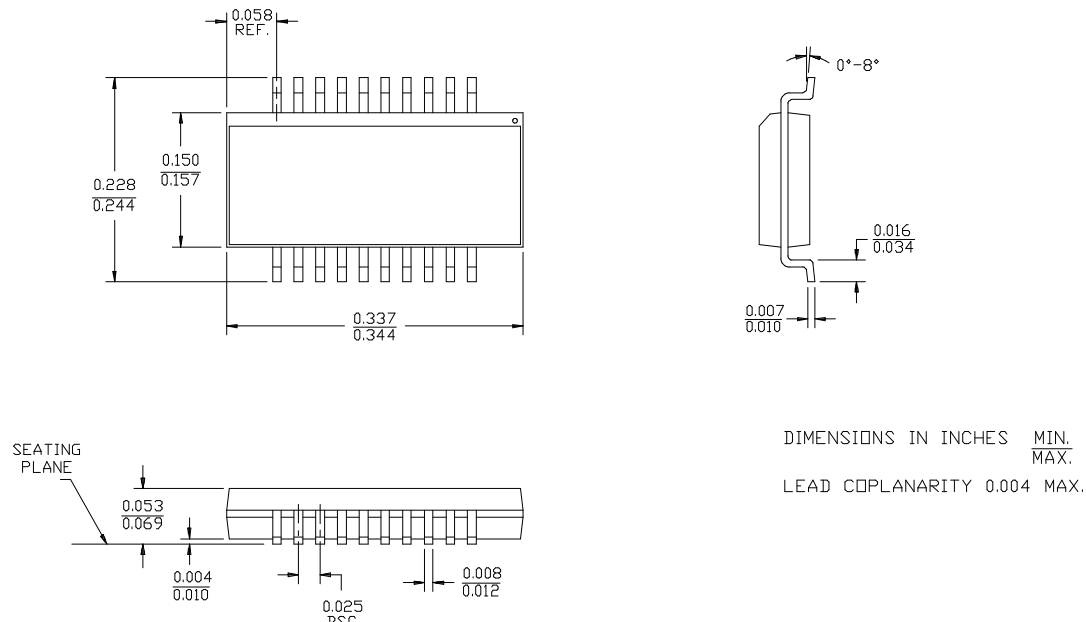


20-Lead (300-Mil) Molded DIP P5



Package Diagrams (continued)

20-Lead Quarter Size Outline Q5



20-Lead (300-Mil) Molded SOIC S5

