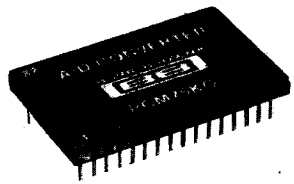
BURR-BROWN®



PCM75
DESIGNED FOR AUDIO

16-Bit Hybrid ANALOG-TO-DIGITAL CONVERTER

FEATURES

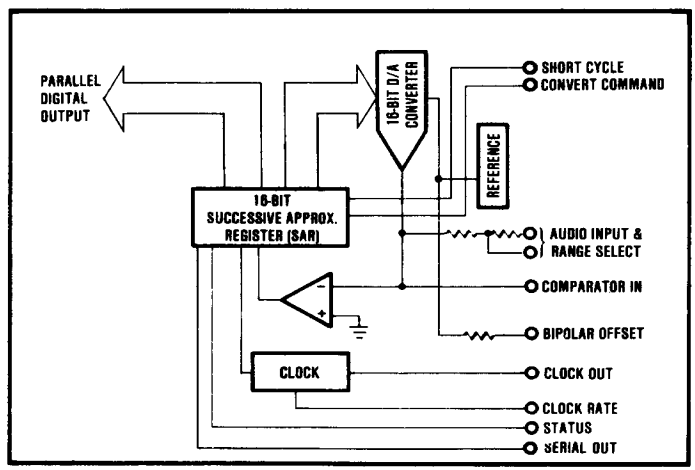
- 16-BIT RESOLUTION
- 90dB DYNAMIC RANGE
- 0.004% THD (FS Input, 16 Bits)
- 0.02% MAX THD (-15dB, 16 Bits)
- 17μs MAX CONVERSION TIME (16 Bits)
- 15μs MAX CONVERSION TIME (14 Bits)
- 10μs CONVERSION TIME (Reduced Specs)
- EIAJ STC-007-COMPATIBLE

DESCRIPTION

The PCM75 is a low cost, high quality, 16-bit successive approximation analog-to-digital converter. The PCM75 uses state-of-the-art IC and laser-trimmed thin-film components and is packaged in a bottom-brazed ceramic 32-pin dual-in-line package. The converter is complete with internal reference and clock.

The PCM75 is designed for PCM audio applications and is compatible with EIAJ STC-007 specifications.

The conversion time can be reduced from 15μs to 10μs with some increase in distortion. Distortion is specified on the data sheet to assure performance in critical audio applications.



International Airport Industrial Park · P.O. Box 11400 · Tucson, Arizona 85734 · Tel. (602) 746-1111 · Twx: 910-952-1111 · Cable: BBRCORP · Telex: 66-6491

PDS-624A

SPECIFICATIONS

ELECTRICAL

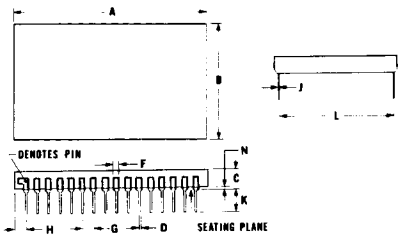
At 25°C and rated power supplies unless otherwise noted.

MODEL	PCM75KG			PCM76JG			UNITS
	MIN	TYP	MAX	MIN	TYP	MAX	
RESOLUTION			16			*	Bits
DYNAMIC RANGE[1]		90			*		dB
INPUT							
ANALOG							
Voltage Ranges, Bipolar		±2.5, ±5, ±10			*		V
Impedance (Direct Input)							
0 to +5V, ±2.5V		2.5			*		kΩ
0 to +10V, ±5V		5			*		kΩ
0 to +20V, ±10V		10			*		kΩ
DIGITAL[2]							
Convert Command		Positive pulse 50ns wide (min) trailing edge ("1" to "0" initiates conversion)					
Logic Loading			1			*	TTL Load
TRANSFER CHARACTERISTICS							
ACCURACY							
Gain Error		±0.1[3]			*		%
Offset Error, Bipolar		±0.1[3]			*		% of FSR[4]
Differential Linearity Error (major carry)		±0.0015			±0.003		% of FSR
Inherent Quantization Error		±1/2			*		LSB
TOTAL HARMONIC DISTORTION + NOISE[1,5]							
V_{IN} = ±FS at f = 400Hz							
14-Bit Resolution		0.006			0.008		%
16-Bit Resolution		0.004			0.006		%
V_{IN} = −15dB at f = 400Hz							
14-Bit Resolution		0.025			0.03	0.05	%
16-Bit Resolution		0.015	0.02		0.021		%
POWER SUPPLY SENSITIVITY							
±15VDC		0.003			*		% of FSR/%V_S
+5VDC		0.001			*		% of FSR/%V_S
CONVERSION TIME[6]							
14 Bits			15			*	μs
16 Bits			17				μs
WARM-UP TIME	5			*			min
DRIFT							
Gain			±20			*	ppm/°C
Offset, Bipolar			±15			*	ppm of FSR/°C
OUTPUT							
DIGITAL (all codes complementary)							
Parallel							
Bipolar Output Codes[8]		COB, CTC[7]			*		
Output Drive	2			*			TTL Loads
Serial Data Code (NRZ)		CSB, COB			*		
Output Drive			2			*	TTL Loads
Status		Logic "1" during conversion			*		
Status Output Drive	2			*			TTL Loads
Internal Clock: Output Drive	2			*			TTL Loads
Frequency[8]		933			*		kHz
POWER SUPPLY REQUIREMENTS							
Power Consumption		0.525			*		W
Rated Voltage: Analog	±14.5	±15	±15.5	*	*	*	VDC
Digital	+4.75	+5	+5.25	*	*	*	VDC
Supply Drain: +15VDC		+14			*		mA
−15VDC		−17			*		mA
+5VDC		+10			*		mA
TEMPERATURE RANGE							
Specification	0		+70	*		*	°C
Operating (derated specs)	−25		+85	*		*	°C
Storage	−55		+100	*		*	°C

*Specification same as PCM75KG.

NOTES: (1) The measurement of Total Harmonic Distortion + Noise (THD+N) and Dynamic Range is highly dependent on the characteristics of the sample/hold amplifier, the digital-to-analog converter, the deglitcher, and the low-pass filter. To accurately measure THD+N and Dynamic Range, the accuracy of each device should be better than 16-bit accuracy. A block diagram showing the measurement technique Burr-Brown uses is shown in Figure 6. (2) DTL/TTL compatible, i.e., Logic "0" = 0.8V max. Logic "1" = 2.0V min for inputs. For digital outputs Logic "0" = +0.4V max. Logic "1" = 2.4V min. (3) Adjustable to zero. (see "Optional External Gain and Offset Adjustment.") (4) FSR means Full Scale Range. For example, unit connected for ±10V range has 20V FSR. (5) Conversion time may be shortened with "Short Cycle" set for lower resolution and with use of Clock Rate Control. See "Additional Optional Connections" section. The Clock Rate Control (pin 23) should be connected to Digital Common for specified max conversion time. Short Cycle (pin 32) should be left open for 16-bit resolution or connected to the n + 1 digital output for n-bit resolution. For example, connect Short Cycle to bit 15 (pin 15) for 14-bit resolution. (6) See Table I. CSB—Complementary Straight Binary, COB—Complementary Offset Binary, CTC—Complementary Two's Complement. (7) CTC coding obtained by inverting MSB (pin 1). (8) Adjustable with Clock Rate Control from approximately 933kHz to 1.4MHz. See Figures 14 and 15 and Table III.

MECHANICAL



Pin numbers shown for reference only. Numbers may not be marked on package.

CASE: Ceramic

WEIGHT: 13 grams (0.46oz.)

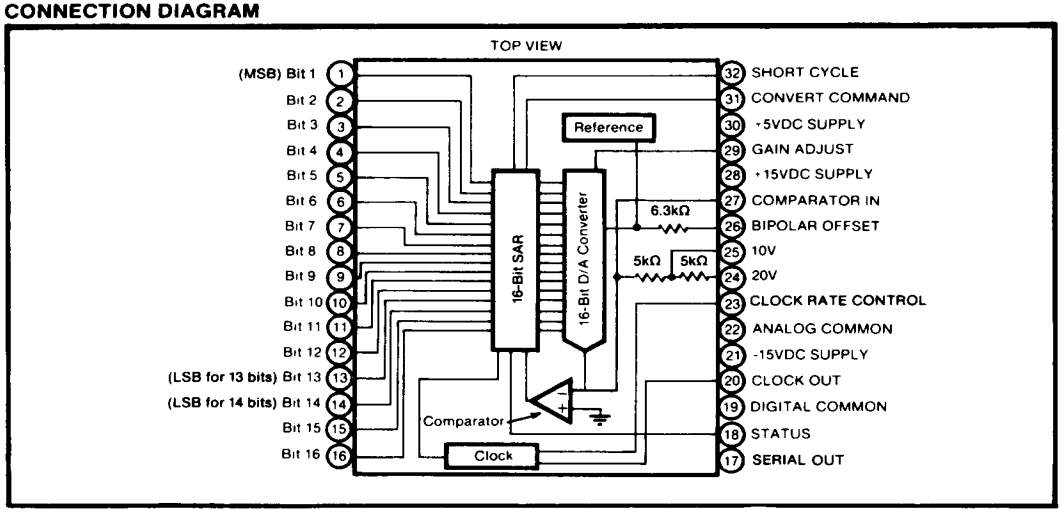
HERMETICITY:

Conforms to method 1014 condition C step 1 (fluorocarbon) of MIL-STD-883 (gross leak).

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	1.678	1.712	42.62	43.48
B	1.079	1.101	27.41	27.97
C	180	.210	4.57	5.33
D	.016	.020	.41	.51
F	.045	.055	1.14	1.40
G	100 BASIC		2.54 BASIC	
H	.089	.106	2.26	2.69
J	.009	.012	.23	.30
K	.200	.210	5.08	5.33
L	.900 BASIC		22.86 BASIC	
N	.015	.035	.38	.89

LEADS IN TRUE POSITION WITHIN .010" (.25 MM) R @ MMC AT SEATING PLANE

CONNECTION DIAGRAM



THEORY OF OPERATION

The accuracy of a successive-approximation A/D converter is described by the transfer function shown in Figure 1. All successive-approximation A/D converters have an inherent Quantization Error ±1/2LSB. The remaining errors in the A/D converters are combinations of analog errors due to the linear circuitry, matching and tracking properties of the ladder and scaling networks, power supply rejection, and reference errors. In summary, these errors consist of initial errors including Gain, Offset, Linearity, Differential Linearity, and Power Supply Sensitivity. Initial Gain and Offset errors may be adjusted to zero. Gain drift over temperature rotates the line (Figure 1) about the zero or minus full scale point (all bits Off), and Offset drift shifts the line left or right over the operating temperature range. Total Harmonic Distortion (THD) is a measure of the magnitude and distribution of the Linearity Error, Differential Linearity Error, and Noise, as well as Quantization Error, that is useful in Audio Applications. To be useful, THD should be specified for both high level and low level input

signals. This error is unadjustable and is the most meaningful indicator of A/D converter accuracy for Audio Applications. The resolution of an A/D converter can be expressed in terms of Dynamic Range. The Dynamic Range is a measure of the ratio of the smallest signals the converter can resolve to the full scale range and is usually expressed in decibels (dB). The theoretical dynamic range of a converter is approximately 6 x n, where n is the number of bits of resolution, or 96dB for a 16-bit converter. The actual or useful dynamic range is limited by noise and linearity errors and is therefore somewhat less than the theoretical limit.

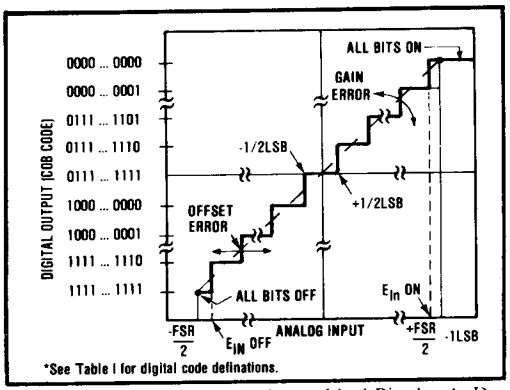


FIGURE 1. Input vs Output for an Ideal Bipolar A/D Converter.

TIMING CONSIDERATIONS

The timing diagram in Figure 2 assumes an analog input such that the positive true digital word 1001 1000 1001 0110 exists. The output will be complementary as shown in Figure 2 (0110 0111 0110 1001 is the digital output). Figures 3 and 4 are timing diagrams showing the relationship of serial data to clock and valid data to status.

DEFINITION OF DIGITAL CODES

Parallel Data

Two binary codes are available on the PCM75 parallel output; they are complementary (logic "0" is true) straight binary (CSB) for unipolar input signal ranges and complementary offset binary (COB) for bipolar input signal ranges. Complementary two's complement (CTC) may be obtained by inverting MSB (pin1).

Table I shows the LSB, transition values, and code definitions for each possible analog input signal range for 14-, 15- and 16-bit resolutions. Figure 5 shows the connections for 14-bit resolution, parallel data output, with ±5V input.

Serial Data

Two straight binary (complementary) codes are available on the serial output line; they are CSB and COB. The serial data is available only during conversion and appears with MSB occurring first. The serial data is synchronous with the internal clock as shown in the timing diagram of Figure 2. The LSB and transition values shown in Table I also apply to the serial data output except for the CTC code.

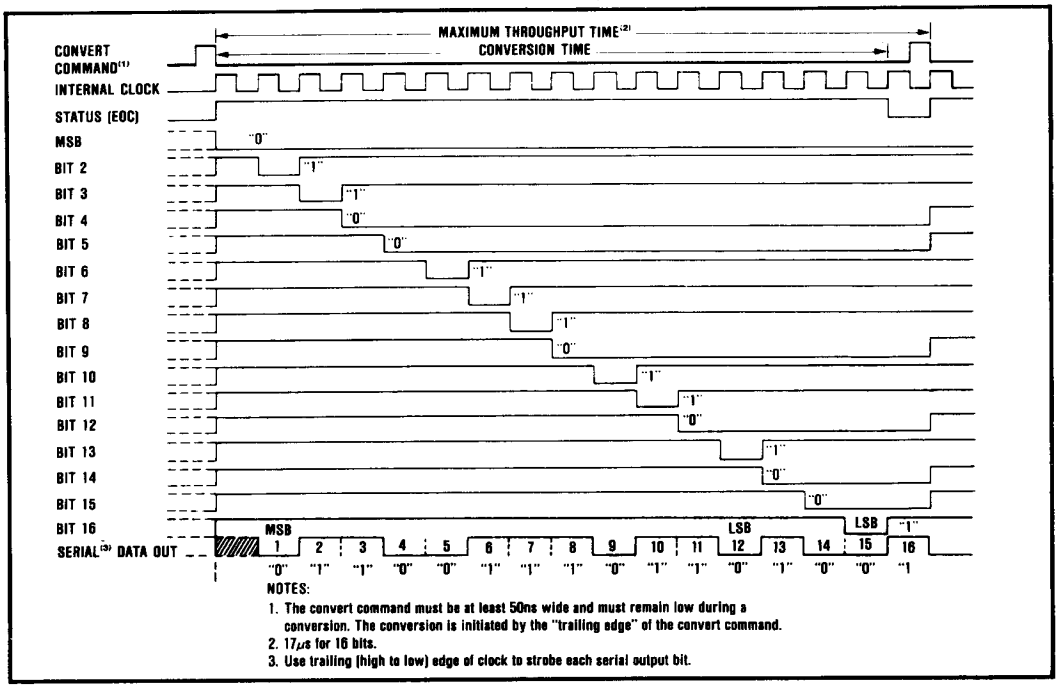


FIGURE 2. Timing Diagram.

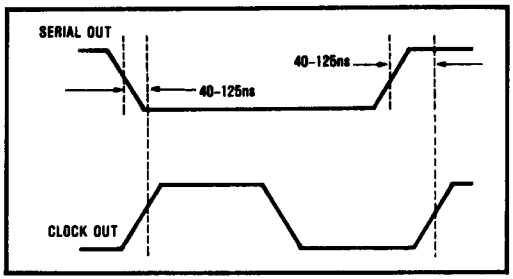


FIGURE 3. Timing Relationship of Serial Data to Clock.

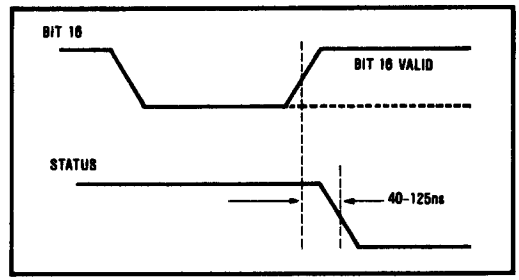


FIGURE 4. Timing Relationship of Valid Data to Status.

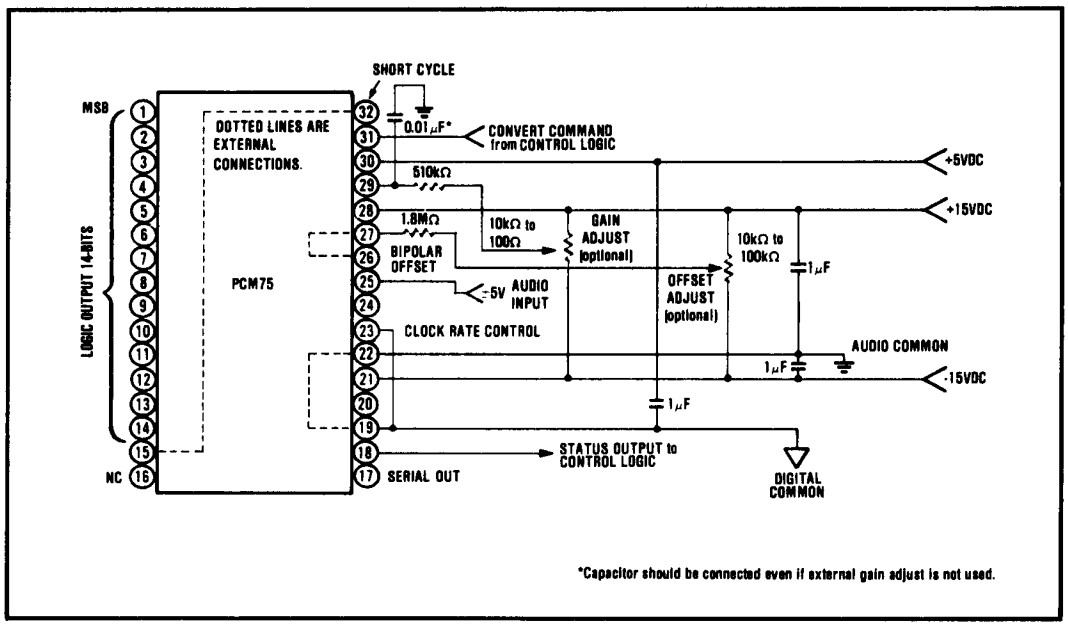


FIGURE 5. PCM75 Connections for: ±5V Audio Input, 14-Bit Resolution (Short-Cycled), Parallel Data Output.

TABLE I. Input Voltages, Transition Values, LSB Values, and Code Definitions.

Binary BIN Output	INPUT VOLTAGE RANGE AND LSB VALUES						
Audio Input Voltage Range	Defined As:	±10V	+5V	+2.5V	0 to +10V	0 to +5V	0 to +20V
Code Designation		COB[1] or CTC[2]	COB[1] or CTC[2]	COB[1] or CTC[2]	CSB[3]	CSB[3]	CSB[3]
One Least Significant Bit LSB	$\frac{FSR}{2^n}$	$\frac{20V}{2^n}$	$\frac{10V}{2^n}$	$\frac{5V}{2^n}$	$\frac{10V}{2^n}$	$\frac{5V}{2^n}$	$\frac{20V}{2^n}$
	n = 16	305µV	153µV	77µV	153µV	77µV	305µV
	n 15	610µV	305µV	153µV	305µV	153µV	610µV
	n = 14	1.22mV	610µV	305µV	6.0µV	305µV	1.22mV
Transition Values MSB LSB							
000...000[4]	+Full Scale	+10V -3/2LSB	+5V -3/2LSB	+2.5V -3/2LSB	+10V -3/2LSB	+5V -3/2LSB	+20V -3/2LSB
011...111	Mid Scale	0	0	0	+5V	+2.5V	+10V
111...110	-Full Scale	-10V +1/2LSB	-5V +1/2LSB	-2.5V +1/2LSB	0 +1/2LSB	0 +1/2LSB	0 +1/2LSB

(1) COB = Complementary Offset Binary
(2) CTC = Complementary Two's Complement - obtained by inverting the most significant bit. MSB pin 1.
(3) CSB = Complementary Straight Binary
(4) Voltages given are the nominal value for transition to the code specified.

DISCUSSION OF SPECIFICATIONS

The PCM75 is specified to provide critical performance criteria for a wide variety of applications. The most critical specifications for an A/D converter in audio applications are total harmonic distortion, drift, gain and offset errors, and conversion time effects on accuracy. The ADC is factory-trimmed and tested for all critical key specifications.

CONVERT COMMAND CONSIDERATIONS

Convert command resets the converter whenever taken high. This insures a valid conversion on the first conversion after power-up.

Convert command must stay low during a conversion unless it is desired to reset the converter during a conversion.

GAIN AND OFFSET ERROR

Initial Gain and Offset errors are factory trimmed to typically ±0.1% of FSR (typically ±0.05% for unipolar offset) at 25°C. These errors may be trimmed to zero by connecting external trim potentiometers as shown in Figures 12 and 13.

POWER SUPPLY SENSITIVITY

Changes in the DC power supplies will affect accuracy. The PCM75 power supply sensitivity is specified for ±0.003% of FSR %/V, for ±15VDC supplies and ±0.0015% of FSR %/V, for +5VDC supplies. Normally, regulated power supplies with 1% or less ripple are recommended for use with this ADC. See Layout Precautions, Power Supply Decoupling, and Figure 9.

TOTAL HARMONIC DISTORTION

The Total Harmonic Distortion (THD) is defined as the ratio of the square root of the sum of the squares of the value of the rms harmonics to the value of the rms fundamental and is expressed in percent or dB. A block diagram of the test circuit used to measure the THD of the PCM75 is shown in Figure 6 along with a timing diagram for the control logic. If we assume that the error due to the test circuit is negligible, then the rms value of the PCM75 error referred to the input can be shown to be

$$\epsilon_{rms} = \sqrt{\frac{1}{N}\sum_{i=1}^{N} [E_I(i) + E_Q(i)]^2}$$

where N is the number of samples, $E_I(i)$ is the linearity error of the PCM75 at each sampling point, and $E_Q(i)$ is the quantization error at each sampling point. The THD can then be expressed as

$$THD = \frac{\epsilon_{rms}}{E_{rms}} = \frac{\sqrt{\frac{1}{N}\sum_{i=1}^{N} [E_I(i) + E_Q(i)]^2}}{E_{rms}} \times 100\%$$

This expression indicates that there is a correlation between the THD and the square root of the sum of the squares of the linearity errors at each digital word of interest. However, this expression does not mean that the worst-case linearity error of the A/D is directly correlated to the THD because the digital output words from the A/D vary according to the amplitude and frequency of the sine wave input as well as the sampling frequency.

For the PCM75 the test sampling period was chosen to be 22.7μs, which is compatible with the EIAJ STC-007 specification for PCM audio. The test frequency is 400Hz and the amplitude of the input signal is 0dB (full scale) and −15dB.

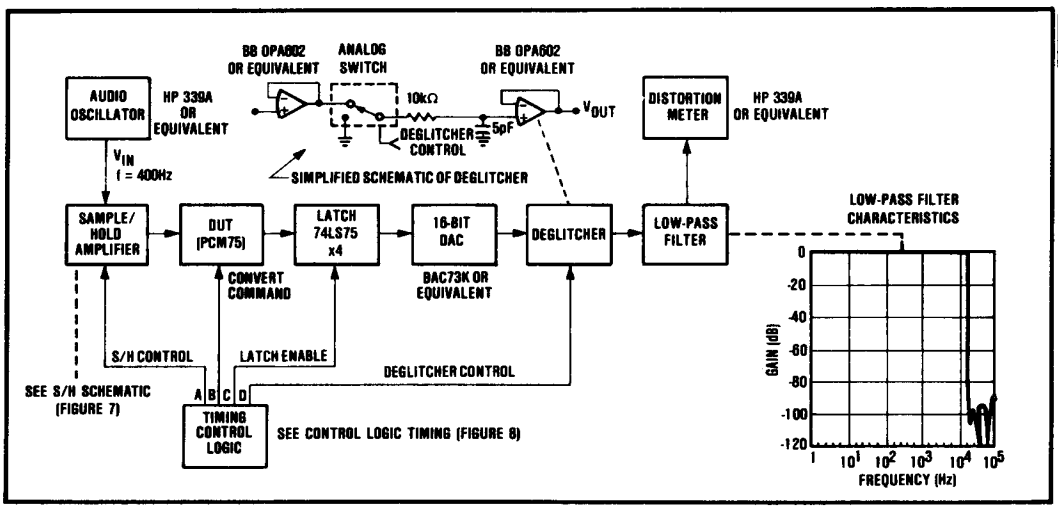


FIGURE 6. Block Diagram of Distortion Test Circuit.

ACCURACY VS CONVERSION TIME

Figures 16 and 17 show the relationship of THD vs input voltage level for the PCM75 with both 14-bit and 16-bit resolution. Notice that the distortion level is reduced by increasing the resolution from 14 to 16 bits due to the reduced quantization error.

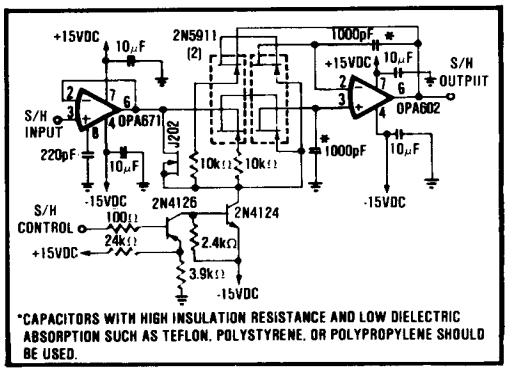


FIGURE 7. Schematic of Sample/Hold Amplifier.

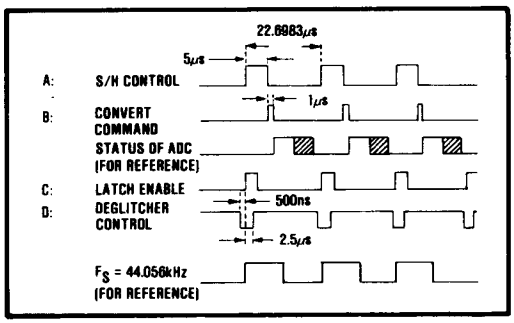


FIGURE 8. Control Logic Timing for PCM75 Distortion Test Circuit.

LAYOUT AND OPERATING INSTRUCTIONS

LAYOUT PRECAUTIONS

Analog and Digital Common are not connected internally in the PCM75 but should be connected together as close to the unit as possible, preferably to a large plane under the ADC. If these grounds must be run separately, use wide conductor pattern and a 0.01µF to 0.1µF nonpolarized bypass capacitor between analog and digital commons at the unit. Low impedance analog and digital common returns are essential for low noise performance. Coupling between analog inputs and digital lines should be minimized by careful layout. The comparator input (pin 27) is extremely sensitive to noise. Any connection to this point should be as short as possible and shielded by Analog Common or ±15VDC supply patterns.

POWER SUPPLY DECOUPLING

The power supplies should be bypassed with tantalum or electrolytic capacitors as shown in Figure 9 to obtain noise free operation. These capacitors should be located close to the ADC. Bypass the 1µF electrolytic type capacitors with 0.01µF ceramic capacitors for improved high frequency performance.

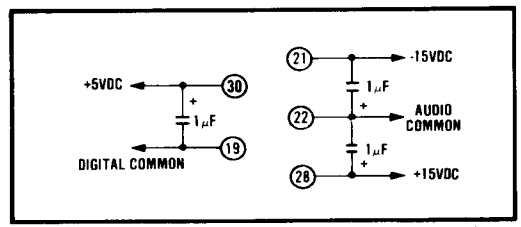


FIGURE 9. Recommended Power Supply Decoupling.

INPUT SCALING

The analog input should be scaled as close to the maximum input signal range as possible in order to utilize the maximum signal resolution of the A/D converter. Connect the input signal as shown in Table II. See Figure 10 for circuit details.

TABLE II. PCM75 Input Scaling Connections.

Input Signal Range	Output Code	Connect Pin 26 To Pin	Connect Pin 24 To	Connect Input Signal To Pin
±10V	COB or CTC*	27	Input Sig.	24
±5V	COB or CTC*	27	Open	25
±2.5V	COB or CTC*	27	Pin 27	25
0 to +5V	CSB	22	Pin 27	25
0 to -10V	CSB	22	Open	25
0 to -20V	CSB	22	Input Sig.	24

*Obtained by inverting MSB pin 1.

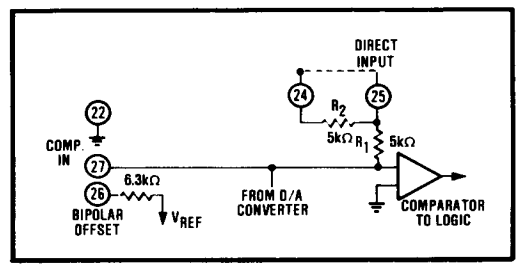


FIGURE 10. PCM75 Input Scaling Circuit.

INPUT IMPEDANCE

The input signal to the PCM75 should come from a low impedance source, such as the output of an op amp, to avoid any errors due to the relatively low input impedance of the PCM75.

If this impedance is not low, a buffer amplifier should be added between the input signal and the direct input to the PCM75 as shown in Figure 11.

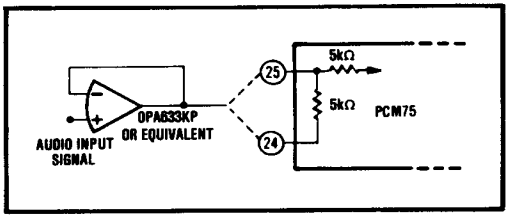


FIGURE 11. Buffer Amplifier for PCM75 Input.

OPTIONAL EXTERNAL GAIN AND OFFSET ADJUSTMENTS

Gain and Offset errors may be trimmed to zero using external gain and offset trim potentiometers connected to the ADC as shown in Figures 12 and 13. Multiturn potentiometers with 100ppm/°C or better TCRs are recommended for minimum drift over temperature and time. These pots may be any value from 10kΩ to 100kΩ. All resistors should be 20% carbon or better. Pin 29 (Gain Adjust) and pin 27 (Offset Adjust) may be left open if no external adjustment is required; however, pin 29 should always be bypassed with 0.01μF to Audio Common.

ADJUSTMENT PROCEDURE

OFFSET—Connect the Offset potentiometer (make sure R_1 is as close to pin 27 as possible) as shown in Figure 12. Sweep the input through the end point transition voltage that should cause an output transition to all bits off (E_{IN}^{OFF}).

Adjust the Offset potentiometer until the actual end point transition voltage occurs at E_{IN}^{OFF}. The ideal transition voltage values of the input are given in Table I.

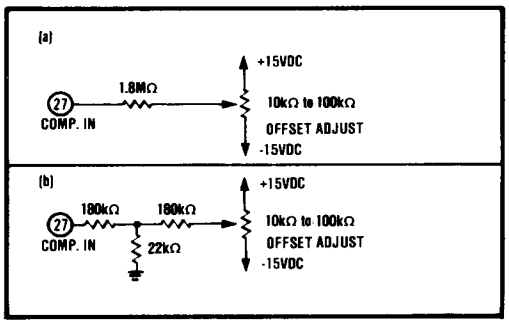


FIGURE 12. Two Methods of Connecting Optional Offset Adjust.

GAIN—Connect the Gain adjust potentiometer as shown in Figure 13. Sweep the input through the end point transition voltage that should cause an output transition to all bits on (E_{IN}^{ON}). Adjust the Gain potentiometer until the actual end point transition voltage occurs at E_{IN}^{ON}. Table I details the transition voltage levels required.

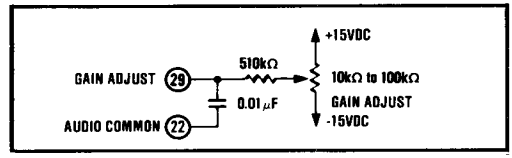


FIGURE 13. Connecting Optional Gain Adjust.

OUTPUT DRIVE

Normally all PCM75 logic outputs will drive two standard TTL loads; however, if long digital lines must be driven, external logic buffers are recommended.

ADDITIONAL OPTIONAL CONNECTIONS

The PCM75 may be operated with faster conversion times for resolutions less than 14 bits, if a higher THD is acceptable, by connecting Short Cycle (pin 32) as shown in Table III. Typical conversion times for the resolution and connections are indicated.

TABLE III. Short Cycle Connections for 14- to 16-Bit Resolutions.

Resolution (Bits)	16	15	14
Connect Pin 32 to	Open	Pin 16	Pin 15
Conversion Time (Typical) μsec	17	16	15

The Clock Rate pin may be connected to an external multiturn trim potentiometer with a TCR of ±100ppm/°C or less as shown in Figure 14. The typical conversion time vs the Clock Rate Control voltage is shown in Figure 15. The effect of varying the conversion time and the resolution on the total harmonic distortion is shown in Figures 16 and 17.

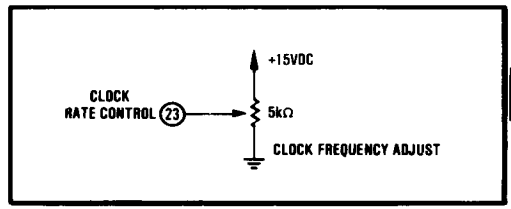


FIGURE 14. Clock Rate Control, Optional Fine Adjust.

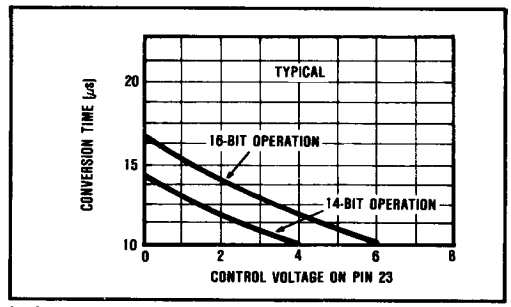


FIGURE 15. Conversion Time vs Clock Rate Control Voltage.

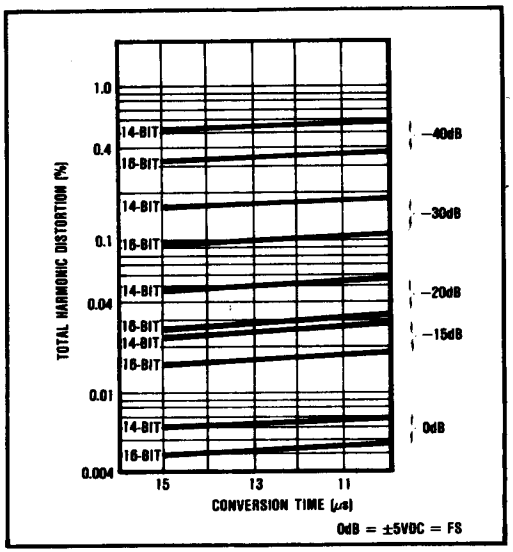


FIGURE 16. Total Harmonic Distortion vs Conversion Time.

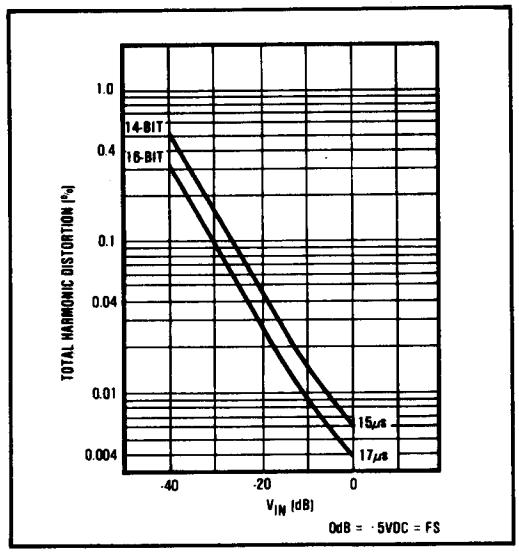


FIGURE 17. Total Harmonic Distortion vs Input Voltage Level.