Preliminary Information

This document contains information on a new product. Parametric information, although not fully characterized, is the result of testing initial devices.

Bt291

27 MHz VideoNet™ RGB-to-YCrCb 8-bit Encoder for 4:2:2 Video Applications

3

Distinguishing Features

- NTSC and CCIR Compatible
- Three 256 x 8 RGB Input RAMs
- Selectable RGB to YCrCb Conversion
- 16-Bit Multiplexed YCrCb I/O Bus
- 8-bit Ancillary Data Input Bus
- Selectable Cr/Cb Decimation Filters
- Low-Pass Y Filter (Optional)
- Video Timing Insertion
- Dynamic Range Control
- TTL Compatible Inputs and Outputs
- +5 V Monolithic CMOS
- 100-pin PLCC Package
- Typical Power Dissipation: 1.1 W

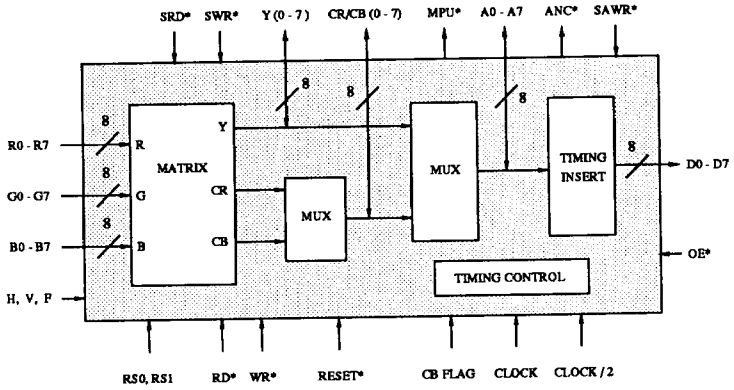
Applications

- CCIR601
- SMPTE RP125
- EBU 3246-E
- Image Processing and Capture
- RGB to YCrCb Conversion

Related Products

- Bt294, Bt296

Functional Block Diagram



Product Description

The Bt291 performs real-time RGB-to-YCrCb conversion. Twenty-four bits of RGB information (8 bits each) are input and converted to YCrCb color information (8 bits each). YCrCb data (4:4:4 format) may also be input via the RGB inputs.

The Y data is optionally low-pass filtered. The Cr and Cb data are decimated to 1/2 the Y data rate and multiplexed together. The Y and Cr/Cb data are further multiplexed, video timing information inserted, and output onto D0–D7.

A 16-bit YCrCb I/O bus is available for active video data I/O. Ancillary data may also be input via A0–A7 for insertion of digital audio, teletext, etc.

Three 256 x 8 lookup RAMs are available on the RGB inputs, to support gamma correction, etc.

The output enable (OE*) three-states the D0–D7 outputs asynchronously to the clocks.

An internal command register (accessible via A0–A7) enables forced blanking levels of Y and Cr/Cb data, and automatic line count transmission. RD* and WR* are used to control accessing the command register.

Brooktree Corporation
9950 Barnes Canyon Rd.
San Diego, CA 92121
(619) 452-7580 • (800) VIDEO IC
TLX: 383 596 • FAX: (619) 452-1249
L291001 Rev. E

Brooktree®

Detailed Block Diagram

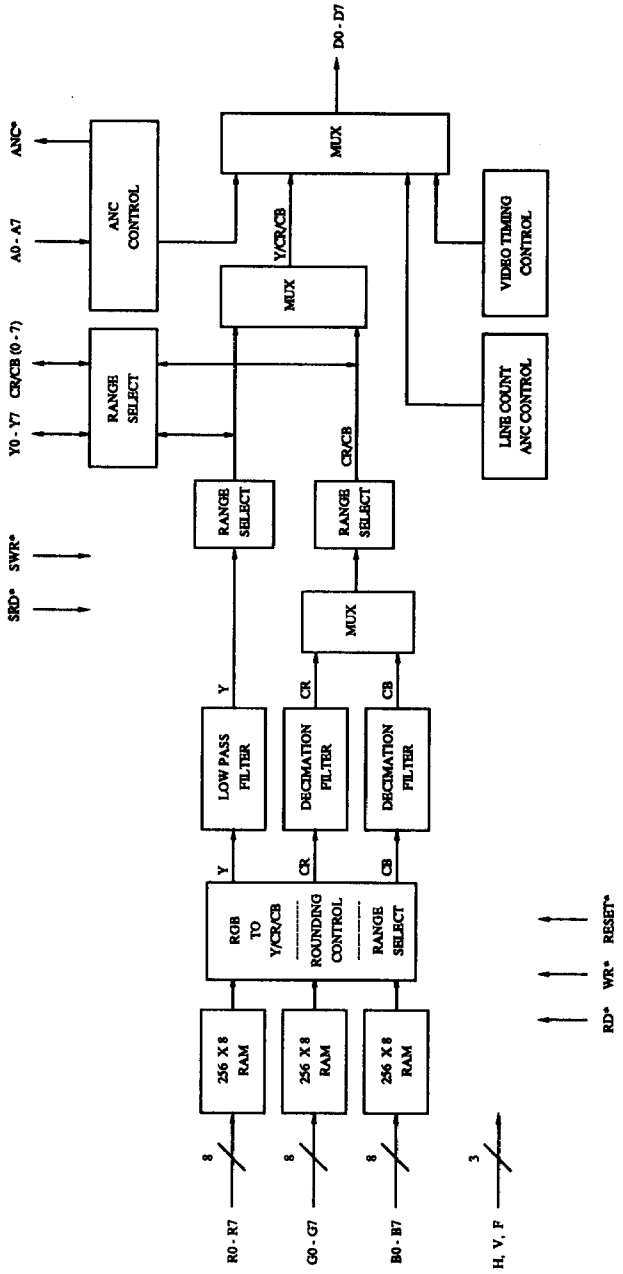


Figure 1. Detailed Block Diagram.

Circuit Description

Input Lookup Table RAMs

R0–R7, G0–G7, and B0–B7 are latched on the rising edge of CLOCK while CLOCK/2 is a logical one. R0–R7 address the red 256 x 8 lookup table RAM, G0–G7 address the green 256 x 8 lookup table RAM, and B0–B7 address the blue 256 x 8 lookup RAM. The outputs of the lookup table RAMs drive the RGB to Y/Cr/Cb color conversion circuitry. (See Figure 1.)

Note that gamma-corrected RGB data must be used for conversion to the YCrCb color space. The three input lookup table RAMs may be used to provide gamma correction on the R0–R7, G0–G7, and B0–B7 inputs in the event that they contain linear (rather than gamma-corrected) RGB data.

The lookup table RAMs are not dual-ported, so MPU accesses have priority over pixel accessing. During MPU access to the color palette RAMs, the lookup table RAM outputs are undefined and invalid.

The lookup table RAMs are not initialized following a reset condition or power-up sequence.

RGB to YCrCb Matrix

The output of the lookup table RAMs drives the RGB to YCrCb matrix. The selected RGB to YCrCb conversion is determined by the command register and is either:

analog coefficient matrix:

$$Y = 0.299R + 0.587G + 0.114B$$

$$Cr = 0.500R - 0.419G - 0.081B + 128$$

$$Cb = -0.169R - 0.331G + 0.500B + 128$$

or digital coefficient matrix:

$$Y = (77/256)R + (150/256)G + (29/256)B$$

$$Cr = (131/256)R - (110/256)G - (21/256)B + 128$$

$$Cb = -(44/256)R - (87/256)G + (131/256)B + 128$$

The analog coefficient matrix can handle RGB data ranges of 1–254 or 16–235. The digital coefficient matrix can only handle RGB data ranges of 16–235. If the RGB data has a range of 0 to 255 (such as data in a graphics frame buffer), the lookup table RAMs may also be used to compress the RGB data range to 16 to 235 (or 1–254), in addition to providing gamma correction.

ROM lookup tables are used to perform the multiplications, and for the analog matrix, 5 bits of fractional data are maintained. The final result is rounded to 8 bits as specified by command register_1. Note the digital matrix maintains full precision (8 bits of fractional data).

The output range of matrix is selected by the CR04 command bit:

(0) Y = 16 to 235; Cr and Cb = 16 to 240

or

(1) Y = 1 to 254; Cr and Cb = 1 to 254

If the CR04 command bit is a logical one, then if the Y, Cr, or Cb output value is zero, it is made 1; if the Y, Cr, or Cb output value is 255, it is made 254.

If the CR04 command bit is a logical zero, then if the Y output value is 0–15, it is made 16; if the Y output value is 236–255, it is made 235. If the Cr or Cb output value is 0–15, it is made 16; if the Cr or Cb output value is 241–255, it is made 240.

This YCrCb range limiting also applies when inputting YCrCb data via the RGB inputs, bypassing the RGB to YCrCb matrix. Note that the lookup table RAMs are still used when inputting YCrCb data via the RGB inputs. The YCrCb range limiting occurs after the lookup table RAMs.

To ease system timing requirements, the RGB, YCrCb, CbFLAG, H, V, and F inputs have the same relative input timing.

Y Low-Pass Filter

The Y channel has a digital low-pass filter after the RGB to YCrCb matrix. Command bit CR00 specifies whether or not to bypass the low-pass filter.

Cr/Cb Filters and Multiplexer

Digital filters low-pass and subsample the Cr and Cb data, reducing the sampling rate of the Cr and Cb data to 1/2 the Y rate, generating 4:2:2 data. The decimated Cr and Cb data is multiplexed together by the Cr/Cb multiplexer. The multiplexer is controlled by the CbFLAG signal.

CbFLAG is latched on the rising edge of CLOCK while CLOCK/2 is a logical one.

Circuit Description (continued)

YCrCb Multiplexer

The YCrCb multiplexer multiplexes the Y and multiplexed Cr/Cb video data into an 8-bit data stream. The timing of the multiplexer is controlled by the internal video timing circuitry.

Timing Insertion

The Bt291 inputs horizontal blanking (H), vertical blanking (V), and even/odd frame (F) timing information. H, V, and F are latched on the rising edge of CLOCK while CLOCK/2 is a logical one and pipelined to maintain synchronization with the RGB data inputs. All changes in state of the V and F inputs must occur with a change of state in H. (Refer to Figures 2–7.)

EAV and SAV Sequences

A zero-to-one transition on the H input triggers an EAV (end of active video) sequence that is output onto D0–D7, overriding YCrCb color data (refer to Figure 9). A one-to-zero transition on the H input triggers a SAV (start of active video) sequence that is output onto D0–D7, overriding any Ancillary data (refer to Figure 10. The pipeline delay of the H input is internally adjusted relative to the RGB inputs so that the SAV and EAV sequences start at the proper location.

The EAV and SAV output sequences are as follows:

$FF $00 $00 $xx

$FF is output with the start of horizontal blanking during the EAV sequence. $xx is output with the end of horizontal blanking during the SAV sequence.

$xx is defined as follows:

D7 = logical one
D6 = F input (F = 1 for field 2; F = 0 for field 1)
D5 = V input (V = 1 during vertical blanking)
D4 = H (H = 0 at SAV, H = 1 at EAV)
D3–D0 = protection bits

The protection bits are derived from V, H, and F as follows:

F = D6	V = D5	H = D4	D3 - D0
0	0	0	0000
0	0	1	1101
0	1	0	1011
0	1	1	0110
1	0	0	0111
1	0	1	1010
1	1	0	1100
1	1	1	0001

D1–D3 are protection bits (Hamming code 6:3) while D0 is an even parity bit for D1–D6.

Line Count Ancillary Sequence

If the line count ANC bit in the command register is set, the Bt291 will generate an Ancillary (ANC) sequence indicating the line number of the scan line about to be sent. This occurs during the six words preceding the SAV sequence. The Line Count ANC output sequence is as follows:

$00 $FF $FF TT MM LL

TT is the automatic Line Count ANC identification code, and is specified by the Line Count register.

Byte TT
D7 = Line Count register bit A7
D6 = Line Count register bit A6
D5 = Line Count register bit A5
D4 = Line Count register bit A4
D3 = Line Count register bit A3
D2 = Line Count register bit A2
D1 = Line Count register bit A1
D0 = odd parity bit

The Bt291 generates an odd parity bit for the Line Count register contents automatically.

Circuit Description (continued)

The MM and LL data words are defined as:

Byte MM	Byte LL
D7 = 0	D7 = 0
D6 = L11	D6 = L5
D5 = L10	D5 = L4
D4 = L9	D4 = L3
D3 = L8	D3 = L2
D2 = L7	D2 = L1
D1 = L6	D1 = L0
D0 = odd parity bit	D0 = odd parity bit

An internal 12-bit vertical counter (L0 is the least significant bit) is used to determine the line number. The H, V, and F inputs are used to control the vertical counter. Command bit CR10 specifies whether line counting is to conform to SMPTE/NTSC or EBU/CCIR standards.

If CR10 is a logical zero (SMPTE/NTSC compatible), the vertical counter is reset to $001 when the V input makes a transition from a logical zero to a logical one while the F input is a logical one. The F input must change state only at the beginning of the vertical sync interval, and have the same timing as the H input. The V input must also have the same timing as the H input (i.e., all changes in state of the V and F inputs must occur with a change of state in H). Field 1 will have 262 lines and field 2 will have 263 lines (assuming a 525-line interlaced system).

If CR10 is a logical one (EBU/CCIR compatible), the vertical counter is reset to $001 when the F input makes a transition from a logical one to a logical zero. The F input must change state only at the beginning of the vertical sync interval, and have the same timing as the H input. The V input must also have the same timing as the H input (i.e. all changes in state of the V and F inputs must occur with a change of state in H). Field 1 will have 312 lines and field 2 will have 313 lines (assuming a 625-line interlaced system).

The vertical counter increments when the H input makes a transition from a logical zero to a logical one.

Note that there are no Ancillary data words associated with the line count ANC sequence. If the automatic line count ANC is enabled, the ANC* output will go high six clock cycles earlier than indicated in Figure 10.

	525-Line 60 Field per Sec.	625-Line 50 Field per Sec.
Effective sampling frequency*		
Luminance (Y)	13.5 MHz	13.5 MHz
Color difference (Cr, Cb)	6.75 MHz	6.75 MHz
Luminance samples (Y) per total line	858	864
Color difference samples per total line (Cr, Cb)	429	432
Number of samples per digital active line		
Y	720	720
Cr, Cb	360	360
Analog to digital horizontal timing relationship		
start of digital blanking to start of analog sync	32 words	24 words
start of analog sync to end of digital blanking	244 words	264 words
digital blanking interval	276 words	288 words

*with CLOCK = 27 MHz. Sampling structure is orthogonal, line, field, and picture repetitive Cr and Cb samples co-sited with odd (1st, 3rd, 5th, etc.) Y samples in each line.

Table 1. Typical Operational Parameters.

Circuit Description (continued)

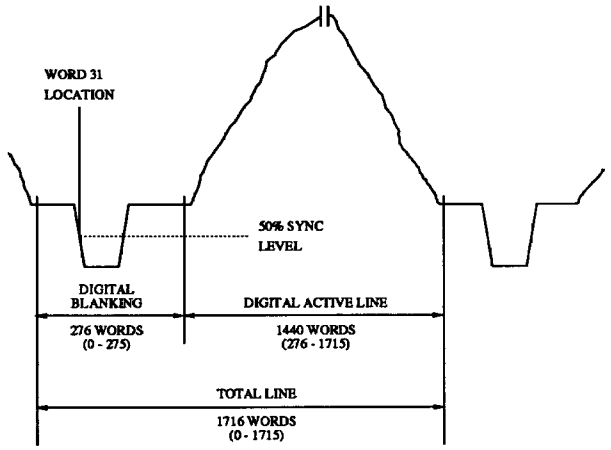


Figure 2. 525-Line, 60 Field/Sec. Horizontal Sync Relationship.

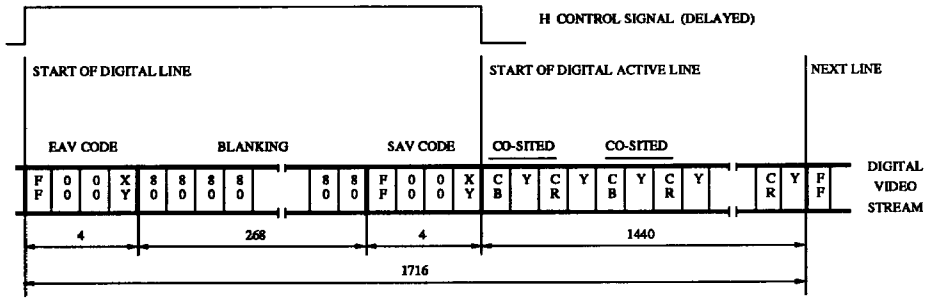


Figure 3. 525-Line, 60 Field/Sec. Digital Horizontal Blanking.

Circuit Description (continued)

YCrCb I/O Bus

A 16-bit bidirectional multiplexed YCrCb bus is provided for reading and writing active video data. The SRD* and SWR* inputs are used to synchronously read and write YCrCb data. SRD* and SWR* must be synchronous to CLOCK/2. (See Figure 8.)

Reading YCrCb Data

While SRD* is a logical zero, YCrCb information from the RGB to YCrCb matrix is output onto Y (0–7) and Cr/Cb (0–7) following the rising edge of CLOCK while CLOCK/2 is a logical one.

The YCrCb output range is selected by the CR04 command bit:

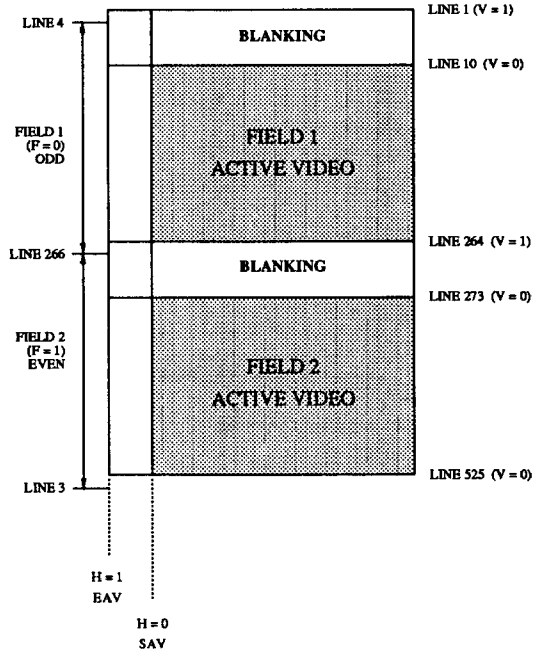
(0) Y = 16 to 235; Cr and Cb = 16 to 240

or

(1) Y = 1 to 254; Cr and Cb = 1 to 254

If the CR04 command bit is a logical one, then if the Y, Cr, or Cb output value is zero, it is made 1; if the Y, Cr, or Cb output value is 255, it is made 254.

If the CR04 command bit is a logical zero, then if the Y output value is 0–15, it is made 16; if the Y output value is 236–255, it is made 235. If the Cr or Cb output value is 0–15, it is made 16; if the Cr or Cb output value is 241–255, it is made 240.



LINE NUMBER	F	V	H (EAV)	H (SAV)
1 - 3	1	1	1	0
4 - 9	0	1	1	0
10 - 263	0	0	1	0
264 - 265	0	1	1	0
266 - 272	1	1	1	0
273 - 525	1	0	1	0

Figure 4. 525-Line, 60 Field/Sec. Vertical Timing.

Circuit Description (continued)

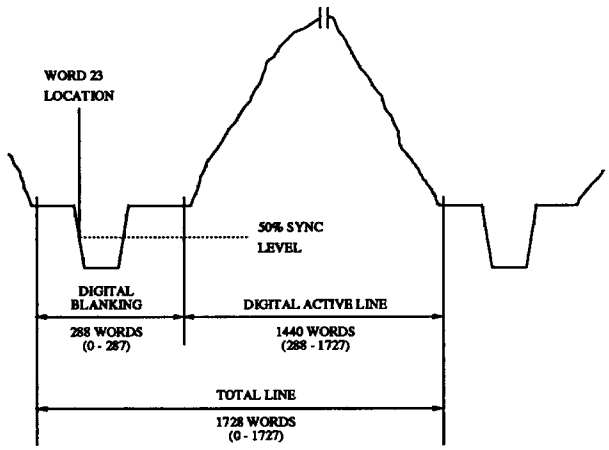


Figure 5. 625-Line, 50 Field/Sec. Horizontal Sync Relationship.

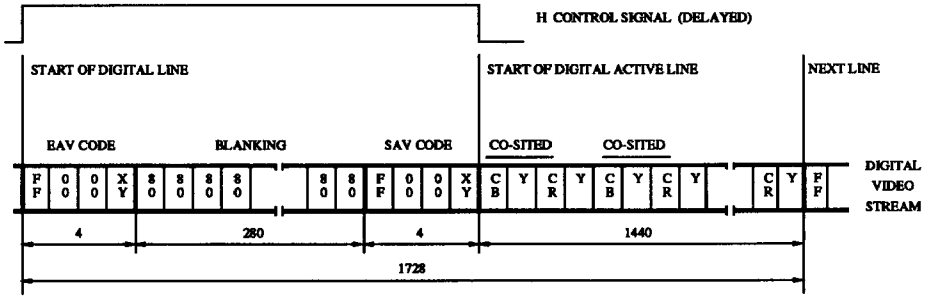


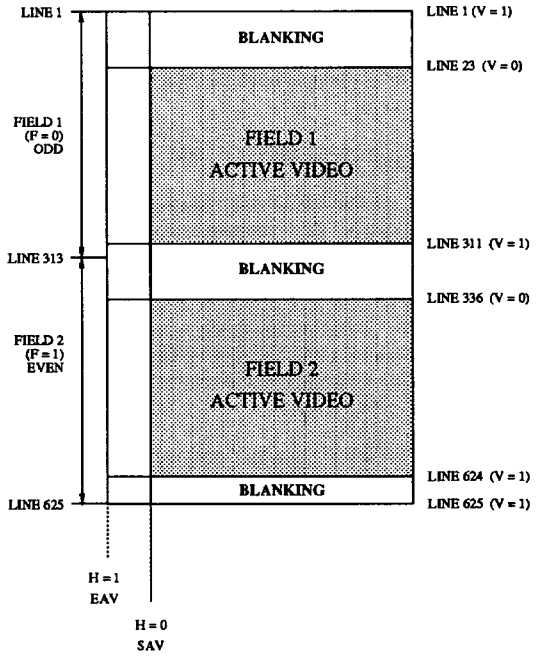
Figure 6. 625-Line, 50 Field/Sec. Digital Horizontal Blanking.

Circuit Description (continued)

525/60 systems	122T	720T	16T	
	0H	digital active line period		Next line
	leading edge of line syncs, half-amplitude reference		0H	
625/50 systems	132T	720T	12T	

T = one luminance sampling clock (74 ns nominal).

Table 2. Digital-Analog Timing Relationship.



LINE NUMBER	F	V	H (EAV)	H (SAV)
1 - 22	0	1	1	0
23 - 310	0	0	1	0
311 - 312	0	1	1	0
313 - 335	1	1	1	0
336 - 623	1	0	1	0
624 - 625	1	1	1	0

Figure 7. 625-Line, 50 Field/Sec. Vertical Timing.

Circuit Description (continued)

If reading YCrCb data during the blanking intervals, Y will be either 1 (CR04 = logical one) or 16 (CR04 = logical zero); CrCb data will be 128.

Note that Y data will be 16 if command register bit CR06 is a logical one (regardless of the value of CR04) and CrCb data will be 128 if command register bit CR07 is a logical one.

If CbFLAG is a logical zero (and CLOCK/2 = 1), Cb data is output onto the CrCb bus during the next read cycle; if CbFLAG is a logical one (and CLOCK/2 = 1), Cr data is output during the next read cycle. This timing enables the CbFLAG status to match the data present on the CrCb (0–7) outputs. CbFLAG is latched on the rising edge of CLOCK while CLOCK/2 is a logical one.

While SRD* is a logical one, the YCrCb bus is three-stated. Note: SRD* must be synchronized to CLOCK externally for proper operation.

Writing YCrCb Data

While SWR* is a logical zero, YCrCb information (and CbFLAG) are latched on the rising edge of CLOCK while CLOCK/2 is a logical one (the RGB inputs are ignored). This YCrCb information is used to generate the D0–D7 output data, rather than the RGB inputs.

The YCrCb input range is selected by the CR04 command bit:

(0) Y = 16 to 235; Cr and Cb = 16 to 240

or

(1) Y = 1 to 254; Cr and Cb = 1 to 254

If the CR04 command bit is a logical one, then if the Y, Cr, or Cb input value is zero, it is made 1; if the Y, Cr, or Cb input value is 255, it is made 254.

If the CR04 command bit is a logical zero, then if the Y input value is 0–15, it is made 16; if the Y input value is 236–255, it is made 235. If the Cr or Cb input value is 0–15, it is made 16; if the Cr or Cb input value is 241–255, it is made 240.

Note that if command register bit CR06 is a logical one, the Y data will be made 16. CrCb data will be made 128 if command register bit CR07 is a logical one.

The CbFLAG input is used to specify whether Cr (CbFLAG = 0) or Cb (CbFLAG = 1) data is being latched via the CrCb bus.

Inputting Ancillary Data—Mode 0

The A1–A7 bus, along with the ANC* output and SAWR* input, are used to input Ancillary data, such as digital audio, teletext, etc. The Bt291 ensures that the ANC and its associated data block will not occupy the intervals reserved for EAV, SAV, or active video.

ANC* is a logical zero for CLOCK cycles that Ancillary data may be input into the Bt291 during horizontal blanking intervals (except when EAV, SAV, or automatic Line Count ANCs are being generated) and active video time during vertical blanking intervals. ANC* is output following the rising edge of CLOCK and its timing is relative to the A1–A7 inputs.

If both SAWR* and ANC* are a logical zero during the rising edge of CLOCK, the A1–A7 input data is accepted as Ancillary data on the rising edge of CLOCK. If ANC* or SAWR* are a logical one, A1–A7 are ignored (except while accessing the command register).

The Ancillary sequence input via A1–A7 and output onto D0–D7 is:

$00 $FF $FF TT MM LL xx xx. . .

where the A1–A7 inputs provide the TT, MM, LL, and $xx data. TT is the data identification code, MM and LL specify the Ancillary data word count, and xx are Ancillary data words.

The Bt291 automatically generates the three word preamble ($00, $FF, $FF). The preamble is generated after a high to low transition of SAWR* while ANC* is a logical zero.

Note that if more than one Ancillary sequence is to be transmitted during a digital blanking interval, the SAWR* input must be a logical one for at least three CLOCK cycles to allow the generation of the three word preamble ($00, $FF, $FF).

Ancillary data identification codes (TT) are represented by a 7-bit word, input via A1–A7. The A0 input is ignored, and the Bt291 internally generates an odd parity bit for the D0 data. This prevents the data identification codes from generating the $00 and $FF values reserved for timing reference purposes.

Circuit Description (continued)

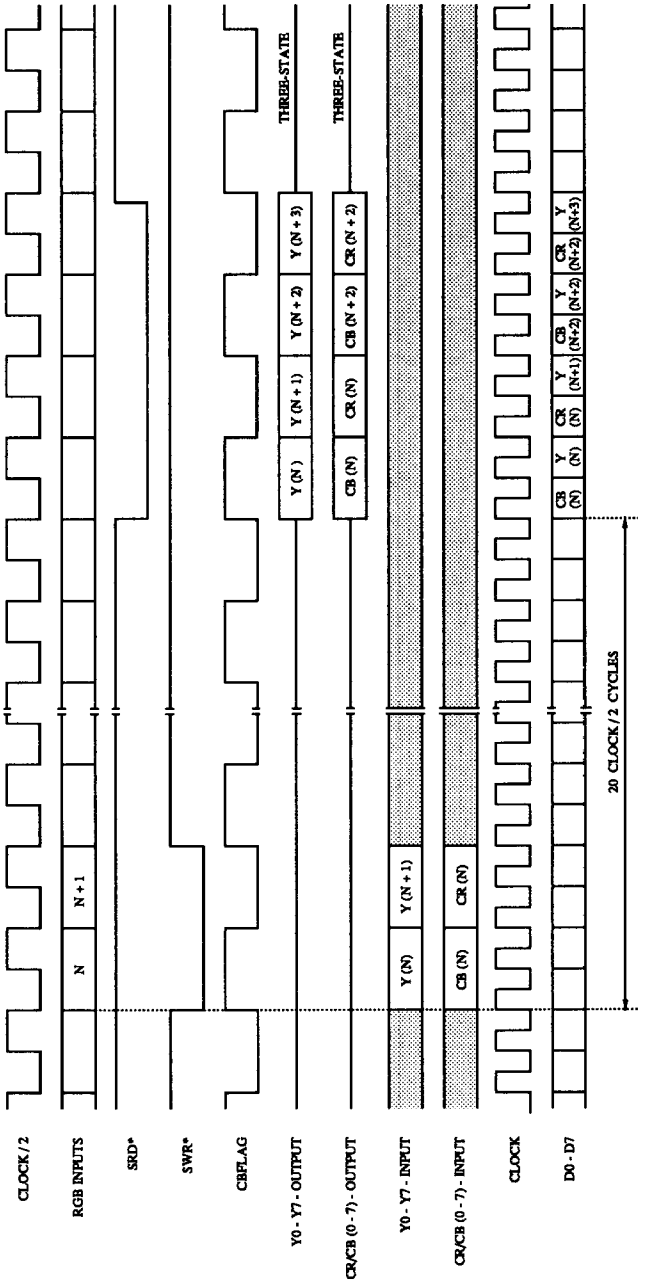


Figure 8. Reading/Writing Active Video Data.

Circuit Description (continued)

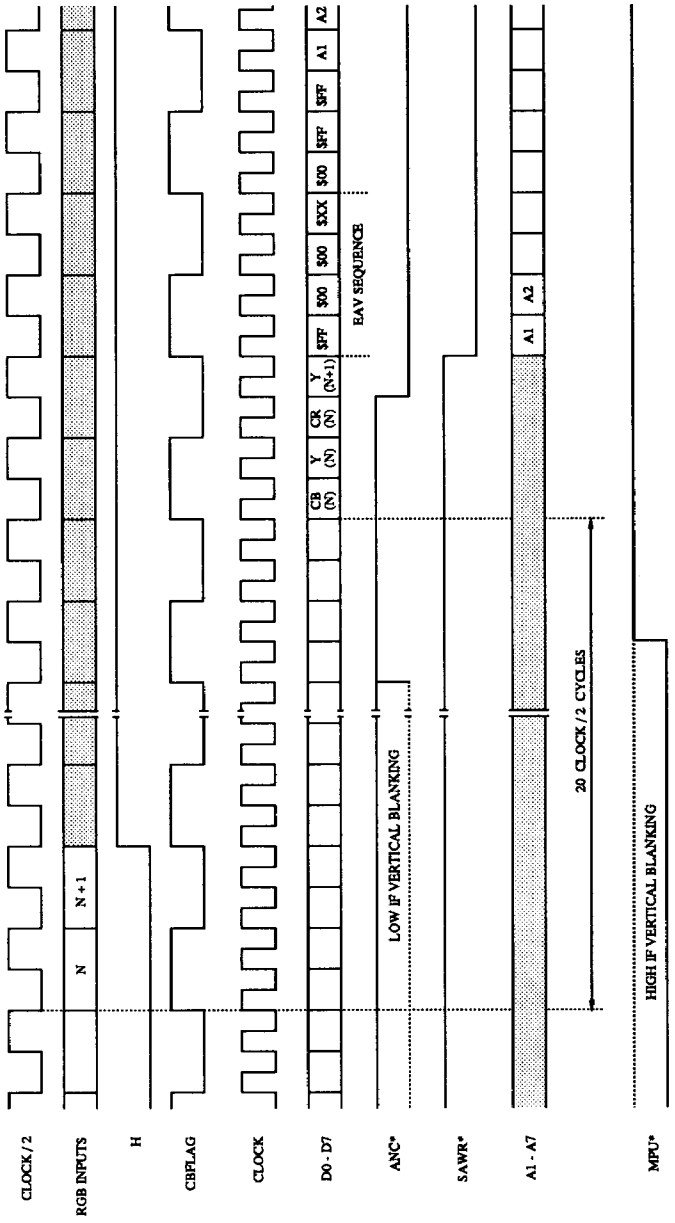


Figure 9. EAV Sequence and Writing Ancillary Data.

Circuit Description (continued)

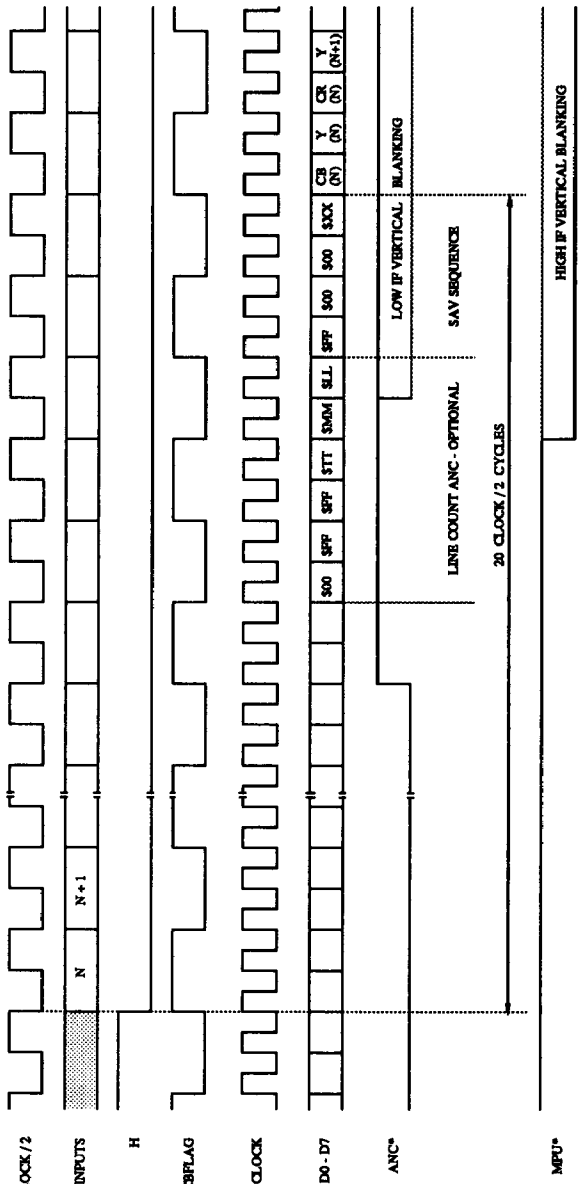


Figure 10. SAV Sequence.

Circuit Description (continued)

Byte TT
D7 = A7 D6 = A6 D5 = A5 D4 = A4 D3 = A3 D2 = A2 D1 = A1 D0 = odd parity bit (A0 = x)

The Ancillary data word count is specified as a 12-bit binary value, with a range of 1 to 1440. Two 6-bit values (MM) and (LL) are written, the most significant 6 bits (MM) first.

The Ancillary data word count is represented as two 6-bit words, input via A1–A6. The A0 and A7 inputs are ignored. The Bt291 internally generates an odd parity bit for the D0 data and internally sets the D7 bit to a logical zero. This prevents the data from generating the $00 and $FF values reserved for timing reference purposes. The most significant 6 bits are transmitted first.

Byte MM	Byte LL
D7 = 0 (A7 = x) D6 = M5 (A6) D5 = M4 (A5) D4 = M3 (A4) D3 = M2 (A3) D2 = M1 (A2) D1 = M0 (A1) D0 = odd parity bit (A0 = x)	D7 = 0 (A7 = x) D6 = L5 (A6) D5 = L4 (A5) D4 = L3 (A4) D3 = L2 (A3) D2 = L1 (A2) D1 = L0 (A1) D0 = odd parity bit (A0 = x)

Ancillary data words are represented as one or more 7-bit words, input via A1–A7. The A0 input is ignored, and the Bt291 internally generates an odd parity bit for the A0 data. This prevents the data from generating the $00 and $FF values reserved for timing reference purposes.

Byte(s) xx
D7 = A7 D6 = A6 D5 = A5 D4 = A4 D3 = A3 D2 = A2 D1 = A1 D0 = odd parity bit (A0 = x)

Ancillary sequences can occur multiple times per scan line if different blocks of data are transmitted.

SAWR* and A1–A7 are latched on the rising edge of CLOCK. When not transmitting Ancillary information (ANC* = logical zero, SAWR* = logical one), a value of 128 is transmitted.

Inputting Ancillary Data—Mode 1

Unlike Mode 0, in this mode the A0–A7 data are output onto D0–D7 directly. No three word ANC preamble is generated, no parity information is generated, and no checking is done to ensure the reserved words $00 and $FF are not transmitted. It is the responsibility of external circuitry to properly generate the Ancillary sequence. There is no change in the pipeline delay from the Mode 0 operation.

Ancillary sequences can occur multiple times per scan line if different blocks of data are transmitted.

SAWR* and A0–A7 are latched on the rising edge of CLOCK. When not transmitting Ancillary information (ANC* = logical zero and SAWR* = logical one), a value of 128 is transmitted.

Ancillary Data Blocks (NTSC)

During horizontal blanking, small blocks of data, up to 268 words in total length (including the ANC preamble(s)), can be transmitted within a horizontal blanking interval. If the Line Count ANC is enabled, 262 words are available (including the ANC preamble (s)).

During vertical blanking, large blocks of data, up to 1440 words in total length (including the ANC preamble(s)), may be transmitted in the interval starting with the end of the SAV and terminating with the beginning of EAV.

Note that in Ancillary mode 1, three less words are available per horizontal or vertical blanking interval.

Ancillary Data Blocks (CCIR)

During horizontal blanking, small blocks of data, up to 280 words in total length (including the ANC preamble(s)), can be transmitted within a horizontal blanking interval. If the Line Count ANC is enabled, 274 words are available (including the ANC preamble (s)).

Circuit Description (continued)

During vertical blanking, large blocks of data, up to 1440 words in total length (including the ANC preamble(s)), may be transmitted in the interval starting with the end of the SAV and terminating with the beginning of EAV.

Note that in Ancillary mode 1, three less words are available per horizontal or vertical blanking interval.

D0–D7 Outputs

Video data is output onto D0–D7 following the rising edge of CLOCK. Command bit CR11 is logically gated with the OE* input, and the resulting value is used to control three-stating the D0–D7 outputs asynchronously to the clocks as described in the Pin Descriptions section.

The output sequence of YCrCb color data is:

Cb Y Cr [Y] ...

where the three words Cb, Y, Cr refer to co-sited samples, the following word [Y] being an isolated luminance sample. Note that Y data will be 16 if command register bit CR06 is a logical one and Cr/Cb data will be 128 if command register bit CR07 is a logical one.

Note that the Bt291 ensures that color data does not generate $00 or $FF to avoid timing errors in the received data.

During horizontal and vertical digital blanking intervals (except for EAV and SAV sequences), the Bt291 outputs 128 if no Ancillary information is being transmitted.

3

RS1, RS0	CR17, CR16	ADDR0–ADDR7	Accessed by MPU
00	xx	$xx	address register
01	00	$00	red RAM location $00
01	00	$01	red RAM location $01
:	:	:	:
01	00	$FF	red RAM location $FF
01	01	$00	blue RAM location $00
01	01	$01	blue RAM location $01
:	:	:	:
01	01	$FF	blue RAM location $FF
01	10	$00	green RAM location $00
01	10	$01	green RAM location $01
:	:	:	:
01	10	$FF	green RAM location $FF
10	xx	$00	command register_0
10	xx	$01	command register_1
10	xx	$02	line count ANC register
10	xx	$03	reserved
:	:	:	:
10	xx	$FF	reserved
11	xx	$xx	reserved

Table 3. Internal Register Addressing.

Circuit Description (continued)

MPU Interface

The Bt291 supports a standard MPU interface (A0–A7, RD*, WR*, MPU*, RS0, and RS1).

The MPU* output indicates when the MPU may access the Bt291 via the A0–A7 pins. A logical zero indicates MPU accesses may be done without contention with Ancillary data timing.

RS0 and RS1 are used to select address register (logical zero) or RAM location or control register specified by the address register (logical one), as shown in Table 3. The 8-bit address register specifies which control register or RAM location the MPU is accessing, also seen in Table 3. The address register resets to $00 following a read or write cycle to location $FF. Write cycles to reserved addresses are ignored, read cycles from reserved addresses return invalid data.

The address register increments after each MPU read or write cycle (except when reading or writing to the address register), and is not initialized. ADDR0 is the least significant bit and corresponds to bit A0.

As the MPU shares the Ancillary bus with Ancillary information, care must be taken that the MPU does not attempt to access the internal registers and lookup table RAMs during the digital blanking intervals. The MPU* output signal may be used to provide arbitration; while MPU* is a logical zero, the MPU may access the Bt291 without contention with any Ancillary data.

The rising edge of WR* latches A0–A7 into the selected register or lookup table RAM location. While RD* is a logical zero, the contents of the selected register or lookup table RAM location are output onto A0–A7. Only one of the RD*, WR*, and SAWR* inputs should be asserted at a time to avoid bus contention.

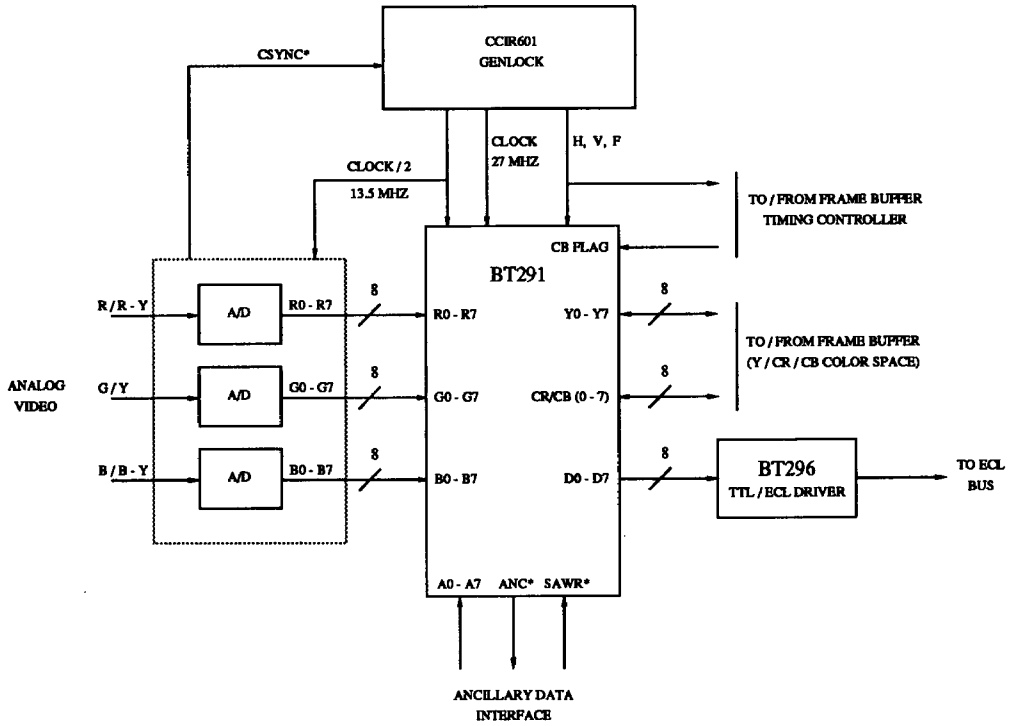


Figure 11. Typical Application.

Circuit Description (continued)

Typical Application

Figure 11 shows the Bt291 in a typical application. Three A/D converters digitize three channels of analog RGB video.

The Bt291 converts this digital video information into 16-bit multiplexed Y and Cr/Cb data for loading into the frame buffer. Data from the frame buffer may also be clocked into the Bt291.

The Bt291 formats the YCrCb data, inserting the necessary timing signals, for driving the Bt296 TTL-to-ECL driver.

A 24-bit frame buffer may also drive the RGB inputs, while the A0–A7 inputs provide Ancillary data. In this instance, the YCrCb I/O bus would not be used, as shown in Figure 12.

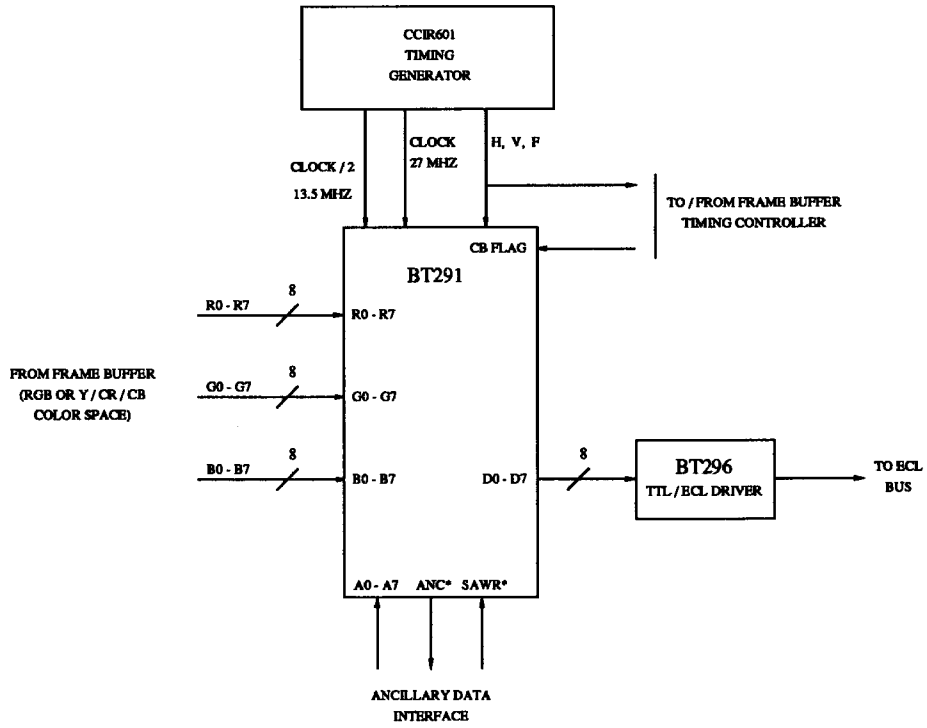


Figure 12. Typical Application.

Internal Registers

Command Register_0

This command register may be written to or read by the MPU at any time and is initialized to $03 following a reset condition. CR00 is the least significant bit and corresponds to bit A0.

CR07	Cr/Cb blanking enable (0) normal operation (1) set Cr/Cb data to 128	A logical one forces the Cr/Cb data from the color matrix to 128, and also forces Cr/Cb data output onto D0–D7 to 128.
CR06	Y blanking enable (0) normal operation (1) set Y data to 16	A logical one forces the Y data from the color matrix to 16, and also forces Y data output onto D0–D7 to 16.
CR05	Line count ANC enable (0) no line count ANC (1) automatic line count ANC	A logical one enables a Line Count ANC to be automatically sent, using the six words prior to the SAV sequence. A logical zero disables transmitting the Line Count ANC.
CR04	YCrCb range (0) Y = 16 to 235, Cr/Cb = 16 to 240 (1) Y, Cr, Cb = 1 to 254	This bit specifies the range of Y, Cr, and Cb for the output of the RGB to YCrCb matrix and the YCrCb I/O bus (when inputting or outputting color data). Typically, mode (0) should be used. Regardless of the selection, there is no change in the pipeline delay.
CR03	RGB or YCrCb input select (0) RGB (1) YCrCb	This bit specifies whether the RGB inputs are inputting RGB or YCrCb color information. Y information is input via the G0–G7 inputs, Cr information is input via the R0–R7 inputs, and Cb information is input via the B0–B7 inputs. If inputting YCrCb information, the RGB-to-YCrCb matrix is bypassed; however, the range specified by command bit CR04 is still used. Regardless of the selection, there is no change in the pipeline delay.
CR02 , CR01	Cr/Cb decimation filters select (00) use 3-tap filters (01) use 13-tap filters (10) reserved (11) bypass filters	These bits specify whether or not to bypass the Cr/Cb decimation filters and which decimation filter to use. If bypassed, the Cr/Cb multiplexer performs the actual decimation of the Cr and Cb data. Regardless of the selection, there is no change in the pipeline delay. Typically, the 13-tap filters should be used.
CR00	Y low pass filter bypass enable (0) use filter (1) bypass filter	This bit specifies whether or not to bypass the Y low pass filter. Regardless of the selection, there is no change in the pipeline delay.

Internal Registers (continued)

Command Register_1

This command register may be written to or read by the MPU at any time and is initialized to $3A following a reset condition. CR10 is the least significant bit and corresponds to bit A0.

CR17, CR16 — Lookup table RAM select

- (00) red lookup table RAM
- (01) blue lookup table RAM
- (10) green lookup table RAM
- (11) reserved

These bits specify which lookup table RAM the MPU is accessing. NOTE: This decode differs from the Bt294 command bits CR03 and CR02.

CR15 — Matrix coefficient select

- (0) analog matrix
- (1) digital matrix

This bit selects which set of coefficients to use in the RGB-to-YCrCb matrix, as described in the text. Typically, the digital matrix should be used. Regardless of the selection, there is no change in the pipeline delay.

CR14, CR13 — Rounding select

- (00) normal rounding
- (01) even rounding
- (10) reserved
- (11) Dynamic Rounding™

This bit specifies the type of rounding used. Regardless of the selection, there is no change in the pipeline delay.

(00) specifies round up if the fractional data is ≥ 0.5. If the fractional data is < 0.5, the number will be rounded down.

(01) specifies round up if the fractional data = 0.5 and the rounded result will be an even number (LSB = 0) or if the fractional data is > 0.5. If the fractional data is < 0.5, the number will be rounded down.

(11) specifies to use Dynamic Rounding™, where the fractional data is compared to a random number, and the result (1 bit) added to the 8 bits of color data. If the fractional data = 0, no rounding is done. R, G, and B each have their own random number generator. Typically, this mode should be used.

Dynamic Rounding™ is used under license from Quantel Limited.

CR12 — Ancillary input format

- (0) mode 0
- (1) mode 1

This bit specifies the operation of inputting Ancillary data. Refer to text for details. Typically, mode (0) should be used.

CR11 — D0–D7 output disable

- (0) enable D0–D7 outputs
- (1) disable D0–D7 outputs

This bit is logically gated with the OE* input pin, and the resulting value is used to control three-stating the D0–D7 outputs.

Internal Registers (continued)

Command Register_1 (continued)

CR10	Vertical counter operation (0) SMPTE/NTSC compatible (1) EBU/CCIR compatible	This bit specifies whether the vertical counter scan line numbering for the Line Count ANC function is to be SMPTE/NTSC (logical zero) or EBU/CCIR (logical one) compatible. During SMPTE/NTSC compatibility, scan line number one is the first scan line during vertical blanking in digital field 2. During EBU/CCIR compatibility, scan line number one is the first scan line during vertical sync in digital field 1.

Line Count ANC Register

The 8-bit Line Count register may be written to or read by the MPU at any time and is initialized to $00 following a reset condition. A0 is the least significant bit.

This register specifies the Ancillary data ID value (TT) of the automatic Line Count ANC.

Bit A0 is always a logical zero. MPU data written to bit A0 is ignored.

Pin Descriptions

Pin Name	Description
Y0–Y7	Y data inputs/outputs (TTL compatible). Y information is input or output via these pins depending on the value of SWR* and SRD*. Y0 is the least significant bit. If inputting Y data, it is latched on the rising edge of CLOCK while CLOCK/2 is a logical one. If outputting Y data, it is output following the rising edge of CLOCK while CLOCK/2 is a logical one.
CR/Cb (0–7)	Cr/Cb data inputs/outputs (TTL compatible). Multiplexed Cr and Cb information is input or output via these pins depending on the value of SWR* and SRD*. CrCb0 is the least significant bit. If inputting Cr/Cb data, it is latched on the rising edge of CLOCK while CLOCK/2 is a logical one. If outputting Cr/Cb data, it is output following the rising edge of CLOCK while CLOCK/2 is a logical one.
SWR*	Synchronous write control input (TTL compatible). A logical zero enables Y/Cr/Cb data to be input via the Y0–Y7 and Cr/Cb (0–7) pins. Both SRD* and SWR* should not be asserted simultaneously.
SRD*	Synchronous read control input (TTL compatible). A logical zero enables Y/Cr/Cb data to be output onto the Y0–Y7 and Cr/Cb (0–7) pins. Both SRD* and SWR* should not be asserted simultaneously.
A0–A7	Ancillary data inputs (TTL compatible). While both ANC* and SAWR* are a logical zero, A1–A7 are latched on the rising edge of CLOCK and output onto D0–D7. MPU data is also input and output via this bus. A0 is the least significant bit.
SAWR*	Ancillary write control input (TTL compatible). If ANC* is a logical zero, a logical zero on SAWR* will enable A1–A7 data to be latched. SAWR* is latched on the rising edge of CLOCK, and pipelined to maintain synchronization with the A1–A7 data. This pin should be a logical one if the Ancillary data transmission capabilities are not used.
ANC*	Ancillary output (TTL compatible). A logical zero indicates Ancillary data may be input via the A1–A7 pins. ANC* is output following the rising edge of CLOCK.
CbFLAG	CbFLAG control input (TTL compatible). It is latched on the rising edge of CLOCK while CLOCK/2 is a logical one.
R0–R7	Red inputs (TTL compatible). Red color information is input via these pins. Data is latched on the rising edge of CLOCK while CLOCK/2 is a logical one. R0 is the least significant bit.
G0–G7	Green inputs (TTL compatible). Green color information is input via these pins. Data is latched on the rising edge of CLOCK while CLOCK/2 is a logical one. G0 is the least significant bit.
B0–B7	Blue inputs (TTL compatible). Blue color information is input via these pins. Data is latched on the rising edge of CLOCK while CLOCK/2 is a logical one. B0 is the least significant bit.
D0–D7	Data outputs (TTL compatible). Transmitted data is output onto D0–D7 following the rising edge of CLOCK. D0 is the least significant bit.
V, H, F	Video timing control inputs (TTL compatible). They are latched on the rising edge of CLOCK while CLOCK/2 is a logical one.

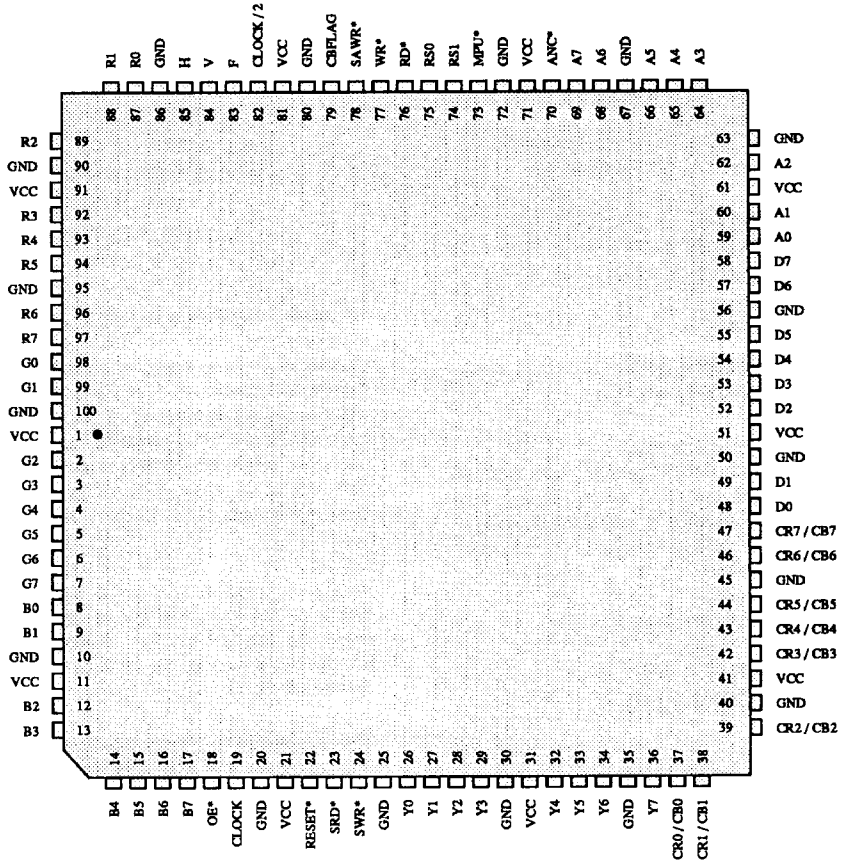
Pin Descriptions (continued)

Pin Name	Description
OE*	Output enable control input (TTL compatible). This input is logically gated with command bit CR11, and the result controls three-stating the D0–D7 outputs as follows:

CR11	OE*	D0–D7 Outputs
0	0	enabled
0	1	three-stated
1	0	three-stated
1	1	three-stated

RESET*	Reset control input (TTL compatible). RESET* is sampled on the rising edge of CLOCK, and must be a logical zero for a minimum of three consecutive CLOCK cycles to reset the device. RESET* must be a logical one for normal operation.
RD*	MPU read control input (TTL compatible). While a logical zero, the contents of the control register/RAM location are output onto A0–A7 asynchronously to the clocks. If both RD* and WR* are asserted simultaneously, all signal pins are three-stated (note the device should be reset after three-stating the signal pins).
WR*	MPU write control input (TTL compatible). The rising edge of WR* latches the A0–A7 inputs into the control register/RAM location asynchronously to the clocks. If both RD* and WR* are a asserted simultaneously, all signal pins are three-stated (note the device should be reset after three-stating the signal pins).
RS0, RS1	Register select control inputs (TTL compatible). These bits specify whether the MPU is accessing the address register or the control register/RAM location specified by the address register. See Table 3.
MPU*	MPU access control output (TTL compatible). A logical zero indicates the MPU may access the internal registers without contention with Ancillary data. MPU* is output following the rising edge of CLOCK.
CLOCK	27 MHz clock input (TTL compatible). The clock must be present for the MPU to access the internal control registers.
CLOCK/2	13.5 MHz clock input (TTL compatible).
VCC	Power pins. All VCC pins must be connected together.
GND	Ground pins. All GND pins must be connected together.

Pin Descriptions (continued)



Application Information

Cr/Cb Decimation Filters

The Cr/Cb linear phase decimation filters low-pass and subsample the Cr and Cb data to generate 4:2:2 YCrCb data.

If the CR04 command bit is a logical one, then then if the result is zero, it is made 1; if the result is 255, it is made 254. If the CR04 command bit is a logical zero, if the result is 0–15, it is made 16; if the result is 241–255, it is made 240.

The transfer function of the 13-tap filters is:

$$H(Z) = 128/256 * Z0 + (80/25) * (Z^{-1} + Z^{+1}) + (-24/256)*(Z^{-3} + Z^{+3}) + (12/256)*(Z^{-5} + Z^{+5}) + (-6/256)*(Z^{-7} + Z^{+7}) + (3/256)*(Z^{-9} + Z^{+9}) + (-1/256)*(Z^{-11} + Z^{+11})$$

Eighteen-bit precision (including sign and overflow) is maintained until the final output stage, then rounded to 8 bits as specified by command register_1. Figure 13 shows the transfer function of the 13-tap Cr and Cb decimation filters.

The transfer function of the 3-tap filters is:

$$H(Z) = 128/256*Z^0 + (64/256)*(Z^{-1} + Z^{+1})$$

Twelve-bit precision (including sign and overflow) is maintained until the final output stage, then rounded to 8 bits as specified by command register_1.

During blanking periods, the input color data is undefined, possibly disturbing the computed color data at the beginning and end of active color data. To avoid this, if the 13-tap is filter selected, the 3-tap filter is automatically used at the beginning and end of the active line unless the 13-tap filter is available (i.e., the filter pipe is full). Regardless of the filter selection, the first active pixel per scan line to be decimated uses only the multiplexer (bypassing the digital filters).

Y Low-Pass Filter

Y may be optionally low-pass filtered using a 19-tap filter whose transfer function is:

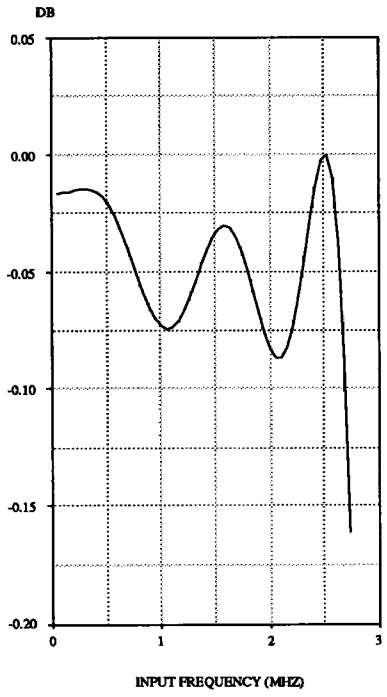
$$H(Z) = 116/128* Z0 + (12/128)*(Z^{-1} + Z^{+1}) + (-11/128)*(Z^{-2} + Z^{+2}) + (10/128)*(Z^{-3} + Z^{+3}) + (-8/128)*(Z^{-4} + Z^{+4}) + (6/128)*(Z^{-5} + Z^{+5}) + (-5/128)*(Z^{-6} + Z^{+6}) + (3/128)*(Z^{-7} + Z^{+7}) + (-2/128)*(Z^{-8} + Z^{+8}) + (1/128)*(Z^{-9} + Z^{+9})$$

Seventeen-bit precision (including sign and overflow) is maintained until the final output stage, then rounded to 8 bits as specified by command register_1. If the CR04 command bit is a logical one, then if the result is zero, it is made 1; if the result is 255, it is made 254. If the CR04 command bit is a logical zero, then if the result is 0–15, it is made 16; if the result is 236–255, it is made 235. Figure 14 shows the transfer functions of the 19-tap Y filter.

During blanking periods, the input color data is undefined, possibly disturbing the computed color data at the beginning and end of active color data. To avoid this, the first and last 19 active pixels per scan line are not processed by the digital filter (bypassing the digital filter).

The Y data and control signals are pipelined to maintain synchronization with the Cr/Cb data. There is no change in the pipeline delay regardless of which filter (if any) is used.

Application Information (continued)



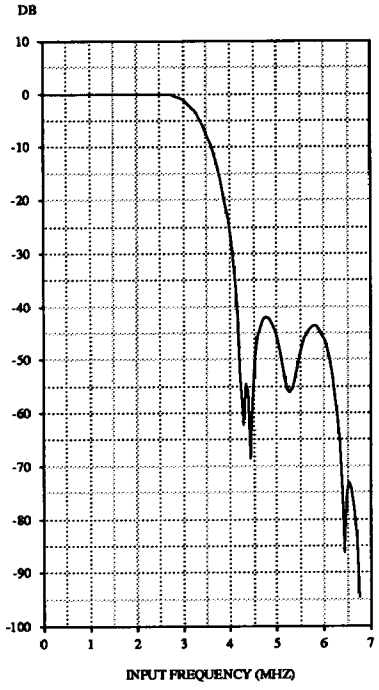


Figure 13. CrCb 13-Tap Pass-Band and Stop-Band Low-Pass / Decimation Filter Characteristics.

Application Information (continued)

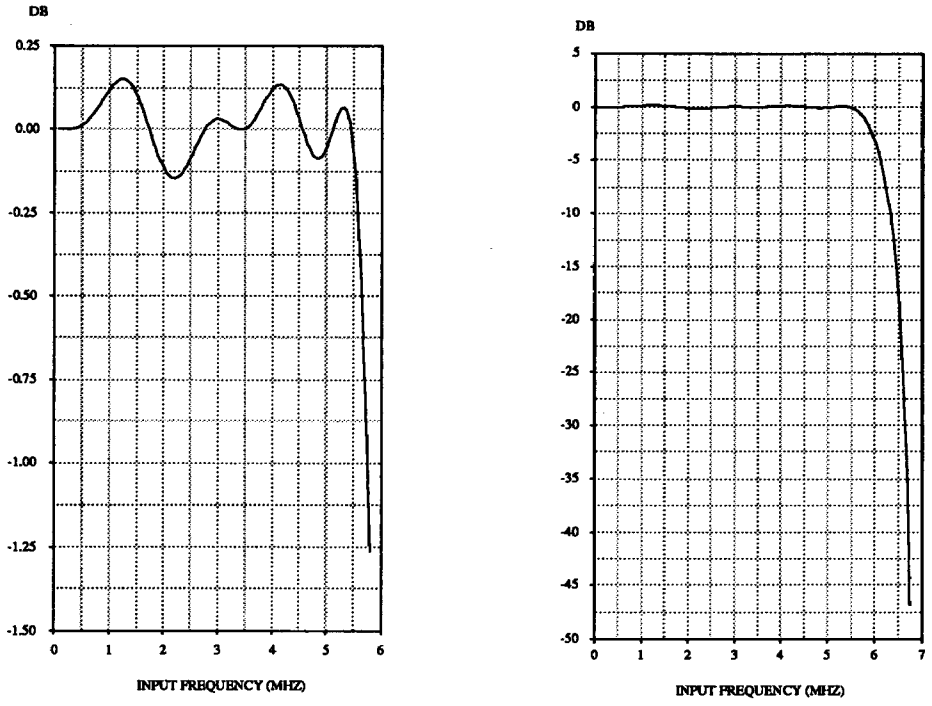


Figure 14. Y 19-Tap Pass-Band and Stop-Band Low-Pass Filter Characteristics.

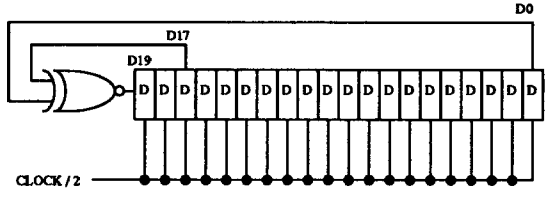


Figure 15. Random Number Generator.

Application Information (continued)

Random Number Generator

Figure 15 illustrates the random number generator used when Dynamic Rounding™ (used under license from Quantel Limited) is selected. Following a reset condition the random number generator is initialized to $00000.

As each YCrCb value in the analog matrix has 5 fractional data bits, 5 bits of random numbering is generated for each Y, Cr, and Cb value (random number bits D0, D4, and D8 correspond to the LSBs of Y, Cr, and Cb digital matrix fractional data).

Usage	Fractional Data Bits (MSB–LSB)
Y matrix (digital)	D7–D0
Y matrix (analog)	D7–D3
Cr matrix (digital)	D11–D4
Cb matrix (digital)	D15–D8
Cr matrix (analog)	D11–D7
Cb matrix (analog)	D15–D11
Y filter	D3–D0, D19–D17
CrCb filter (13-tap)	D19–D12
CrCb filter (3-tap)	D19, D18

As a single CrCb filter is used in a multiplexed fashion, a single CrCb random number generator is used. The 13-tap CrCb filter has 8 bits of fractional data. Random number bit D12 corresponds to the LSB of Cr and Cb fractional data.

Random number bits D19 and D18 are used for the 3-tap CrCb filter, which has 2 bits of fractional data.

The 19-tap Y filter has 7 fractional data bits, with the random number fractional bits shown above.

Typical Applications

Figure 16 shows the Bt291 and Bt294 being used with a 24-bit RGB frame buffer. The Bt291 and Bt294 provide another video I/O port to the imaging/graphics system.

Figure 17 shows the Bt291 and Bt294 being used with a 16-bit YCrCb frame buffer. The Bt291 and Bt294 provide another video I/O port to the imaging/graphics system.

ESD and Latchup Considerations

Correct ESD sensitive handling procedures are required to prevent device damage which can produce symptoms of catastrophic failure or erratic device behavior with somewhat "leaky" inputs.

All logic inputs should be held low until power to the device has settled to the specified tolerance.

Latchup can be prevented by assuring that all VCC pins are at the same potential, and that the VCC supply voltage is applied before the signal pin voltages. The correct power-up sequence assures that any signal pin voltage will never exceed the power supply voltage by more than +0.5 V.

PLCC Sockets

100-pin PLCC sockets for the Bt291 are available from:

McKenzie Technology
44370 Old Warm Springs Blvd.
Fremont, CA 94538
Phone: (415) 651-2700
FAX: (415) 651-1020
TLX: 910-240-6355
Part Number: PLCC-100-P-T

or

Yamaichi Electric Mfg.Co., LTD.
3-28-7 Nakamagome, Ohta-Ku,
Tokyo 143 Japan
Phone: 03-778-6161
FAX: 03-778-6181
U.S. Representative: (408) 452-0797

Application Information (continued)

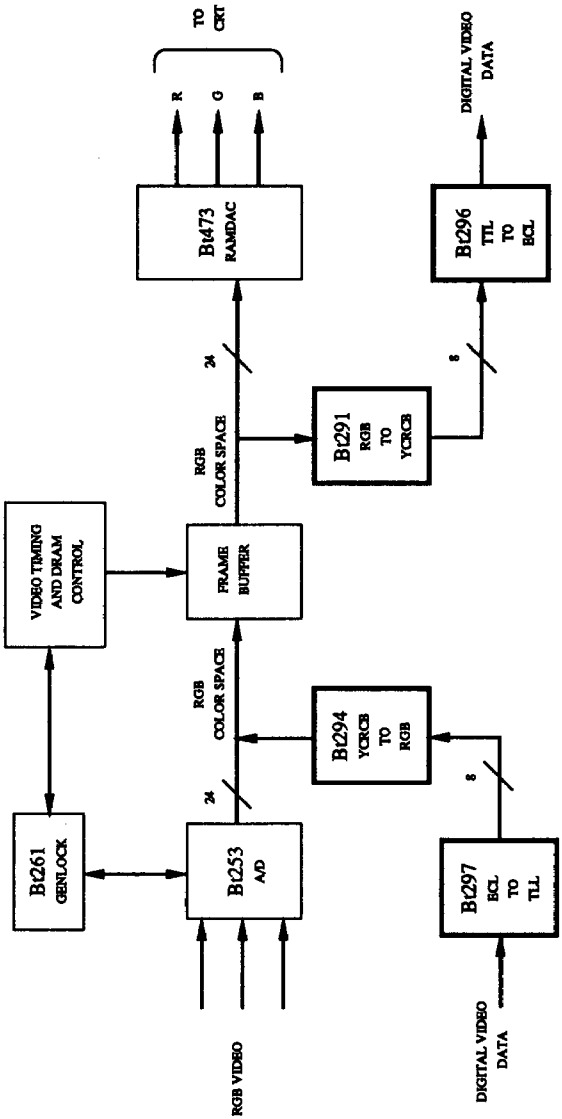


Figure 16. Typical Application.

Application Information (continued)

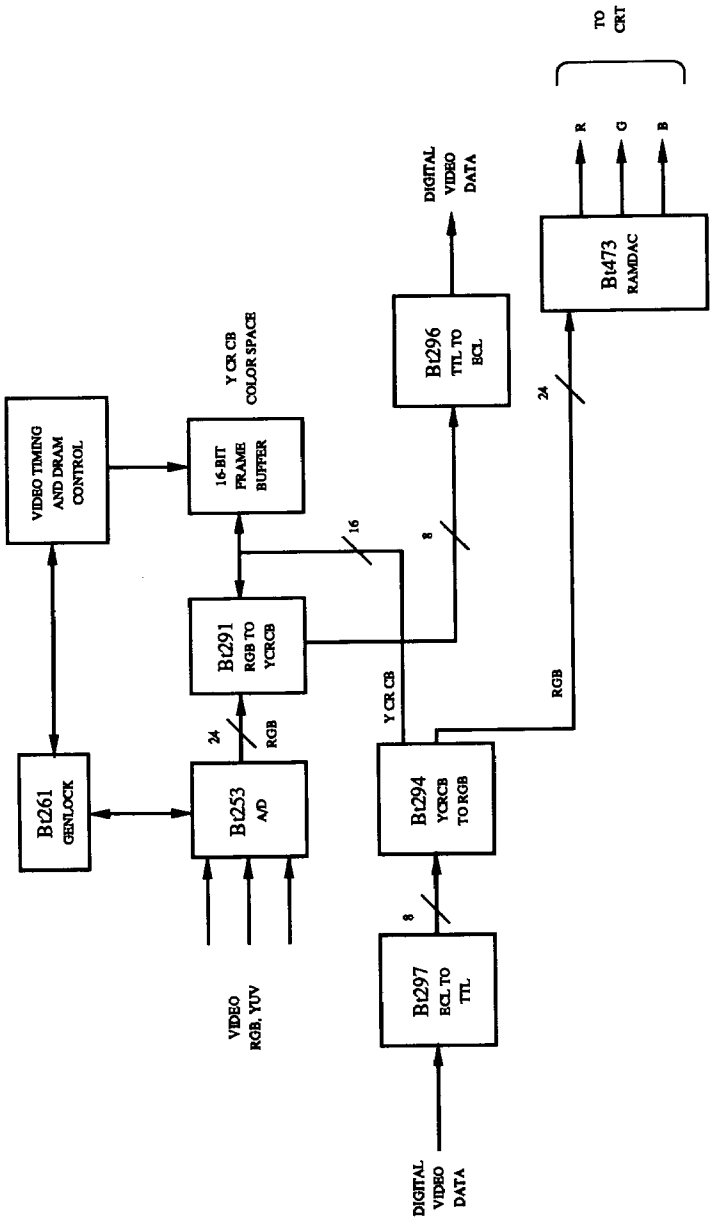


Figure 17. Typical Application.

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Units
Power Supply	VCC	4.5	5.00	5.5	Volts
Ambient Operating Temperature	TA	0		+70	°C

Absolute Maximum Ratings

Parameter	Symbol	Min	Typ	Max	Units
VCC (measured to GND)				7.0	Volts
Voltage on Any Signal Pin*		GND–0.5		VCC + 0.5	Volts
Ambient Operating Temperature	TA	–55		+125	°C
Storage Temperature	TS	–65		+150	°C
Junction Temperature	TJ			+150	°C
Vapor Phase Soldering (1 minute)	TVSOL			220	°C

Note: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

* This device employs high impedance CMOS devices on all signal pins. It should be handled as an ESD-sensitive device. Voltage on any signal pin that exceeds the power supply voltage by more than +0.5 V can induce destructive latchup.

DC Characteristics

Parameter	Symbol	Min	Typ	Max	Units
Digital Inputs					
Input High Voltage	VIH	2.0		VCC + 0.5	Volts
Input Low Voltage	VIL	GND–0.5		0.8	Volts
Input High Current (Vin = 2.4 V)	IIH			1	µA
Input Low Current (Vin = 0.4 V)	IIL			–1	µA
Input Capacitance (f = 1 MHz, Vin = 2.4 V)	CIN		7		pF
Digital Outputs					
Output High Voltage (IOH = –400 µA)	VOH	2.4			Volts
Output Low Voltage (IOL = 6.4 mA)	VOL			0.4	Volts
3-state Current (If Applicable)	IOZ			50	µA
Output Capacitance	COUT		20		pF

Test conditions (unless otherwise specified): "Recommended Operating Conditions." Typical values are based on nominal temperature, i.e., room, and nominal voltage, i.e., 5 V.

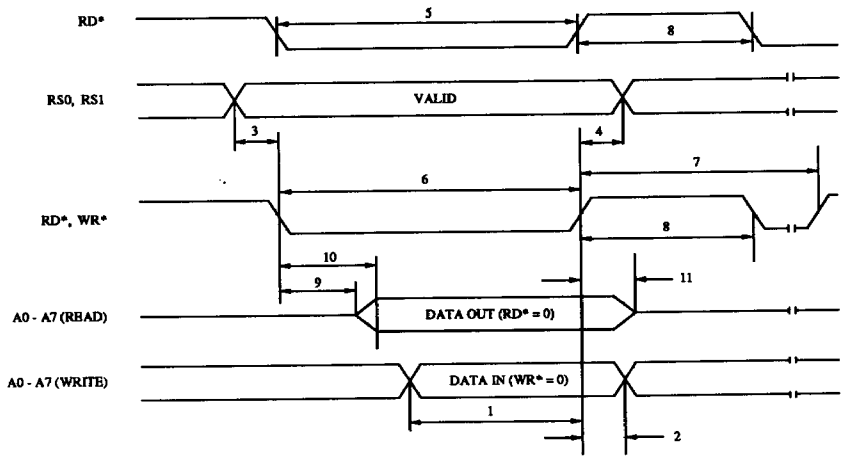
AC Characteristics

Parameter	Symbol	Min	Typ	Max	Units
Clock Rate	Fmax			27	MHz
MPU Write Data Setup Time	1	10			ns
MPU Write Data Hold Time	2	10			ns
RS0, RS1 Setup Time	3	10			ns
RS0, RS1 Hold Time	4	10			ns
RD* Low Time	5	1			Clock
WR* Low Time	6	100			ns
WR* Cycle Time	7	3			Clocks
RD*, WR* High Time	8	30			ns
RD* Asserted to Data Bus Driven	9	5			ns
RD* Asserted to Data Valid	10			100	ns
RD* Negated to Data Bus 3-Stated	11			25	ns
Clock/2 Setup Time	12	12			ns
Clock/2 Hold Time	13	5			ns
RGB (0–7), H, V, F, CbFLAG, Y/Cr/Cb (0–7)					
Setup Time	14	10			ns
Hold Time	15	4			ns
Y/Cr/Cb Output Delay	16	5		23	ns
A1–A7 Input Data, SAWR*					
Setup Time	17	10			ns
Hold Time	18	4			ns
SRD* Asserted to YCrCb Bus Driven				25	ns
SRD* Negated to YCrCb Bus 3-Stated				25	ns
MPU*, ANC* Output Delay	19	5		23	ns
D0–D7 Output Delay	20	5		23	ns
D0–D7					
Three-State Disable Time	21			25	ns
Three-State Enable Time	22			25	ns
Clock Cycle Time	23	37.04			ns
Clock Pulse Width High	24	15			ns
Clock Pulse Width Low	25	15			ns
VCC Supply Current*	ICC		220	tbd	mA

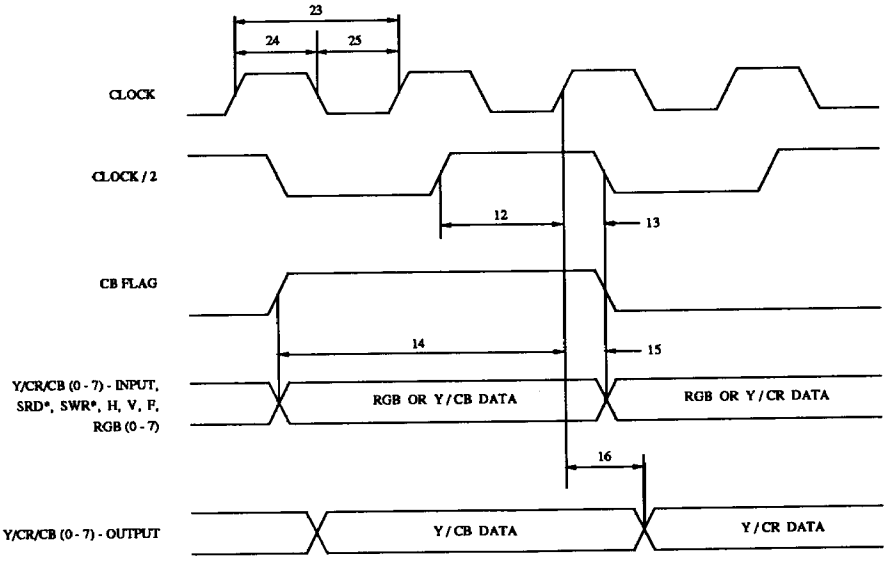
Test conditions (unless otherwise specified): "Recommended Operating Conditions." TTL input values are 0–3 V, with input rise/fall times ≤ 4 ns, measured between the 10% and 90% points. Timing reference points at 50% for inputs and outputs. ANC*, Yx, Crx/Cbx, Dx, MPU* output load ≤ 75 pF. Typical values are based on nominal temperature, i.e., room, and nominal voltage, i.e., 5 V.

*At Fmax. ICC (typ) at VCC = 5.0 V. ICC (max) at VCC (max).

Timing Waveforms

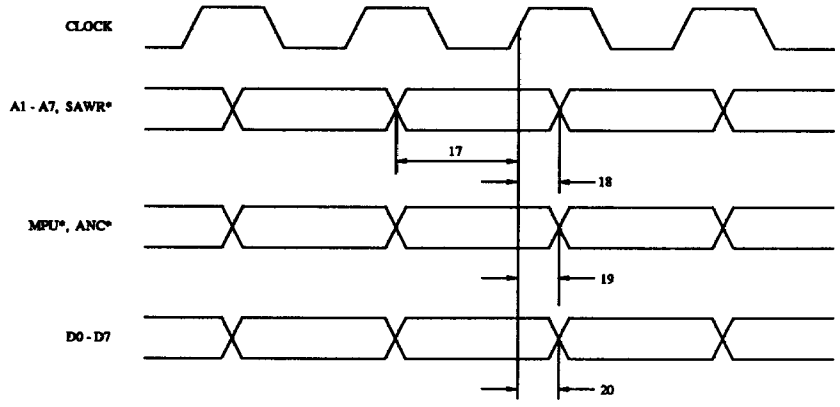


MPU Read/Write Timing.

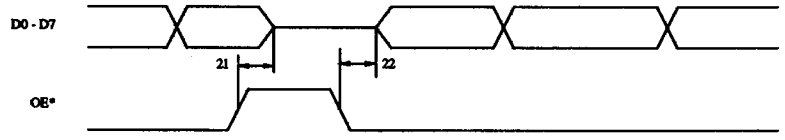


RGB, YCrCb Timing.

Timing Waveforms (continued)



A1–A7, D0–D7 Timing.



Output Enable Timing.

Ordering Information

Model Number	Package	Ambient Temperature Range
Bt291KPJ	100-pin Plastic J-Lead	0° to +70° C