Low Inductance Capacitors

Introduction

As switching speeds increase and pulse rise times decrease the need to reduce inductance becomes a serious limitation for improved system performance. Even the decoupling capacitors, that act as a local energy source, can generate unacceptable voltage spikes: V = L (di/dt). Thus, in high speed circuits, where di/dt can be quite large, the size of the voltage spike can only be reduced by reducing L.

Figure 1 displays the evolution of ceramic capacitor toward lower inductance designs over the last few years. AVX has been at the forefront in the design and manufacture of these newer more effective capacitors.

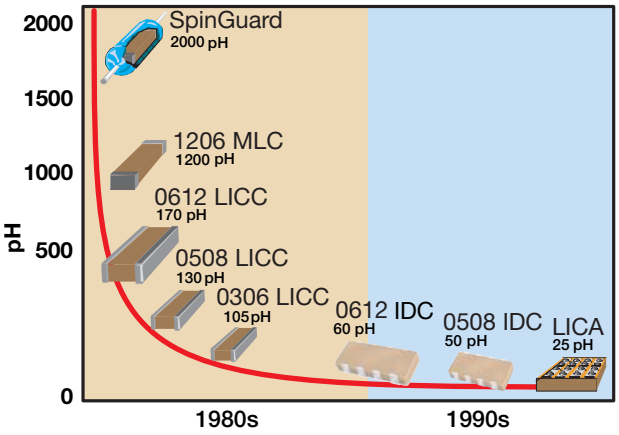


Figure 1. The evolution of Low Inductance Capacitors at AVX (values given for a 100 nF capacitor of each style)

LOW INDUCTANCE CHIP CAPACITORS

The total inductance of a chip capacitor is determined both by its length to width ratio and by the mutual inductance coupling between its electrodes. Thus a 1210 chip size has lower inductance than a 1206 chip. This design improvement is the basis of AVX's low inductance chip capacitors, LI Caps, where the electrodes are terminated on the long side of the chip instead of the short side. The 1206 becomes an 0612 as demonstrated in Figure 2. In the same manner, an 0805 becomes an 0508 and 0603 becomes an 0306. This results in a reduction in inductance from around 1200 pH for conventional MLC chips to below 200 pH for Low Inductance Chip Capacitors. Standard designs and performance of these LI Caps are given on pages 55 and 56.

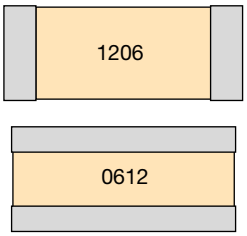
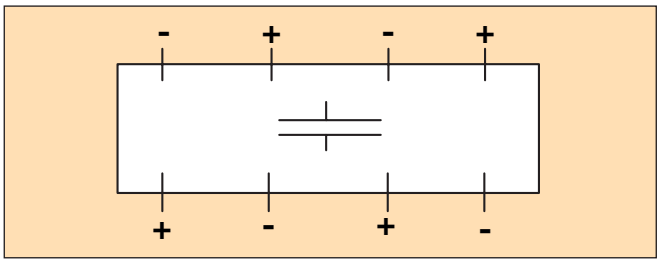


Figure 2. Change in aspect ratio: 1206 vs. 0612

INTERDIGITATED CAPACITORS

Multiple terminations of a capacitor will also help in reducing the parasitic inductance of the device. The IDC is such a device. By terminating one capacitor with 8 connections the ESL can be reduced even further. The measured inductance of the 0612 IDC is 60 pH, while the 0508 comes in around 50 pH. These FR4 mountable devices allow for even higher clock speeds in a digital decoupling scheme. Design and product offerings are shown on pages 59 and 60.



LOW INDUCTANCE CHIP ARRAYS (LICA®)

Further reduction in inductance can be achieved by designing alternative current paths to minimize the mutual inductance factor of the electrodes (Figure 3). This is achieved by AVX's LICA® product which was the result of a joint development between AVX and IBM. As shown in Figure 4, the charging current flowing out of the positive plate returns in the opposite direction along adjacent negative plates. This minimizes the mutual inductance.

The very low inductance of the LICA capacitor stems from the short aspect ratio of the electrodes, the arrangement of the tabs so as to cancel inductance, and the vertical aspect of the electrodes to the mounting surface.

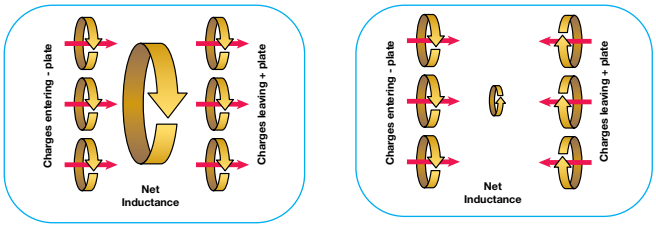


Figure 3. Net Inductance from design. In the standard Multilayer capacitor, the charge currents entering and leaving the capacitor create complementary flux fields, so the net inductance is greater. On the right, however, if the design permits the currents to be opposed, there is a net cancellation, and the inductance is much lower.

Introduction

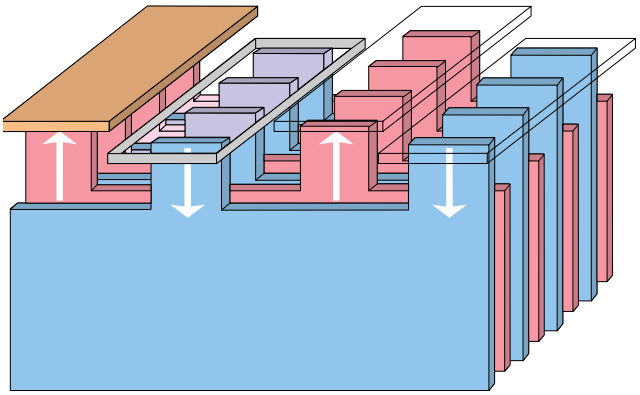


Figure 4. LICA's Electrode/Termination Construction. The current path is minimized – this reduces self-inductance. Current flowing out of the positive plate, returns in the opposite direction along the adjacent negative plate – this reduces the mutual inductance.

Also the effective current path length is minimized because the current does not have to travel the entire length of both electrodes to complete the circuit. This reduces the self inductance of the electrodes. The self inductance is also minimized by the fact that the charging current is supplied by both sets of terminals reducing the path length even further!

The inductance of this arrangement is less than 30 pH, causing the self-resonance to be above 100 MHz for the same popular 100 nF capacitance. Parts available in the LICA design are shown on pages 60 and 61.

Figure 5 compares the self resonant frequencies of various capacitor designs versus capacitance values. The approximate inductance of each style is also shown.

Active development continues on low inductance capacitors. C4 termination with low temperature solder is now available for plastic packages. Consult AVX for details.

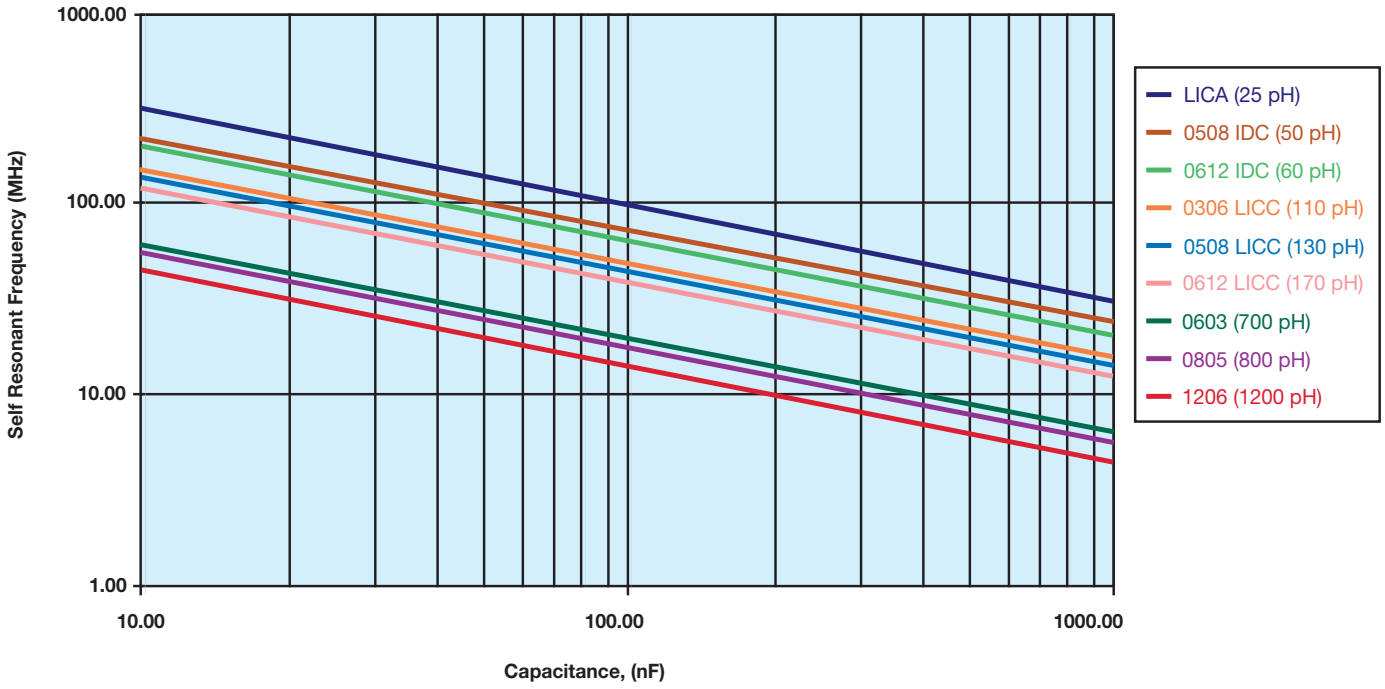
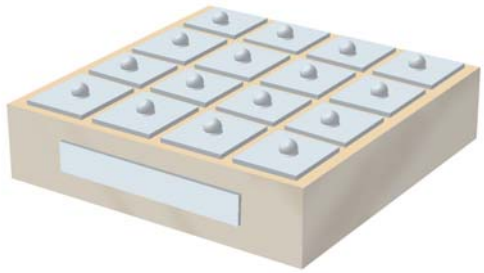


Figure 5. Self Resonant Frequency vs. Capacitance and Capacitor Design

Low Inductance Capacitors

LICA® (Low Inductance Decoupling Capacitor Arrays)



LICA® arrays utilize up to four separate capacitor sections in one ceramic body (see Configurations and Capacitance Options). These designs exhibit a number of technical advancements:

Low Inductance features–

- Low resistance platinum electrodes in a low aspect ratio pattern
- Double electrode pickup and perpendicular current paths
- C4 "flip-chip" technology for minimal interconnect inductance

HOW TO ORDER

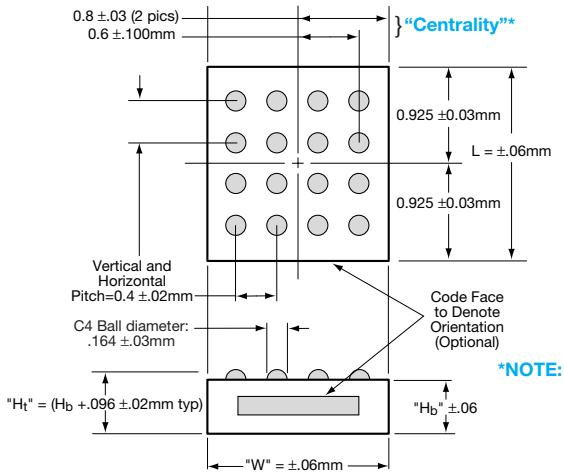
LICA	3	T	102	M	3	F	C	4	A	A
Style & Size	**Voltage** 5V = 9 10V = Z 25V = 3	**Dielectric** D = X5R T = T55T S = High K T55T	**Cap/Section (EIA Code)** 102 = 1000 pF 103 = 10 nF 104 = 100 nF	**Capacitance Tolerance** M = ±20% P = GMV	**Height Code** 6 = 0.500mm 3 = 0.650mm 1 = 0.875mm 5 = 1.100mm 7 = 1.600mm	**Termination** F = C4 Solder Balls- 97Pb/3Sn H = C4 Solder Balls Low ESR P = Cr-Cu-Au N = Cr-Ni-Au X = None	**Reel Packaging** M = 7" Reel R = 13" Reel 6 = 2"x2" Waffle Pack 8 = 2"x2" Black Waffle Pack 7 = 2"x2" Waffle Pack w/ termination facing up A = 2"x2" Black Waffle Pack w/ termination facing up C = 4"x4" Waffle Pack w/ clear lid	**# of Caps/Part** 1 = one 2 = two 4 = four	**Inspection Code** A = Standard B = Established Reliability Testing	**Code Face** A = Bar B = No Bar C = Dot, S55S Dielectrics D = Triangle

NOTE: Contact factory for availability of Termination and Tolerance Options for Specific Part Numbers.

TABLE 1

Typical Parameters	T55T	Units
Capacitance, 25°C	Co	Nanofarads
Capacitance, 55°C	1.4 x Co	Nanofarads
Capacitance, 85°C	0.7 x Co	Nanofarads
Dissipation Factor 25°	15	Percent
ESR	20	Megohms
DC Resistance	0.2	Ohms
IR (Minimum @25°)	2.0	Megaohms
Dielectric Breakdown, Min	500	Volts
Thermal Coefficient of Expansion	8.5	ppm/°C 25-100°
Inductance: (Design Dependent)	30	Pico-Henries
Frequency of Operation	DC to 5 Gigahertz	
Ambient Temp Range	-55° to 125°C	

C4 AND PAD DIMENSIONS



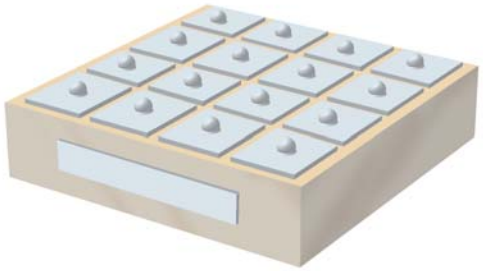
*NOTE: The C4 pattern will be within 0.1mm of the center of the LICA body, in both axes.

Pin A1 is the lower left hand ball.

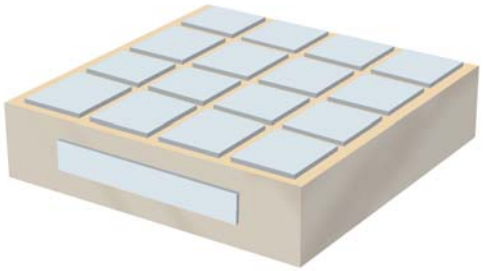
Code (Body Height)	Width (W)	Length (L)	Height Body (H_b)
1	1.600mm	1.850mm	0.875mm
3	1.600mm	1.850mm	0.650mm
5	1.600mm	1.850mm	1.100mm
6	1.600mm	1.850mm	0.500mm
7	1.600mm	1.850mm	1.600mm

TERMINATION OPTIONS

C4 SOLDER (97% Pb/3% Sn) BALLS



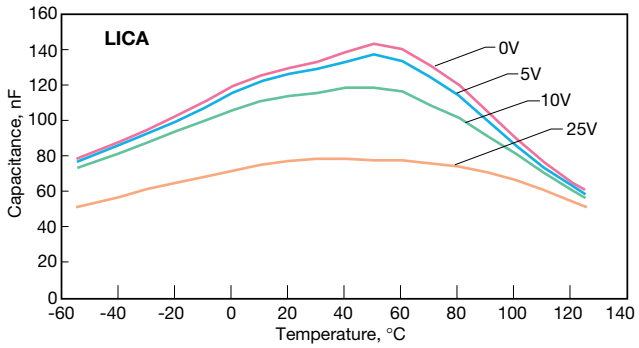
TERMINATION OPTION P OR N



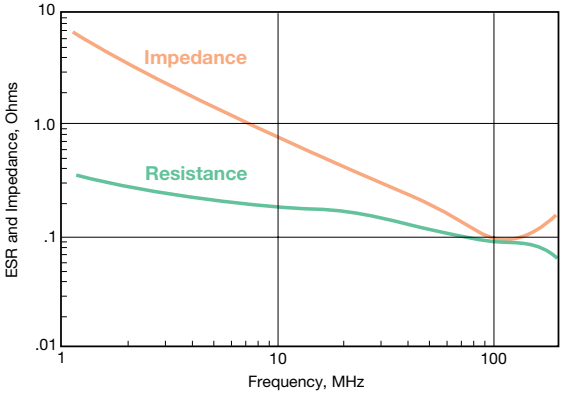
Low Inductance Capacitors

LICA® (Low Inductance Decoupling Capacitor Arrays)

LICA® TYPICAL PERFORMANCE CURVES



Effect of Bias Voltage and Temperature on a 130 nF LICA® (T55T)



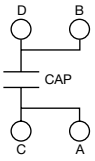
Impedance vs. Frequency

LICA VALID PART NUMBER LIST

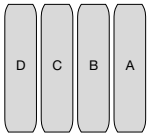
Part Number	Voltage	Thickness (mm)	Capacitors per Package
LICA3T193M3FC4AA	25	0.650	4
LICA3T153P3FC4AA	25	0.650	4
LICA3T134M1FC1AA	25	0.875	1
LICA3T104P1FC1AA	25	0.875	1
LICA3T333M1FC4AA	25	0.875	4
LICA3T263P3FC4AA	25	0.650	4
LICA3T244M5FC1AA	25	1.100	1
LICA3T194P5FC1AA	25	1.100	1
LICA3T394M7FC1AB	25	1.600	1
LICA3T314P7FC1AB	25	1.600	1
Extended Range			
LICAZT623M3FC4AB	10	0.650	4
LICA3T104M3FC1A	25	0.650	1
LICA3T803P3FC1A	25	0.650	1
LICA3T503M3FC2A	25	0.650	2
LICA3T403P3FC2A	25	0.650	2
LICA3S253M3FC4A	25	0.650	4
LICAZD753M3FC4AD	10	0.650	4
LICAZD504M3FC1AB	10	0.650	1
LICAZD604M7FC1AB	10	1.600	1
LICA3D193M3FC4AB	25	0.650	4

CONFIGURATION

Schematic



Code Face



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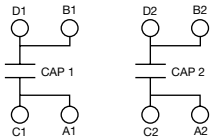

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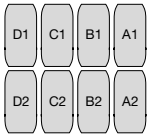

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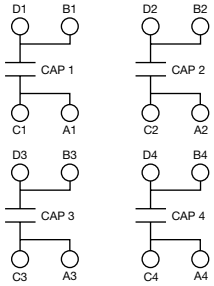

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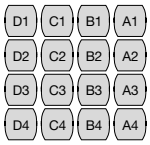
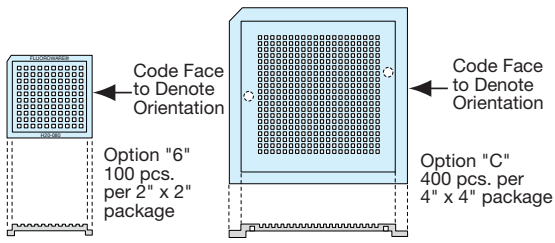


WAFFLE PACK OPTIONS FOR LICA®



Note: Standard configuration is Termination side down

LICA® PACKAGING SCHEME "M" AND "R"

8mm conductive plastic tape on reel:
"M"=7" reel max. qty. 3,000, "R"=13" reel max. qty. 8,000