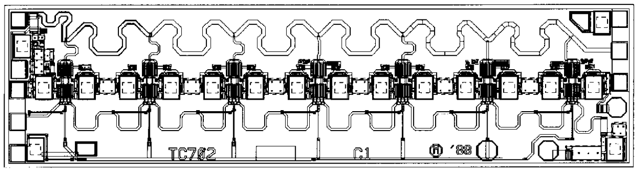
HMMC-5027

2–26.5 GHz Medium Power Amplifier

AVAGO TECHNOLOGIES

Data Sheet



Chip Size:	2980 x 770 µm (117.3 x 30.3 mils)
Chip Size Tolerance:	±10 µm (±0.4 mils)
Chip Thickness:	127 ± 15 µm (5.0 ± 0.6 mils)
Pad Dimensions:	75 x 75 µm (2.95 x 2.95 mils), or larger

Description

The HMMC-5027 is a broadband GaAs MMIC Traveling Wave Amplifier designed for medium output power and moderate gain over the full 2 to 26.5 GHz frequency range. Seven MESFET cascode stages provide a flat gain response, making the HMMC-5027 an ideal wideband power block. Optical lithography is used to produce gate lengths of ≈0.5 µm. The HMMC-5027 incorporates advanced MBE technology, Ti-Pt-Au gate metallization, silicon nitride passivation, and polyimide for scratch protection.

Features

- **Wide-frequency range: 2–26.5 GHz**
- **Moderate gain: 7 dB**
- **Gain flatness: ± 1 dB**
- **Return loss:**
  Input: -13 dB
  Output: -11 dB
- **Low-frequency operation capability: <2 GHz**
- **Gain control: 30 dB dynamic range**
- **Medium power:**
  20 GHz: P_{-1dB}: 22 dBm
  P_{sat}: 24 dBm
  26.5 GHz: P_{-1dB}: 19 dBm
  P_{sat}: 21 dBm

Absolute Maximum Ratings[1]

Symbol	Parameters/Conditions	Units	Min.	Max.
V_{DD}	Positive Drain Voltage	V		8.0
I_{DD}	Total Drain Current	mA		300
V_{G1}	First Gate Voltage	V	-5	0
I_{G1}	First Gate Current	mA	-1	+1
V_{G2}	Second Gate Voltage	V	-2.5	+5
I_{G2}	Second Gate Current	mA	-25	
P_{DC}	DC Power Dissipation	watts		2.4
P_{in}	CW Input Power	dBm		23
T_{ch}	Operating Channel Temp.	°C		+150
T_{case}	Operating Case Temp.	°C	-55	
T_{stg}	Storage Temp.	°C	-65	+165
T_{max}	Max. Assembly Temp. (for 60 seconds max.)	°C		300

Notes:

1. Operation in excess of any one of these conditions may result in permanent damage to this device. T_A = 25°C except for T_{ch}, T_{STG}, and T_{max}.

HMMC-5027 DC Specifications/Physical Properties[1]

Symbol	Parameters and Test Conditions	Units	Min.	Typ.	Max.
I_{DSS}	Saturated Drain Current (V_{DD} = 8.0 V, V_{G1} = 0 V, V_{G2} = open circut)	mA	200	300	500
V_p	First Gate Pinch-Off Voltage (V_{DD} = 8.0 V, I_{DD} = 30 mA, V_{G2} = open circut)	V	-2.2	-1.3	-0.5
V_{G2}	Secong Gate Self-Bias Voltage (V_{DD} = 8.0 V, V_{G1} = 0.0 V)	V		1.8 (0.27 x V_{DD})	
$I_{DSOFF}(V_{G1})$	First Gate Pinch-Off Current (V_{DD} = 8.0 V, V_{G1} = -3.5 V, V_{G2} = open circut)	mA		7	
$I_{DSOFF}(V_{G2})$	Second Gate Pinch-Off Current (V_{DD} = 5.0 V, V_{G1} = 0 V, V_{G2} = -3.5V)	mA		10	
$\theta_{ch\text{-}bs}$	Thermal Resistance ($T_{backside}$ = 25°C)	°C/W		28	

Notes:
1. Measured in wafer form withT_{chuck} = 25°C. (Except $\theta_{ch\text{-}bs}$.)

RF Specifications[1] (V_{DD} = 8.0 V, $I_{DD}(Q)$ = 250 mA, or I_{DSS}, $Z_{in} = Z_o = 50\Omega$)

Symbol	Parameters and Test Conditions	Units	Min.	Typ.	Max.
BW	Guaranteed Bandwidth[2]	GHz	2		26.5
S_{21}	Small Signal Gain	dB	6	7	
ΔS_{21}	Small Signal Gain Flatness	dB		±0.8	
RL_{in}	Input Return Loss	dB		-13	-10
RL_{out}	Output Return Loss	dB		-11	-10
S_{12}	Reverse Isolation	dB		-28	-25
P_{-1dB}	Output Power at 1dB Gain Compression	dBm	16.5	19	
P_{sat}	Saturated Output Power	dBm	18.5	21	
H_2	Second Harmonic ($2 < f_o < 20$) $P_o(f_o)$ = 21 dBm or P_{-1dB} whichever is less	dBc		-21	-18
H_3	Third Harmonic ($2 < f_o < 20$) $P_o(f_o)$ = 21 dBm or P_{-1dB} whichever is less	dBc		-32	-18
NF	Noise Figure	dB		11	

Notes:
1. Small-signal data measured in wafer form with T_{chuck} = 25°C. Large-signal data measured on individual devices mounted in an Avago 83040 Series Modular Microcircuit Package @ T_A = 25°C.
2. Performance may be extended to lower frequencies through the use of appropriate off-chip circuitry. Upper corner frequency ~30 GHz.

Applications

The HMMC-5027 series of traveling wave amplifiers are designed for use as general purpose wideband power stages in communication systems and microwave instrumentation. They are ideally suited for broadband applications requiring a flat gain response and excellent port matches over a 2 to 26.5 GHz frequency range. Dynamic gain control and low-frequency extension capabilities are designed into these devices.

Biasing and Operation

These amplifiers are biased with a single positive drain supply (V_{DD}) and a single negative gate supply (V_{G1}). The recommended bias conditions for the HMMC-5027 are V_{DD} = 8.0V, I_{DD} = 250 mA or I_{DSS}, whichever is less. To achieve this drain current level, V_{G1} is typically biased between 0V and -0.6V. No other bias supplies or connections to the device are required for 2 to 26.5 GHz operation. The gate voltage (V_{G1}) **MUST** be applied prior to the drain voltage (V_{DD}) during power up and removed after the drain voltage during power down. See Figure 3 for assembly information.

The HMMC-5027 is a DC coupled amplifier. External coupling capacitors are needed on RF_{IN} and RF_{OUT} ports. The drain bias pad is connected to RF and must be decoupled to the lowest operating frequency. The auxiliary gate and drain contacts are provided when performance below 1 GHz is required. Connect external capacitors to ground to maintain input and output VSWR at low frequencies (see Additional References). Do not apply bias to these pads.

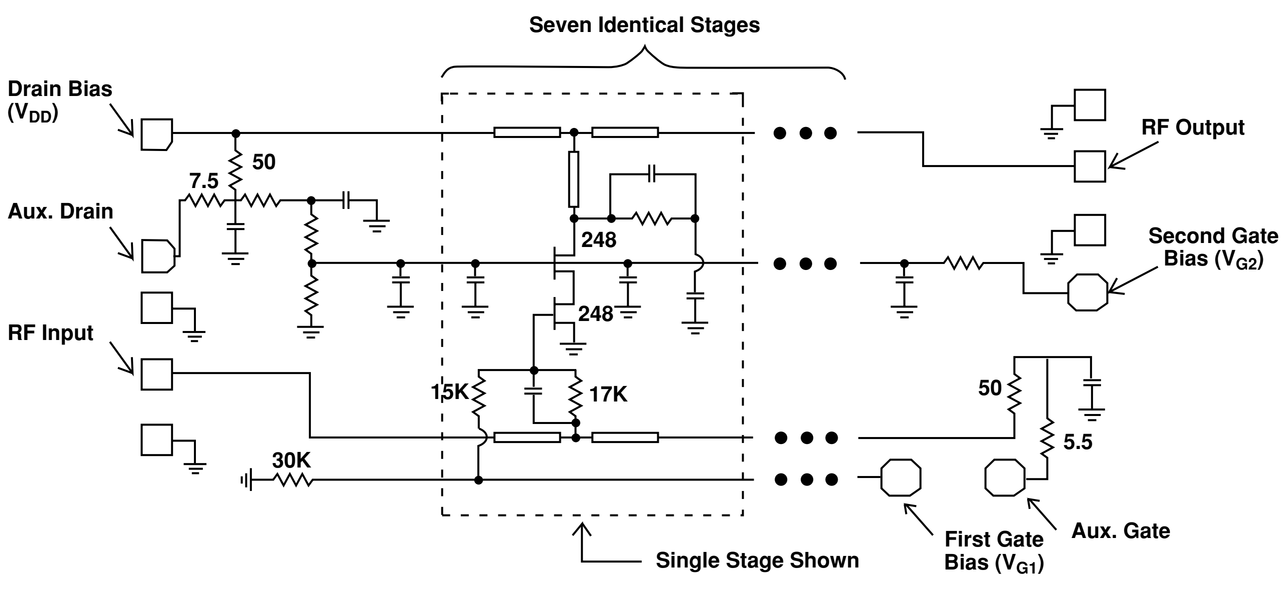
The second gate (V_{G2}) can be used to obtain 30 dB (typical) dynamic gain control. For normal operation, no external bias is required on this contact and its self-bias potential is between +1.5 and +2.5 volts. Applying an external bias between its open circuit potential and -2.5 volts will adjust the gain while maintaining a good input/output port match.

Assembly Techniques

GaAs MMICs are ESD sensitive. ESD preventive measures must be employed in all aspects of storage, handling, and assembly. MMIC ESD precautions, handling considerations, die attach and bonding methods are critical factors in successful GaAs MMIC performance and reliability. Avago application note #54, “GaAs MMIC ESD, Die Attach and Bonding Guidelines” provides basic information on these subjects.

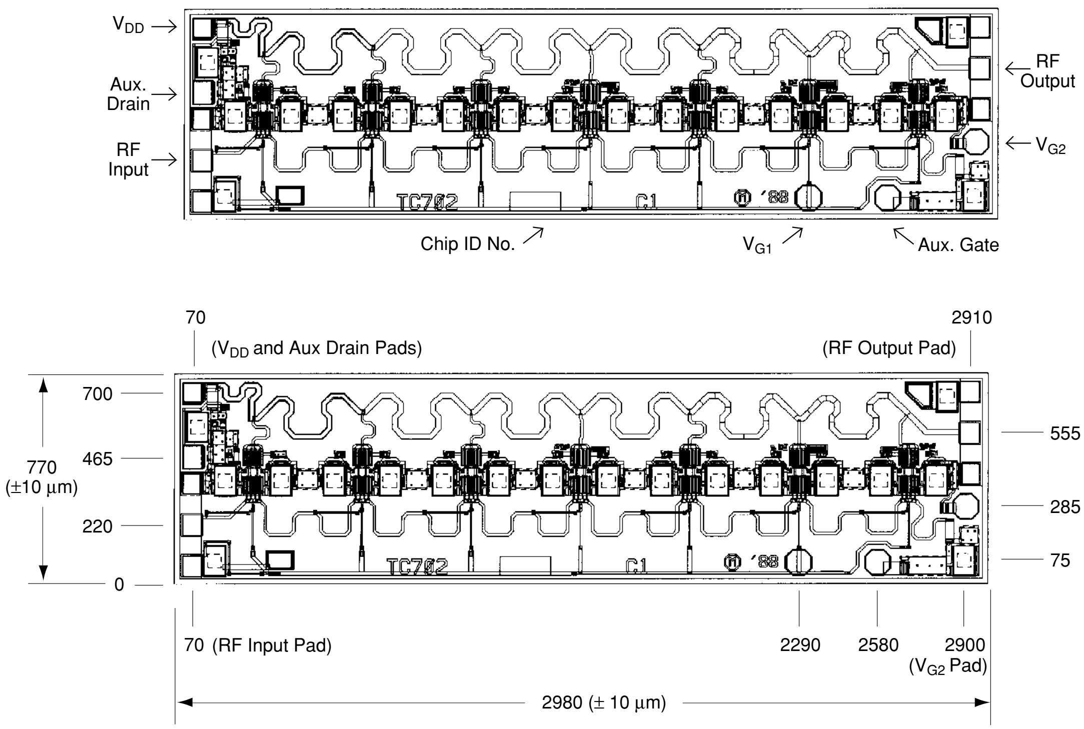
Additional References:

AN# 34, “HMMC-5021/22/26/27 TWA Environmental Data,” AN#1053, “Designing with HMMC-5021/-5022/-5026 and/ -5027 GaAs MMIC Amplifiers.”



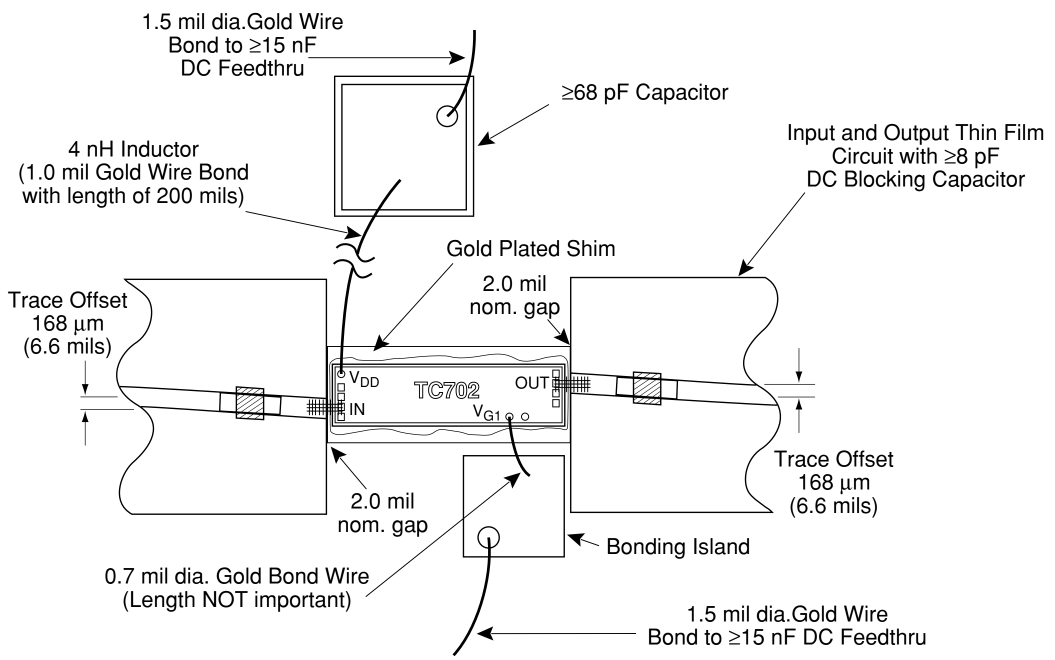
Notes:
FET gate periphery in microns.
All resistors in ohms. (Ω),
(or in K-ohms, where indicated)

Figure 1. Schematic.



Notes:
All dimensions in microns.
Rectangular Pad Dim: 75 x 75 µm.
Octagonal Pad Dim: 90 µm dia.
All other dimensions ±5 µm (unless otherwise noted).
Chip thickness: 127 ± 15 µm.

Figure 2. Bonding Pad Locations.



Note:
Total offset between RF input and RF output pad is 335 µm (13.2 mils).

Figure 3. Assembly Diagram. (For 2.0 – 26.5 GHz Operation)

HMMC-5027 Typical Performance

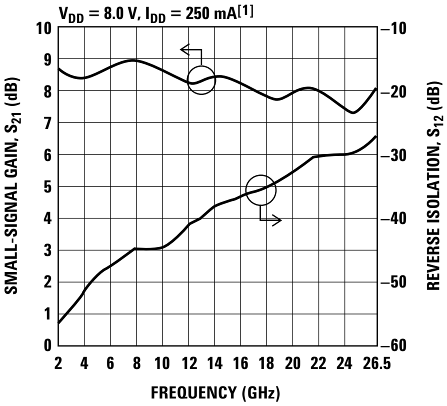


Figure 4. Typical Gain and Reverse Isolation vs. Frequency.

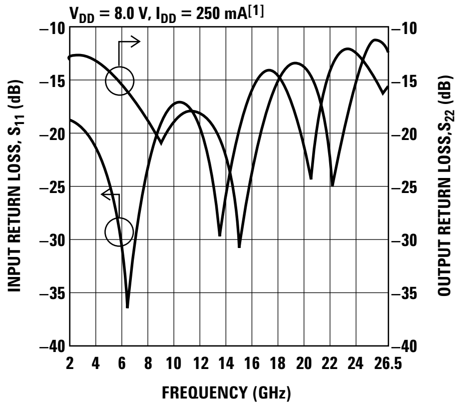


Figure 5. Typical Input and Output Return Loss vs. Frequency.

HMMC-5027 Typical Scattering Parameters[1],

(T_{chuck} = 25°C, V_{DD} = 8.0 V, I_{DD} = 250 mA or I_{DSS}, whichever is less, $Z_{in} = Z_o$ = 50Ω)

Freq.	S_{11}			S_{12}			S_{21}			S_{22}		
GHz	dB	Mag	Ang	dB	Mag	Ang	dB	Mag	Ang	dB	Mag	Ang
2.0	-18.7	0.116	-139.5	-57.7	0.0013	-165.2	8.7	2.717	116.6	-13.0	0.223	173.5
3.0	-20.1	0.099	-159.0	-54.9	0.0018	144.2	8.4	2.635	94.8	-13.0	0.224	150.0
4.0	-21.5	0.084	-175.7	-52.0	0.0025	154.0	8.3	2.612	72.0	-13.5	0.212	127.1
5.0	-24.6	0.059	167.8	-49.9	0.0032	111.3	8.4	2.634	48.2	-14.0	0.200	101.6
6.0	-32.0	0.025	167.4	-48.2	0.0039	91.3	8.6	2.699	23.3	-15.3	0.171	71.7
7.0	-30.8	0.029	-94.8	-46.9	0.0045	74.9	8.8	2.763	-3.5	-16.9	0.143	39.5
8.0	-22.7	0.073	-103.2	-45.5	0.0053	21.0	8.8	2.768	-30.9	-18.4	0.120	-2.2
9.0	-18.9	0.114	-121.5	-45.2	0.0055	10.3	8.8	2.744	-58.9	-21.3	0.086	-46.9
10.0	-17.2	0.137	-142.6	-44.7	0.0058	-15.5	8.5	2.673	-85.9	-18.9	0.114	-90.7
11.0	-17.4	0.135	-163.9	-43.5	0.0067	-33.4	8.3	2.608	-112.5	-17.9	0.127	-129.6
12.0	-19.3	0.108	175.6	-41.5	0.0084	-45.4	8.2	2.564	-138.5	-18.2	0.123	-162.6
13.0	-25.6	0.052	170.3	-40.6	0.0093	-75.8	8.2	2.578	-164.9	-19.3	0.108	163.4
14.0	-27.0	0.045	-113.0	-38.6	0.0118	-95.9	8.3	2.610	167.1	-22.1	0.078	126.5
15.0	-19.2	0.109	-111.0	-37.8	0.0129	-124.7	8.3	2.605	138.4	-31.2	0.028	56.7
16.0	-15.6	0.167	-127.9	-37.1	0.0139	-149.1	8.2	2.574	108.8	-23.5	0.067	-33.3
17.0	-14.3	0.193	-148.4	-36.3	0.0153	-174.5	8.0	2.510	79.7	-18.1	0.124	-80.7
18.0	-14.8	0.182	-166.6	-35.8	0.0163	164.1	7.8	2.444	50.9	-15.2	0.174	-115.2
19.0	-17.1	0.140	-179.3	-34.7	0.0185	141.5	7.7	2.418	22.1	-13.7	0.207	-147.6
20.0	-21.4	0.086	-166.2	-32.9	0.0227	112.6	7.8	2.466	-7.5	-13.9	0.202	177.9
21.0	-18.4	0.121	-129.5	-31.6	0.0262	80.7	8.1	2.527	-39.9	-16.8	0.145	136.7
22.0	-13.8	0.205	-137.2	-30.9	0.0285	42.7	8.0	2.512	-74.0	-25.3	0.054	66.9
23.0	-12.1	0.247	-152.7	-30.6	0.0296	13.3	7.6	2.395	-108.4	-19.8	0.102	-56.2
24.0	-12.3	0.244	-169.8	-30.3	0.0304	-15.5	7.4	2.344	-142.5	-13.7	0.207	-103.5
25.0	-14.7	0.184	-175.8	-29.7	0.0329	-44.9	7.3	2.315	-175.6	-11.3	0.272	-136.7
26.0	-16.7	0.146	-149.3	-28.5	0.0375	-78.1	7.9	2.469	148.1	-11.7	0.259	-171.3
26.5	-14.1	0.197	-141.6	-28.0	0.0399	-98.5	8.0	2.503	126.9	-13.0	0.223	172.3

Note:

1. Data obtained from on-wafer measurements.

HMMC-5027 Typical Temperature Performance

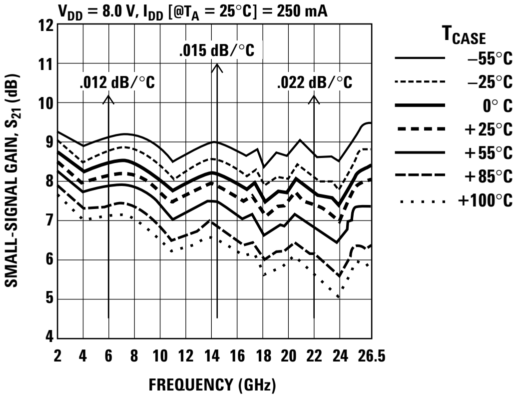


Figure 6. Typical Small-Signal Gain vs. Temperature.

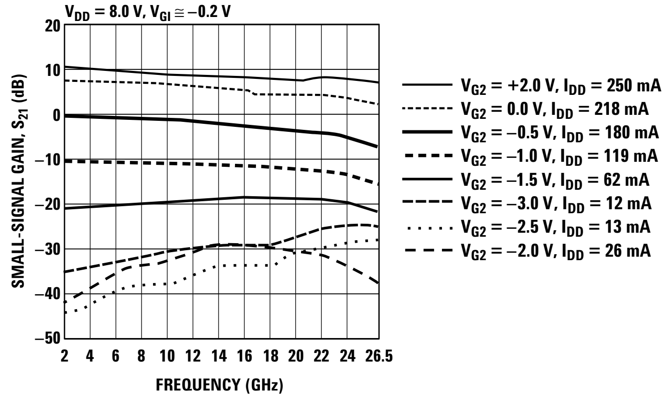


Figure 7. Typical Gain vs. Second Gate Control Voltage.

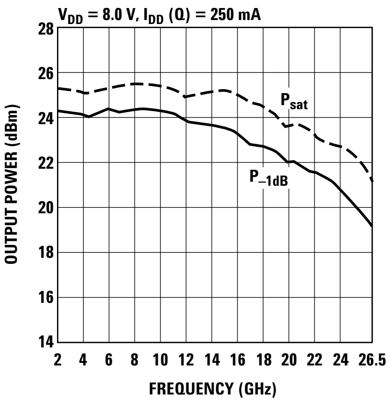


Figure 8. Typical 1 dB Gain Compression and Saturated Output Power vs. Frequency.

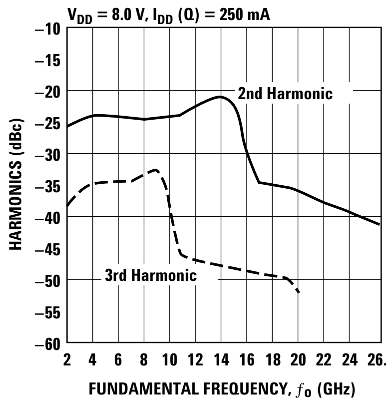


Figure 9. Typical Second and Third Harmonic vs. Fundamental Frequency at P_{OUT} = +21 dBm.

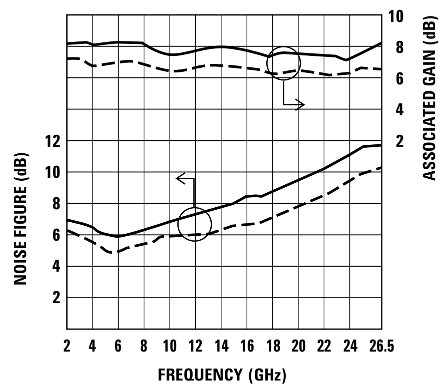


Figure 10. Typical Noise Figure Performance.

Nominal Bias: V_{DD} = 8.0 V, I_{DD} = 250 mA

Optimal NF Bias: V_{DD} = 6.5 V, I_{DD} = 130 mA

Note:
1. All data measured on individual devices mounted in an HP83040 Series Modular Microcircuit Package @ T_A = 25°C (except where noted).

This data sheet contains a variety of typical and guaranteed performance data. The information supplied should not be interpreted as a complete list of circuit specifications. In this data sheet the term *typical* refers to the 50th percentile performance. For additional information contact your local Avago Technologies' sales representative.

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