

41MG and 41MP Quad Differential Line Drivers

Features

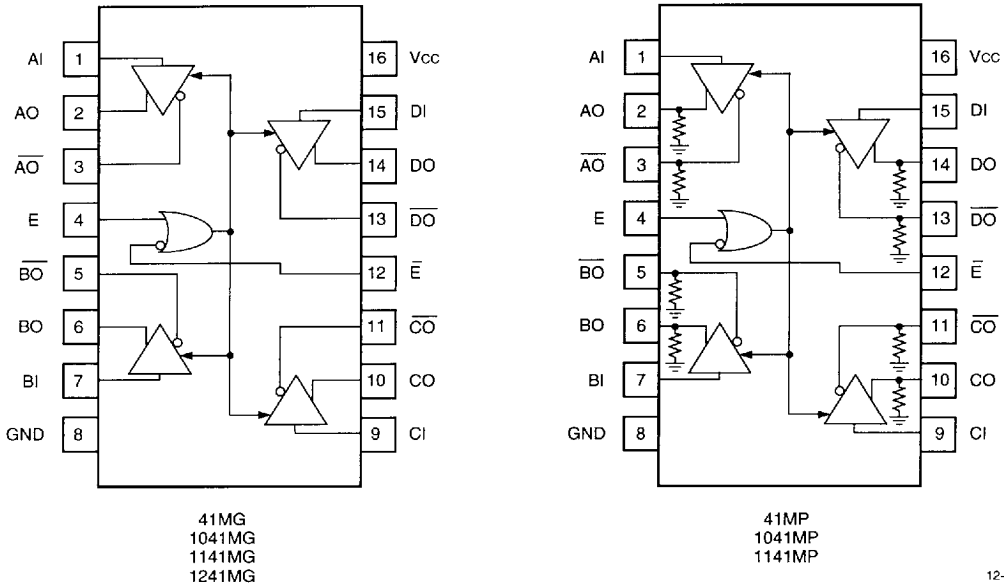
- Pin-equivalent to the general-trade 26LS31 device, with improved speed, reduced power consumption, and significantly lower levels of EMI
- Four line drivers per package
- Logic which converts TTL input logic levels to differential, pseudo-ECL output logic levels
- 200 Mbits/s or 400 Mbits/s maximum data rates when used with the 41Lx and 41Mx receivers respectively
- Meets ESDI standards
- No line loading when $V_{CC} = 0$ V
- High output drive for 50 Ω lines
- 200 mA short-circuit current (typical)
- 2 ns maximum propagation delay
- <0.2 ns output skew (typical)
- 0 °C to 85 °C ambient operating temperature range (See Section 9.)
- Single 5 V supply

Description

The 41MG and 41MP Quad Differential Line Driver integrated circuits transmit digital data over balanced transmission lines. They translate input TTL levels to differential, pseudo-emitter-coupled logic (pseudo-ECL) output levels. All devices in this family have four drivers with a common enable control. The 41MG and 41MP line drivers are compatible with many receivers, including the AT&T 41 Series receivers and transceivers and the general-trade 26LS32 device. The 41MG devices require the customer to supply external termination resistors on the circuit board. The 41MP devices have internal 220 Ω termination resistors to ground on each driver output. The 41MG/41MP drivers are pin-equivalent to the general-trade 26LS31 devices but offer increased speed, reduced power consumption, and significantly lower levels of electromagnetic interference (EMI).

The packaging options that are available for the quad differential line drivers include a 16-pin DIP (41MG, 41MP), a 16-pin J-lead SOJ (1041MG, 1041MP), a 16-pin gull-wing SOIC (1141MG, 1141MP), and a 16-pin narrow-body gull-wing SOIC (1241MG).

Pin Information



12-2038C

Note: The device is disabled when $E = 0$ and $\bar{E} = 1$.

Figure 3-3. 41MG and 41MP Logic Diagrams

Absolute Maximum Ratings

Stresses in excess of the Absolute Maximum Ratings can cause permanent damage to the device. These are absolute stress ratings only. Functional operation of the device is not implied at these or any other conditions in excess of those given in the operational sections of the data sheet. Exposure to Absolute Maximum Ratings for extended periods can adversely affect device reliability.

Parameter	Symbol	Min	Max	Unit
Power Supply Voltage	V _{cc}	—	7.0	V
Ambient Operating Temperature	T _A	0	85	°C
Storage Temperature	T _{stg}	-40	125	°C

Handling Precautions

CAUTION: This device is susceptible to damage as a result of electrostatic discharge. Take proper precautions during both handling and testing. Follow guidelines such as JEDEC Publication No. 108-A (Dec. 1988).

AT&T employs a human-body model (HBM) for ESD-susceptibility testing and protection-design evaluation.
3-10

ESD voltage thresholds are dependent on the critical parameters used to define the model. The standard HBM (resistance = 1.5 kΩ, capacitance = 100 pF) is used. The HBM ESD threshold voltage presented here was obtained using this circuit.

Device	Rating
41MG/41MP Drivers	>1000 V

0050026 0011290 744

Electrical Characteristics

Table 3-7. 41MG and 41MP Power Supply Current Characteristics

$T_A = 0\text{ }^{\circ}\text{C}$ to $85\text{ }^{\circ}\text{C}$, $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$.

Parameter	Symbol	Min	Typ	Max	Unit
Power Supply Current:					
41MG*					
All Outputs Disabled	I_{CC}	—	60	90	mA
All Outputs Enabled	I_{CC}	—	35	55	mA
41MP†					
All Outputs Disabled	I_{CC}	—	130	180	mA
All Outputs Enabled	I_{CC}	—	160	230	mA

* Measured with no load

† The additional power dissipation is the result of integrating the termination resistors into the device. I_{CC} is measured with a $100\text{ }\Omega$ resistor across the driver outputs

Table 3-8. 41MG and 41MP Voltage and Current Characteristics

$T_A = 0\text{ }^{\circ}\text{C}$ to $85\text{ }^{\circ}\text{C}$.

Parameter	Symbol	Min	Typ	Max	Unit
Output Voltages, $V_{CC} = 4.5\text{ V}$:					
Low, $I_{OL} = -8.0\text{ mA}^*$	V_{OL}	—	3.0	$V_{OH} - 0.8^\dagger$	V
High, $I_{OH} = -40.0\text{ mA}^*$	V_{OH}	3.0	4.0	—	V
High Z, $I_{OH} = -1.0\text{ mA}$, $V_{CC} = 4.75\text{ V}$	V_{OZ}	—	2.0	$V_{OL} - 0.02$	V
Input Voltages:					
Low, $V_{CC} = 5.5\text{ V}$	V_{IL}^\ddagger	—	—	0.8	V
High, $V_{CC} = 4.5\text{ V}$	V_{IH}^\ddagger	2.0	—	—	V
Clamp, $V_{CC} = 4.5\text{ V}$, $I_{IN} = -5.0\text{ mA}$	V_{IK}	—	—	-1.5	V
Short-circuit Output Current, $V_{CC} = 5.5\text{ V}$	I_{OS}^\S	-100	-250	-350	mA
Input Currents, $V_{CC} = 5.5\text{ V}$:					
Low, $V_{IN} = 0.4\text{ V}$	I_{IL}	—	—	-400	μA
High, $V_{IN} = 2.7\text{ V}$	I_{IH}	—	—	20	μA
Reverse, $V_{IN} = 5.5\text{ V}$	I_{IH}	—	—	100	μA
Output Resistors (41MP)	R_O	—	220	—	Ω

* Typical value of the output current for the 41LG and the 41MP when terminated per Figure 6-5

† V_{OL} must be a minimum of 0.8 V less than its complementary output for $V_{CC\text{ MIN}} = 4.75\text{ V}$

‡ The input levels provide zero noise immunity and should be tested only in a static, noise-free environment

§ Test must be performed one lead at a time to prevent damage to the device

Timing Characteristics

Table 3-9. 41MG and 41MP Timing Characteristics (See Figures 6-1 and 6-2.)

Propagation-delay test circuit connected to output (see Figure 6-6).

$T_A = 25\text{ }^\circ\text{C}$, $V_{CC} = 5\text{ V}$.

Symbol	Parameter	Typ	Max	Unit
t_{P1}	Propagation Delay: Input High to Output	1.0	2.0	ns
t_{P2}		1.0	2.0	ns
t_{PHZ}	Disable Time: High to High Impedance	8	12	ns
t_{PLZ}		8	12	ns
t_{PZH}	Enable Time: High Impedance to High	8	12	ns
t_{PZL}		8	12	ns
t_{skew1}	$ t_{P1} - t_{P2} $	0.2	0.5	ns
t_{skew2}	$ t_{PHH} - t_{PHL} , t_{PLH} - t_{PLL} $	0.9	1.2	ns
Δt_{skew}	Difference Between Drivers	0.3	0.6	ns
t_{LH}	Rise Time	—	2.0	ns
t_{HL}	Fall Time	—	2.0	ns