DATA SHEET

AL2236 2.4GHz RF Transceiver

Single Chip Transceiver for 802.11bg Applications

MP Datasheet

Airoha Technology Corp.

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INDEX

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1 Features

- Highly integrated 2.4GHz band transceiver with Direct Conversion architecture
- Receiver with 38dB RF selectable gain range and 60dB baseband variable gain range
- Integrated baseband filters with programmable bandwidth for Transmitter and Receiver
- Three-wire control interface
- Integrate PA with 19/21 dBm output power for 11b and 17dBm for 11g
- Integrate RF detector for APC
- Single-ended LNA input without the need of external balun
- On-chip DC offset correction
- Embedded IQ mismatch calibration
- Two common-mode DC voltage supported at IQ signals (1.2V and 0.6V)
- Multiple reference clock frequencies supported: 20/40/22/44/26/52/19.2/38.4 MHz.
- Small QFN-40 package (5mm×5mm)

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2 Description

AL2236 is a highly integrated RF transceiver IC for 2.4GHz band 802.11b/g applications, and combines all functions of the transceiver in a single chip. AL2236 also integrates on-chip PA to help you to minimize the use of external components to design an RF subsystem.

The receive path implements a direct down-conversion architecture to eliminate additional IF filters. It includes a single-ended input Low Noise Amplifier (LNA), a direct down-conversion mixer with DC-offset cancellation, and a variable gain amplifier with a baseband low-pass filter.

The transmitter consists of a direct up-conversion quadrature modulator with a baseband low pass filter, a variable gain amplifier, a power amplifier and a power detector to complete the whole transmit path function.

A power-on calibration procedure is established to correct the TX DC offset and filters mismatch.

These functions are housed in a 40-pin QFN package.

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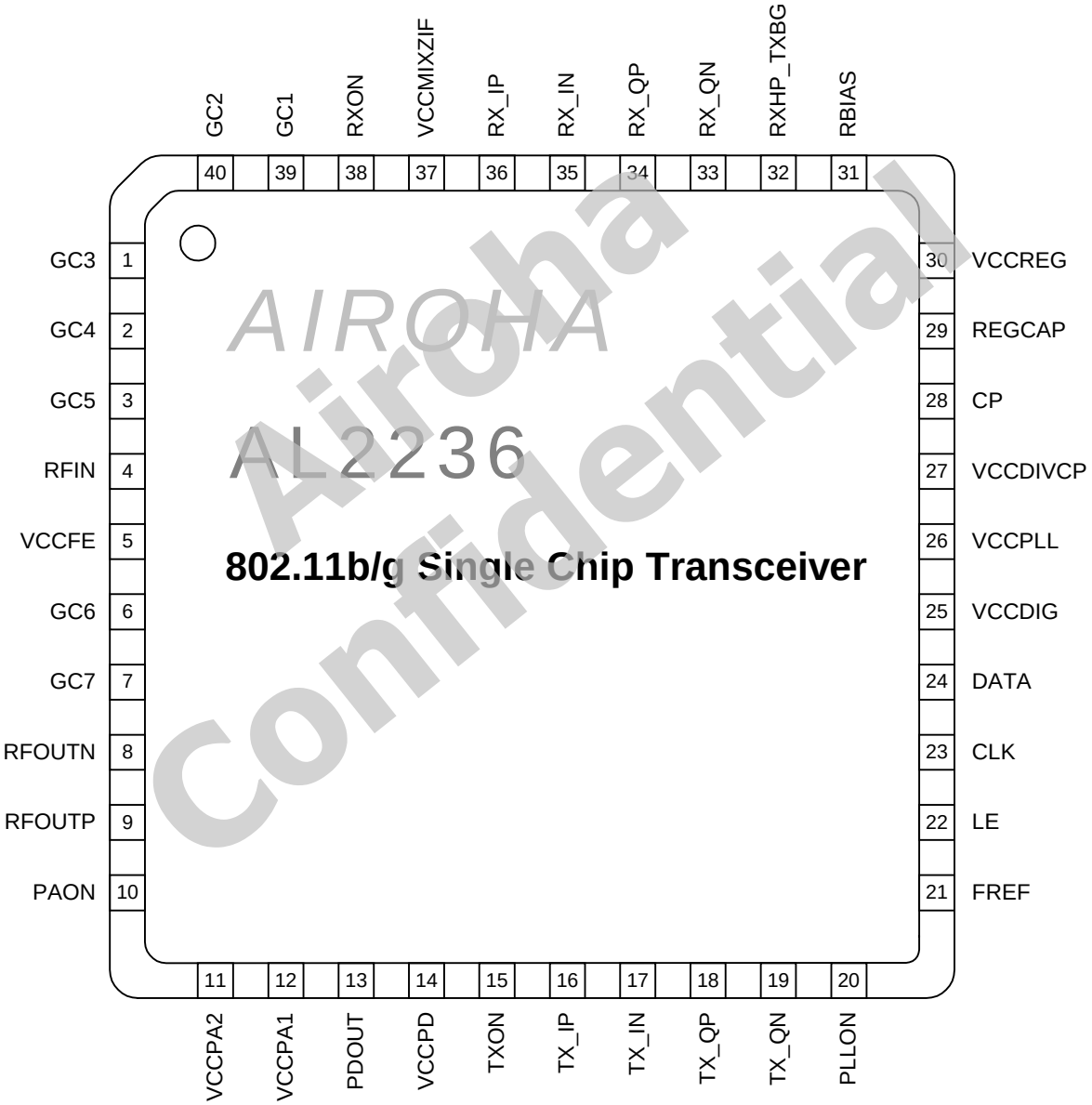
3 Pin Assignment



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4 Block Description

4.1 General Description

The AL2236 is a 2.4GHz-band transceiver for 802.11b/g applications. There are five main blocks – power amplifier, transmitter, receiver, synthesizer and three-wire interface.

The control pins: PLLON, TXON, RXON and PAON are responsible for the power control of the chip. The whole chip is powered up when PLLON is set to High, and the synthesizer is enabled at the same time. After the chip powered-up, the transmitter or receiver block is enabled when TXON or RXON being set to High, respectively. The PA block is controlled by the PAON pin independently, irrelative to the state of PLLON.

4.2 Receiver

The receiver implements a direct-conversion architecture, which is composed with two parts: RF front-end and Zero-IF baseband. The RF front-end part comprises a LNA and a quadrature mixer. The ZIF baseband part comprises a low-pass filter (LPF) for channel filtering and a variable gain amplifier (VGA).

At the RF front-end part, the LNA input is single-ended without the need of external balun. The front-end gain could be adjusted through control pins or 3-wire interface, and thus reduce the probability of bit errors caused by poor signal-to-noise ratio.

After the LNA is followed by a quadrature mixer that down-converts the RF signal directly to baseband signal. A direct-conversion architecture is implemented in order to eliminate the external SAW filters.

At the ZIF baseband part, the down-converted baseband signal is first low-pass filtered by the LPF, and then amplified by the VGA. The 3dB bandwidth of the LPF could be set from 7.5MHz to 20MHz through 3-wire interface. The VGA provides variable gain with 60dB dynamic range, and could be controlled through control pins or 3-wire interface.

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4.3 Transmitter

The transmitter implements a direct-up-conversion architecture, which comprises a LPF, a modulator and a VGA stage. The TX baseband I/Q interface is designed as differential analog inputs directly connected (DC-coupled) to the I/Q DAC outputs of the baseband IC.

A LPF is implemented to attenuate the second sidelobe of signal spectrum and unwanted oversampling clock or spurious signals. The 3dB bandwidth of the LPF could be set from 12MHz to 30MHz through 3-wire interface.

The VGA provides variable gain with more than 23dB dynamic range, and could be controlled through control pins or 3-wire interface.

4.4 PA

The gain of the power amplifier is adjustable via bias current, which is controlled through 3-wire interface. The output power is +17dBm for 11g and +19/+21 dBm for 11b.

An on-chip power detector is integrated to measure the output power strength. Power detector samples the peak voltage of the output power and generates a voltage proportional to the output power.

4.5 Synthesizer

The AL2236 includes a fractional-N synthesizer. The reference frequency is fed from an external oscillator. Multiple reference clock frequencies are supported on AL2236, including: 20/40/22/44/26/52/19.2/38.4 MHz.

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5 Electrical Characteristics

5.1 Absolute Maximum Ratings

AL2236 could be damaged by any stress in excess of the absolute maximum ratings listed below.

ITEM	MIN.	MAX.
Power supply voltage (Vcc)	-0.3V	3.6V
Pin voltage	-0.3V	3.6V
Maximum power dissipation	-	2W
Operating temperature	-40°C	+85°C
Storage temperature	-65°C	+150°C
LNA input level	-	+10 dBm
PA output load mismatch	-	10:1

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5.2 DC Electrical Specifications

Typical values are at VCC=3.3V(PA) / 2.8V(TRX), Ta=25°C unless otherwise specified

Item	Condition	Min.	Typ.	Max.	Unit
Power supply voltage	Power Amplifier	2.7	3.3	3.6	V
	Transceiver (V_{DD})	2.7	2.8		
Digital input voltage	Logic High (V_{IH})	$0.7V_{DD}$			V
	Logic Low (V_{IL})	-		$0.3V_{DD}$	
Shut down current	PLLON=L, PD1= 1		5		µA
	PLLON=L, PD1= 0		500		
Standby current	PLLON=H		41		mA
Rx current	PLLON=RXON=H		62		mA
Tx current	PLLON=TXON=H		83		mA
	PLLON=TXON=PAON=H		215/240/263 *		

Note*: 215mA under Pout 17dBm OFDM mode, 240mA under Pout 19dBm CCK mode and 263mA under Pout 21dBm CCK mode.

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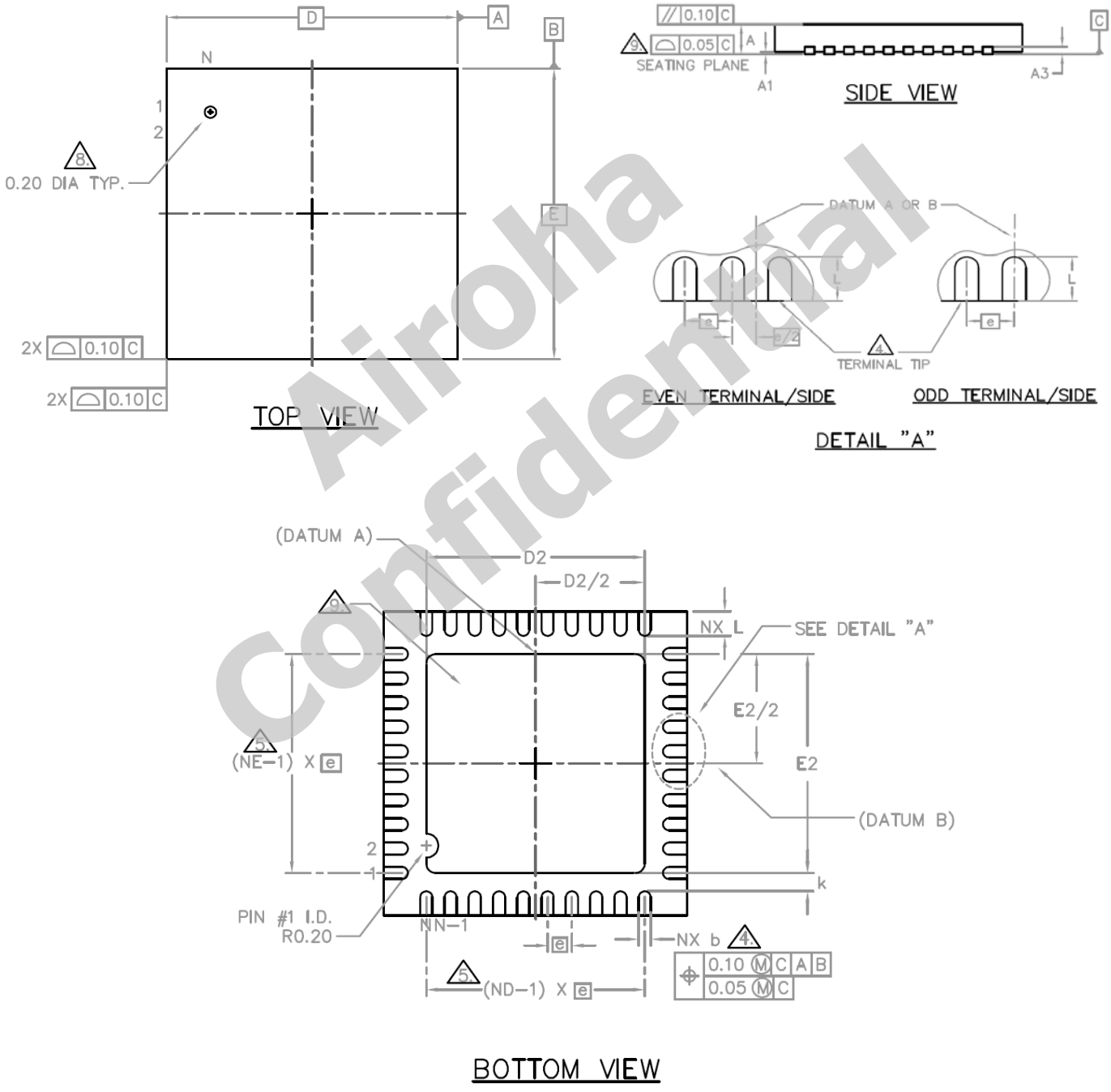
6 Package Dimensions

SAW QFN 40LD, 5x5x0.55mm PKG 0.4 PITCH POD



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SYMBOL	COMMON DIMENSIONS			NOTE
	MIN.	NOM.	MAX.	
A	0.50	0.55	0.60	
A1	0.00	0.02	0.05	
A3		0.15 REF.		
θ	0	—	12	2
K		0.20 MIN.		
D		5.0 BSC		
E		5.0 BSC		

SYMBOL	0.40 mm LEAD PITCH VARIATION			NOTE
	MIN	NOM	MAX	
e		0.40 BSC		
N		40		3
ND		10		5
NE		10		5
L	0.35	0.40	0.45	
b	0.15	0.20	0.25	4
D2	3.50	3.60	3.70	
E2	3.50	3.60	3.70	

NOTES :

1. DIMENSIONING AND TOLERANCING CONFORME TO ASME Y14.5M – 1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS, θ IS IN DEGREES.
3. N IS THE TOTAL NUMBER OF TERMINALS.
4. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30mm FROM TERMINAL TIP. IF THE TERMINAL HAS THE OPTIONAL RADIUS ON THE OTHER END OF THE TERMINAL, THE DIMENSION b SHOULD NOT BE MEASURED IN THAT RADIUS AREA.
5. ND AND NE REFER TO THE NUMBER OF TERMINALS ON EACH D AND E SIDE RESPECTIVELY.
6. MAX. PACKAGE WARPAGE IS 0.05 mm.
7. MAXIMUM ALLOWABLE BURRS IS 0.076 mm IN ALL DIRECTIONS.
8. PIN #1 ID ON TOP WILL BE LASER MARKED.
9. BILATERAL COPLANARITY ZONE APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.
10. THIS DRAWING CONFORMES TO JEDEC REGISTERED OUTLINE MO-220

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