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Preliminary Product Brief
March 1997

LUC4AU01
ATM Layer UNI Manager (ALM)

Introduction

The ALM IC is part of the ATLANTA chip set consisting of four devices that provide a highly integrated, innovative, and complete VLSI solution for implementing the ATM layer core of an ATM switch system. The chip set enables construction of high-performance, feature-rich, and cost-effective ATM switches, scalable over a wide range of switching capacities. This document discusses the ALM device.

Features

- Performs ATM layer User- or Network-Network Interface (UNI or NNI) management functions, supporting up to 662 Mbits/s of ATM traffic (full duplex).
- Controls up to 30 full-duplex ports through MultiPHY (MPHY) devices on the physical layer side.
  - — Manages virtual connection (VC) and virtual path (VP) parameter table in external memory.
  - — Any port can be configured as a UNI or NNI.
  - — Performs VPI/VCI translation for each connection on egress while allowing reusability of same VPI/VCI on different UNIs.
  - — Optionally performs the ATM Forum compliant Dual Leaky-Bucket Policing, with configurable parameters per connection, enabled on a global or per VP basis.
  - — Facilitates call set up and tear down through VC parameter table update via microprocessor port.
  - — Optionally translates or passes the generic flow control (GFC) field of the egress ATM cell header for NNI or UNI applications.
- Supports up to 64K VCs on ingress and up to 64K VCs on egress with scalable external memory.
- Maintains variety of optional per-connection 31-bit statistics counters in external memory:
  - — Ingress CLP0s, ingress CLP1s, nonconforming leaky-bucket A, and nonconforming leaky-bucket B or
  - — Ingress conforming CLP0s, conforming CLP1s, nonconforming CLP0s, and nonconforming CLP1s.
  - — Egress CLP0s, and egress CLP1s.
- Provides UTOPIA Level II interface on the physical layer side, and UTOPIA Level II Plus interface to the ATM layer (or switch core) side.
- Provides two modes of operation:
  - — In user-specific proprietary mode, prepends user-programmable local routing header (up to 12 bytes) to ATM cells on ingress.
  - — In ATLANTA-compatible mode, prepends a preformatted header (required by the ATLANTA chipset) to ATM cells on ingress.
- Supports multicasting to 30 different MPHY ports on egress by providing independent VPI/VCI translation.
- Provides a generic, *Intel** or *Motorola*† compatible, 16-bit microprocessor interface with interrupt.
- Optionally captures ABR RM, F4, and F5 OA&M cells on ingress and any VC on egress to microprocessor port interface.
- Supports read and write modes for cell extraction and insertion via the microprocessor interface.
- Supports 32-bit wide external memory interface using synchronous SRAMs (with 20 ns cycle time).
- Includes system diagnostic features:
  - — Parity on the UTOPIA II interface, UTOPIA II Plus interface, and external memory interface.
  - — Egress to ingress loopback.
  - — Cell insertion via microprocessor port capabilities.
- Facilitates circuit board testing with on-chip *IEEE*‡ standard boundary scan
- Fabricated as a low-power, monolithic IC in 0.5 µm, 3.3 V CMOS technology, with 5 V-tolerant and TTL-level compatible I/O.
- Available in a thermally enhanced 240-pin SQFP package.

* *Intel* is a registered trademark of Intel Corporation.
† *Motorola* is a registered trademark of Motorola, Inc.
‡ *IEEE* is a registered trademark of The Institute of Electrical and Electronics Engineers, Inc.

Description

Figure 1 shows the architecture of an ATM switch designed with the ATLANTA chip set. The LUC4AU01 ATM UNI Layer Manager (ALM) chip performs the ATM layer network interface (UNI or NNI) management functions for an MPHY line card and can be programmed to work with proprietary ATM switch fabric cores.

The ALM operates in a full-duplex manner, with a maximum ATM cell traffic rate of 662 Mbits/s in each direction. The ingress side processes cells arriving from the UNI; the egress side processes cells being sent to the UNI.

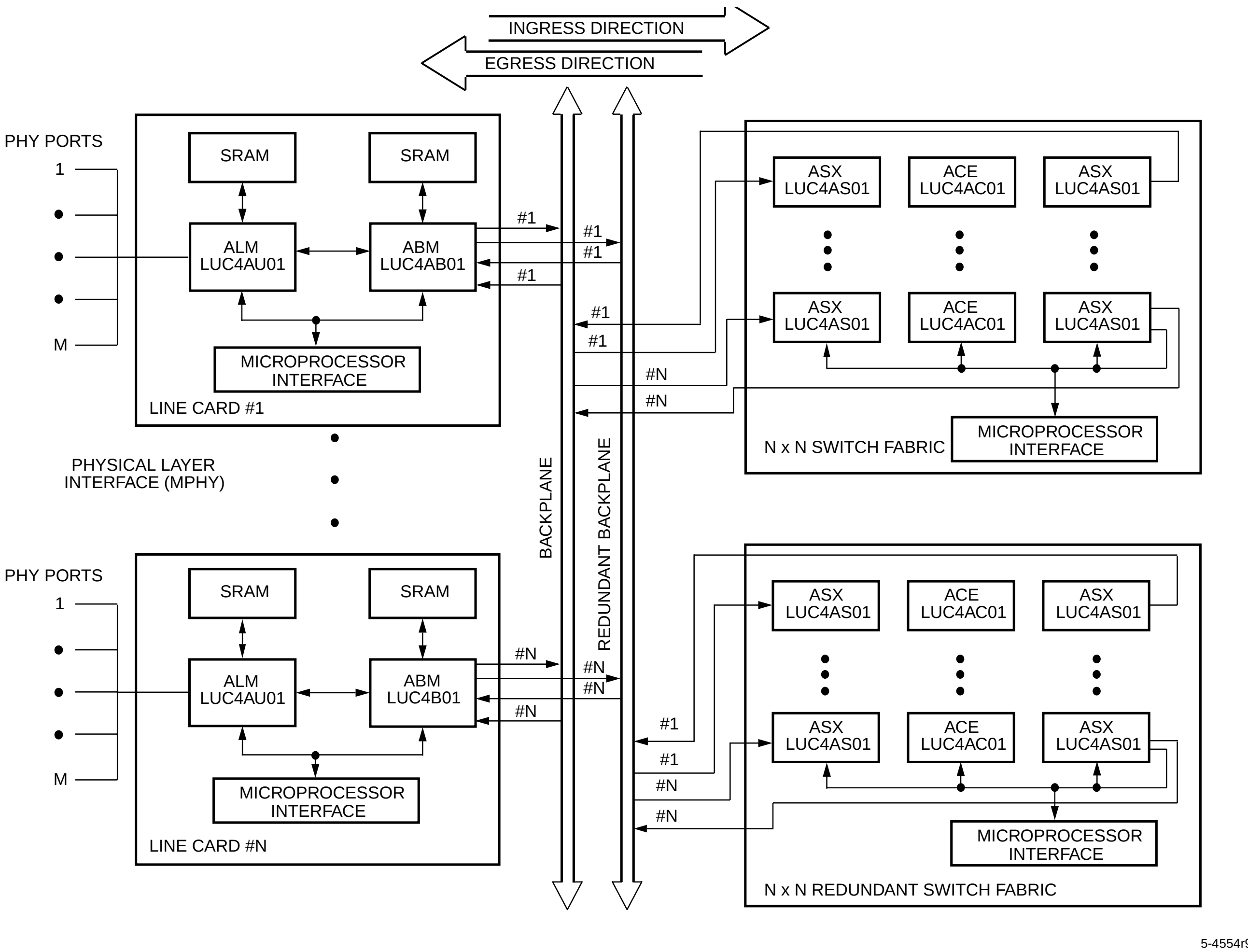

Figure 1. Architecture of an ATM Switch Using the ATLANTA Chip Set

Description (continued)

The block diagram of the chip and a brief description of the functionality of each block follows.

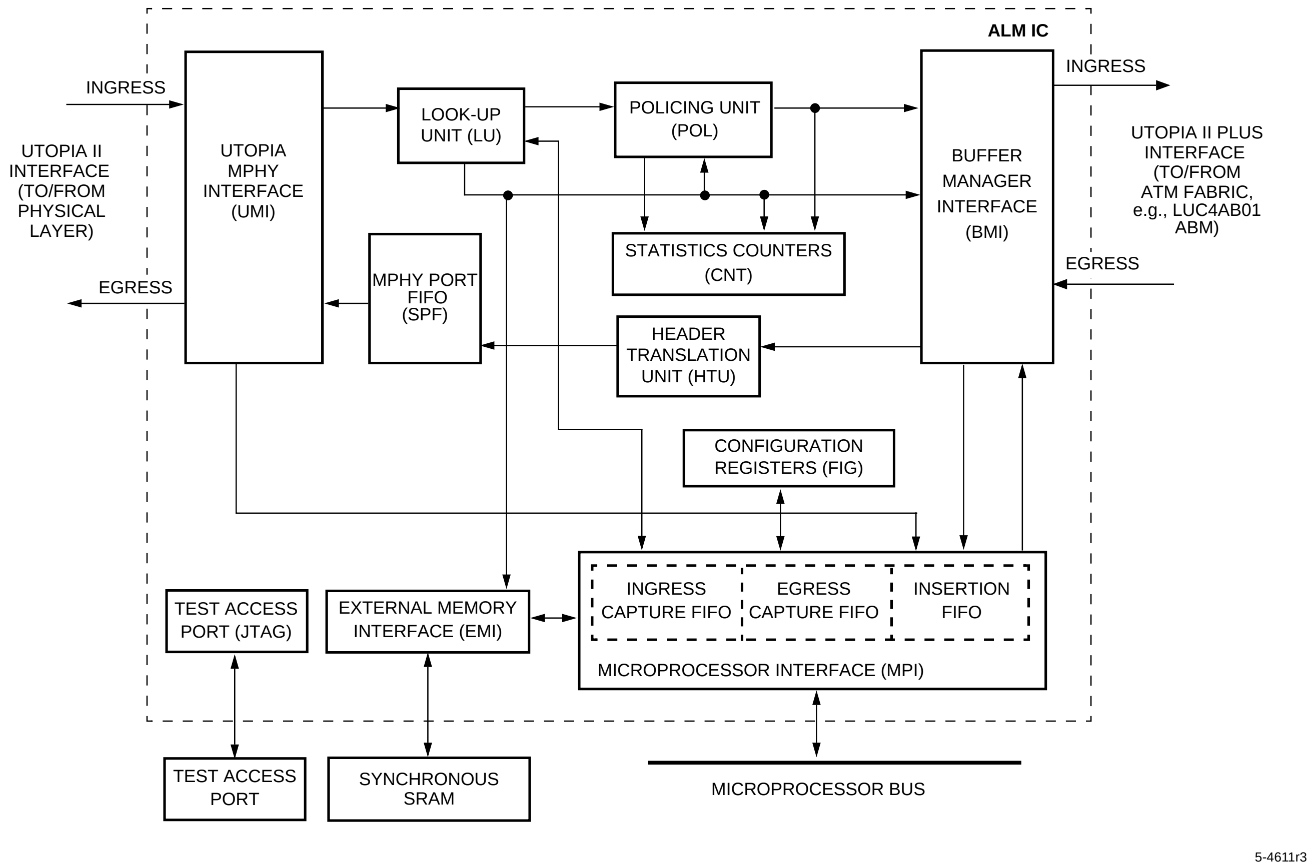

Figure 2. ALM Block Diagram

Description (continued)

UTOPIA MPHY Interface (UMI)

The UMI controls the transfer of ATM cells between the ALM and multiple physical layer devices (MPHYs) connected to ALM via the UTOPIA Level II MPHY interface.

The chip transmits and receives ATM cells via a pair of 16-bit wide buses, using cell-level handshake flow control for up to 30 UNIs or NNIs. The UMI also checks header errors (HEC) on the ingress cells and inserts a locally calculated HEC into the egress cells. Cells received with incorrect HEC are either corrected or dropped depending on the appropriate setting in the configuration register.

Look Up Unit (LU)

Based on the incoming VPI and VCI, the look-up unit performs a two-level look up to fetch connection information (from external memory) for an ingress cell. It supports range check on VPI and VCI. The VPI and VCI values of ingress cells are checked against maximum values for an active connection set up. Cells with invalid VPI or VCI values are dropped or captured depending on the settings in the configuration registers. The look-up unit also recognizes OA&M and ABR RM cells received on ingress by examining the first two bytes of the cell payload.

Policing Unit (POL)

The policing unit checks ingress cells for conformance to their negotiated traffic contracts.

It uses the ATM Forum-compliant dual leaky-bucket algorithm to determine if the cell should be tagged or dropped. Policing can be enabled or disabled on a per-VP basis, as well as globally enabled or disabled. The policing action, tag or drop, can be programmed separately for each individual leaky bucket on a per-connection basis.

Statistics Counters (CNT)

This block maintains per-connection 31-bit statistic counters for the ingress and egress cells. These counters are stored in external memory. They can be written or read through the microprocessor interface. The statistics feature can be globally enabled or disabled. There are six counters available for each connection (four for ingress, two for egress).

Microprocessor Interface (MPI)

The MPI allows an external processor to access the ALM for configuration, maintenance, and internal and external memory reads and writes (e.g., for call set or tear down). It provides a 16-bit asynchronous interface to *Intel*, *Motorola*, or generic microprocessors. It also generates an interrupt when status bits are set.

Configuration Registers (FIG)

The configuration registers store all user-programmable values. They allow the external microprocessor to control the following, for example: to enable/disable global statistics gathering, policing, HEC correction, and generation of time slot synchronization signal. It also allows configuration of base addresses for tables in external memory for policing parameters, translation, VC parameters, and counters. It is also used to determine the size of prepended local routing headers.

External Memory Interface (EMI)

The external memory interface is responsible for accessing external memory (composed of synchronous SRAMs). It is used for scheduling accesses and sends control signals for ALM internal functions or microprocessor-requested operations (e.g., call setup or tear down, collect statistics). The ALM supports a 32-bit wide interface to synchronous SRAMs (20 ns cycle time, nonpipelined, registered input), with a maximum depth of 512 Kwords.

Buffer Module Interface (BMI)

The BMI manages the UTOPIA II Plus ingress and egress data buses and control signals to allow for communication between the ALM and an external buffer manager/module (e.g., the LUC4AB01 ATM Buffer Manager, ABM, device) on the ATM layer (switch) side of ALM. The BMI optionally captures and routes management cells to a microprocessor accessible FIFO. The BMI inserts cell identification bits (OA&M flows, forward and backward ABR RM, and policing outcome as conforming/nonconforming in the local routing header.

Description (continued)

Header Translation Unit (HTU)

The HTU performs ATM header translation on egress cells. It supports up to 64K egress VCs and can optionally translate (for NNI) or pass (for UNI) the GFC field of the ATM header.

MPHY Port FIFOs (SPF)

This block consists of FIFOs that temporarily store outgoing egress cells before their delivery to the destination MPHY ports on UTOPIA II or the microprocessor-accessible egress capture FIFO.

Test Access Port (JTAG)

The ALM incorporates logic to support a standard five-pin test access port (TAP), compatible with the *IEEE* P1149.1 standard (JTAG), used for boundary scan. TAP contains instruction registers, data registers, and control logic, and has its own set of instructions. It is controlled externally by a JTAG bus master. The TAP gives the ALM board-level test capability.

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