

AmZ8030 • AmZ8530 (SCC)

Serial Communications Controller

DISTINCTIVE CHARACTERISTICS

- **Two 1M.bps full duplex serial channels**
Each channel has independent oscillator, baud-rate generator, and PLL for clock recovery, dramatically reducing external components.
- **Programmable protocols**
NRZ, NRZI, and FM data encoding supported under program control.
- **Programmable Asynchronous Modes**
5 to 8 bit characters with programmable stop bits, clock, break detect, and error conditions.
- **Programmable Synchronous Modes**
SDLC and HDLC and SDLC loop supported with frame control, zero insertion and deletion, abort, and residue handling. CRC-16 and CCITT generators and checkers.
- **Z8000* compatible**
The Z8030 interfaces directly to the Z8000 CPU bus and to the Z8000 interrupt structure.
- **Compatible with non-multiplexed bus**
The Z8530 interfaces easily to most other CPUs.

GENERAL DESCRIPTION

The SCC Serial Communications Controller is a dual-channel, multi-protocol data communications peripheral designed for use with 8- and 16-bit microprocessors. The SCC functions as a serial-to-parallel, parallel-to-serial converter/controller. The SCC can be software-configured to satisfy a wide variety of serial communications applications. The device contains a variety of new, sophisticated internal functions including on-chip baud rate generators, digital phase-locked loops, and crystal oscillators, which dramatically reduce the need for external logic.

The SCC handles asynchronous formats, Synchronous byte-oriented protocols such as IBM Bisync, and Synchronous bit-oriented protocols such as HDLC and IBM SDLC. This versatile device supports virtually any serial data transfer application (cassette, diskette, tape drivers, etc.).

The device can generate and check CRC codes in any Synchronous mode and can be programmed to check data integrity in various modes. The SCC also has facilities for modem controls in both channels. In applications where these controls are not needed, the modem controls can be used for general-purpose I/O.

The SCC is offered in two versions. The AmZ8030 is directly compatible with the Z8000 and 8086 CPUs. The AmZ8530 is designed for non-multiplexed buses and is easily interfaced to most other CPUs, such as 8080, Z80, 6800, 68000, and †Multibus.

BLOCK DIAGRAM

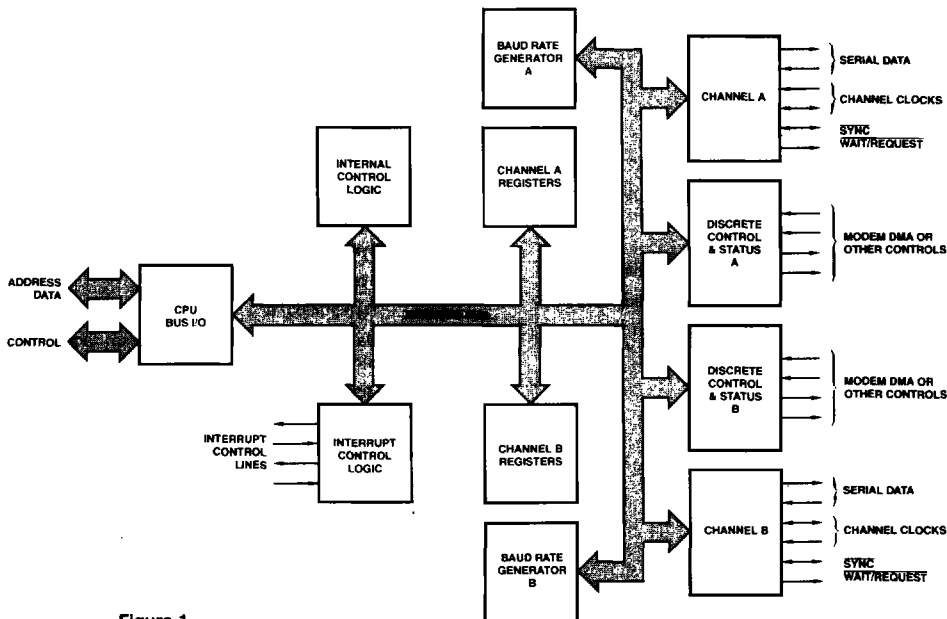


Figure 1.

00970C-1



ARCHITECTURE

The SCC internal structure includes two full-duplex channels, two baud rate generators, internal control and interrupt logic, and a bus interface to the Z8000 CPU (AmZ8030) or to a non-multiplexed CPU bus (AmZ8530). Associated with each channel are a number of read and write registers for mode control and status information, as well as logic necessary to interface to modems or other external devices (Figure 1).

The logic for both channels provides formats, synchronization, and validation for data transferred to and from the channel interface. The modem control inputs are monitored by the control logic under program control. All of the modem control signals are general-purpose in nature and can optionally be used for functions other than modem control.

The register set for each channel includes ten control (write) registers, two synchronous character (write) registers, and four status (read) registers. In addition, each baud rate generator has two (read/write) registers for holding the time constant that determines the baud rate. Finally, associated with the interrupt logic is a write register for the interrupt vector accessible through either channel, a write-only Master Interrupt Control register and three read registers: one containing the vector with status information (Channel B only), one containing the vector without status (A only), and one containing the Interrupt Pending bits (A only).

The registers for each channel are designated as follows:

WR0-WR15 – Write Registers 0 through 15.

RR0-RR3, RR10, RR12, RR13, RR15 – Read Registers 0 through 3, 10, 12, 13, 15.

The following table lists the functions assigned to each read or write register. The SCC contains only one WR2 and WR9, but they can be accessed by either channel. All other registers are paired (one for each channel).

DATA PATH

The transmit and receive data path illustrated in Figure 2 is identical for both channels. The receiver has three 8-bit buffer registers in a FIFO arrangement, in addition to the 8-bit receive shift register. This scheme creates additional time for the CPU to service an interrupt at the beginning of a block of high-speed data. Incoming data is routed through one of several paths (data or CRC) depending on the selected mode (the character length in asynchronous modes also determines the data path).

The transmitter has an 8-bit transmit data buffer register loaded from the internal data bus and a 20-bit transmit shift register that can be loaded either from the sync-character registers or from the transmit data register. Depending on the operational mode, outgoing data is routed through one of four main paths before it is transmitted from the Transmit Data output (TxD).

TABLE 1. READ AND WRITE REGISTER FUNCTIONS

READ REGISTER FUNCTIONS

RR0	Transmit/Receive buffer status and External status
RR1	Special Receive Condition status
RR2	Modified interrupt vector (Channel B only)
	Unmodified interrupt vector (Channel A only)
RR3	Interrupt Pending bits (Channel A only)
RR8	Receive buffer
RR10	Miscellaneous status
RR12	Lower byte of baud rate generator time constant
RR13	Upper byte of baud rate generator time constant
RR15	External/Status interrupt information

WRITE REGISTER FUNCTIONS

WR0	CRC initialize, initialization commands for the various modes, shift right/shift left command
WR1	Transmit/Receive interrupt and data transfer mode definition
WR2	Interrupt vector (accessed through either channel)
WR3	Receive parameters and control
WR4	Transmit/Receive miscellaneous parameters and modes
WR5	Transmit parameters and controls
WR6	Sync characters or SDLC address field
WR7	Sync character or SDLC flag
WR8	Transmit buffer
WR9	Master interrupt control and reset (accessed through either channel)
WR10	Miscellaneous transmitter/receiver control bits
WR11	Clock mode control
WR12	Lower byte of baud rate generator time constant
WR13	Upper byte of baud rate generator time constant
WR14	Miscellaneous control bits
WR15	External/Status interrupt control

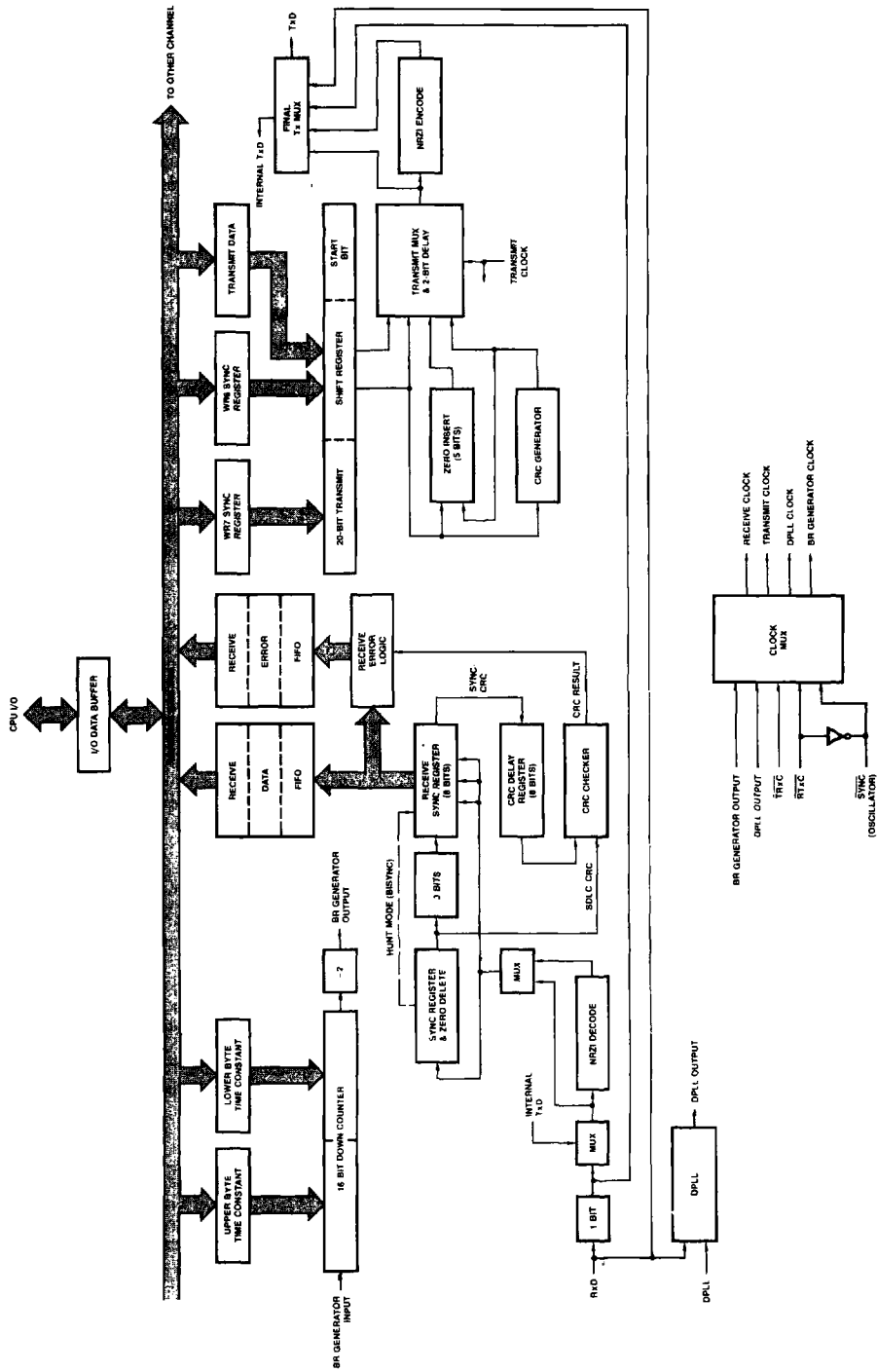


Figure 2. Data Path



FUNCTIONAL DESCRIPTION

The functional capabilities of the SCC can be described from two different points of view: as a data communications device, it transmits and receives data in a wide variety of data communications protocols; as a microprocessor peripheral, it interacts with the CPU and provides vectored interrupts and handshaking signals.

DATA COMMUNICATIONS CAPABILITIES

The SCC provides two independent full-duplex channels programmable for use in any common asynchronous or synchronous data-communication protocol. Figure 3 and the following description briefly detail these protocols.

Asynchronous Modes

Transmission and reception can be accomplished independently on each channel with five to eight bits per character, plus optional even or odd parity. The transmitters can supply one, one-and-a-half or two stop bits per character and can provide a break output at any time. The receiver break-detection logic interrupts the CPU both at the start and at the end of a received break. Reception is protected from spikes by a transient spike-rejection mechanism that checks the signal one-half a bit time after a Low level is detected on the receive data input (RxDA or RxDB in Figure 18). If the Low does not persist (as in the case of a transient), the character assembly process does not start.

Framing errors and overrun errors are detected and buffered together with the partial character on which they occur. Vec-

tored interrupts allow fast servicing or error conditions using dedicated routines. Furthermore, a built-in checking process avoids the interpretation of framing error as a new start bit: a framing error results in the addition of one-half a bit time to the point at which the search for the next start bit begins.

The SCC does not require symmetric transmit and receive clock signals – a feature allowing use of the wide variety of clock sources. The transmitter and receiver can handle data at a rate of 1, 1/16, 1/32, or 1/64 of the clock rate supplied to the receive and transmit clock inputs. In asynchronous modes, the SYNC pin may be programmed as an input used for functions such as monitoring a ring indicator.

Synchronous Modes

The SCC supports both byte-oriented and bit-oriented synchronous communication. Synchronous byte-oriented protocols can be handled in several modes allowing character synchronization with a 6-bit or 8-bit synchronous character (Monosync), any 12-bit synchronous pattern (Bisync), or with an external synchronous signal. Leading synchronous characters can be removed without interrupting the CPU.

Five- or 7-bit synchronous characters are detected with 8- or 16-bit patterns in the SCC by overlapping the larger pattern across multiple incoming synchronous characters as shown in Figure 4.

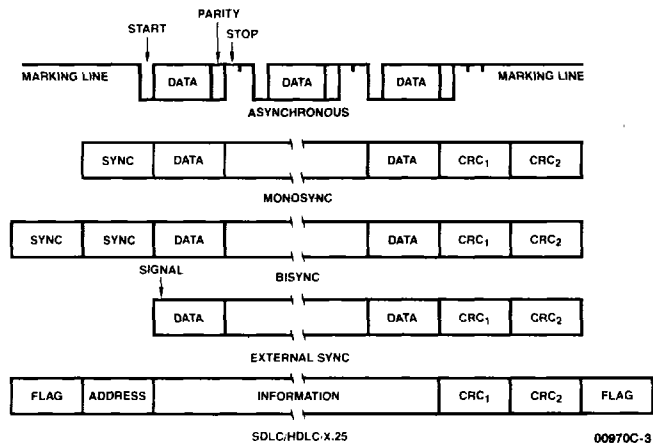


Figure 3. SCC Protocols

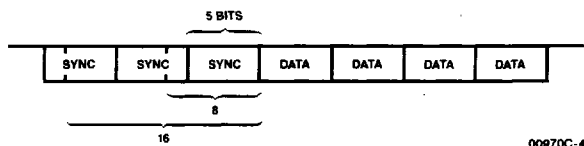


Figure 4. Detecting 5- or 7-Bit Synchronous Characters

CRC checking for Synchronous byte-oriented modes is delayed by one character time so that the CPU may disable CRC checking on specific characters. This permits the implementation of protocols such as IBM Bisync.

Both CRC-16 ($X^{16} + X^{15} + X^2 + 1$) and CCITT ($X^{16} + X^{12} + X^5 + 1$) error checking polynomials are supported. Either polynomial may be selected in all synchronous modes. Users may preset the CRC generator and checker to all 1s or all 0s. The SCC also provides a feature that automatically transmits CRC data when no other data is available for transmission. This allows for high-speed transmissions under DMA control, with no need for CPU intervention at the end of a message. When there is no data or CRC to send in synchronous modes, the transmitter inserts 6-, 8-, or 16-bit synchronous characters, regardless of the programmed character length.

The SCC supports synchronous bit-oriented protocols, such as SDLC and HDLC, by performing automatic flag sending, zero insertion, and CRC generation. A special command can be used to abort a frame in transmission. At the end of a message, the SCC automatically transmits the CRC and trailing flag when the transmitter underruns. The transmitter may also be programmed to send an idle line consisting of continuous flag characters or a steady marking condition.

If a transmit underrun occurs in the middle of a message, an external/status interrupt warns the CPU of this status change so that an abort may be issued. The SCC may also be programmed to send an abort itself in case of an underrun, relieving the CPU of this task. One to eight bits per character can be sent allowing reception of a message with no prior information about the character structure in the information field of a frame.

The receiver automatically acquires synchronization on the leading flag of a frame in SDLC or HDLC and provides a synchronization signal on the SYNC pin (an interrupt can also be programmed). The receiver can be programmed to search for frames addressed by a single byte (or four bits within a byte) of a user-selected address or to a global broadcast address. In this mode, frames not matching either the user-selected or broadcast address are ignored. The number of address bytes can be extended under software control. For receiving data, an interrupt on the first received character, or an interrupt on every character, or on special condition only (end-of-frame) can be selected. The receiver automatically deletes all 0s inserted by the transmitter during character assembly. CRC is also calculated and is automatically checked to validate frame transmission. At the end of transmission, the status of a received frame is available in the status registers. In SDLC mode, the SCC must be programmed to use the SDLC CRC polynomial, but the generator and checker may be preset to all 1s or all 0s. The CRC is inverted before transmission and the receiver checks against the bit pattern 0001110100001111.

NRZ, NRZI or FM coding may be used in any 1X mode. The parity options available in asynchronous modes are available in synchronous modes.

The SCC can be conveniently used under DMA control to provide high-speed reception or transmission. In reception, for example, the SCC can interrupt the CPU when the first character of a message is received. The CPU then enables the DMA to transfer the message to memory. The SCC then issues an end-of-frame interrupt and the CPU can check the status of the received message. Thus, the CPU is freed for other service while the message is being received. The CPU may also enable the DMA first and have the SCC interrupt only on end-of-frame. This procedure allows all data to be transferred via the DMA.

SDLC LOOP MODE

The SCC supports SDLC Loop mode in addition to normal SDLC. In an SDLC Loop, there is a primary controller station that manages the message traffic flow and any number of secondary stations. In SDLC Loop mode, the SCC performs the functions of a secondary station while an SCC operating in regular SDLC mode can act as a controller (Figure 5).

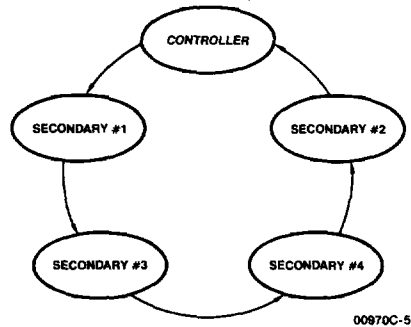


Figure 5. An SDLC Loop

A secondary station in an SDLC Loop is always listening to the messages being sent around the loop, and in fact must pass these messages to the rest of the loop by retransmitting them with a one-bit-time delay. The secondary station can place its own message on the loop only at specific times. The controller signals that secondary stations may transmit messages by sending a special character, called an EOP (End of Poll), around the loop. The EOP character is the bit pattern 11111110. Because of zero insertion during messages, this bit pattern is unique and easily recognized.

When a secondary station has a message to transmit and recognizes an EOP on the line, it changes the last binary one of the EOP to a zero before transmission. This has the effect of turning the EOP into a flag sequence. The secondary station now places its message on the loop and terminates the message with an EOP. Any secondary stations further down the loop with messages to transmit can then append their messages to the message of the first secondary station by the same process. Any secondary stations without messages to send merely echo the incoming messages and are prohibited from placing messages on the loop (except upon recognizing an EOP).

SDLC Loop mode is a programmable option in the SCC. NRZ, NRZI, and FM coding may all be used in SDLC Loop mode.

BAUD RATE GENERATOR

Each channel in the SCC contains a programmable Baud-rate generator. Each generator consists of two 8-bit time constant registers that form a 16-bit time constant, a 16-bit down counter, and a flip-flop on the output producing a square wave. On startup, the flip-flop on the output is set in a High state, the value in the time constant register is loaded into the counter, and the counter starts counting down. The output of the baud rate generator toggles upon reaching zero, the value in the

time constant register is loaded into the counter, and the process is repeated. The time constant may be changed at any time, but the new value does not take effect until the next load of the counter.

The output of the baud rate generator may be used as either the transmit clock, the receive clock, or both. It can also drive the digital phase-locked loop (see next section).

If the receive clock or transmit clock is not programmed to come from the $\overline{\text{TRxC}}$ pin, the output of the baud rate generator may be echoed out via the $\overline{\text{TRxC}}$ pin.

The following formula relates the time constant to the baud rate. (The baud rate is in bits/second and the BR clock period is in seconds.)

$$\text{baud rate} = \frac{1}{2 (\text{time constant} + 2) \times (\text{BR clock period})}$$

Time-Constant Values for Standard Baud Rates at BR Clock = 3.9936MHz		
Rate (Baud)	Time Constant (decimal notation)	Error
19200	102	—
9600	206	—
7200	275	0.12%
4800	414	—
3600	553	0.06%
2400	830	—
2000	996	0.04%
1800	1107	0.03%
1200	1662	—
600	3326	—
300	6654	—
150	13310	—
134.5	14844	0.0007%
110	18151	0.0015%
75	26622	—
50	39934	—

DIGITAL PHASE-LOCKED LOOP

The SCC contains a digital phase-locked-loop (DPLL) to recover clock information from a data stream with NRZI or FM encoding. The DPLL is driven by a clock that is nominally 32 (NRZI) or 16 (FM) times the data rate. The DPLL uses this clock, along with the data stream, to construct a clock for the data. This clock may then be used as the SCC receive clock, the transmit clock, or both.

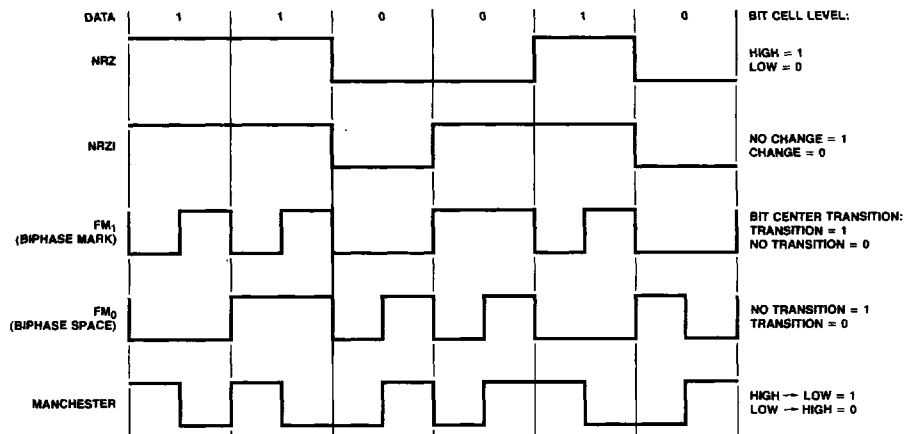
For NRZI encoding, the DPLL counts the 32X clock to create nominal bit times. As the 32X clock is counted, the DPLL is searching the incoming data stream for edges (either 1/0 or 0/1). Whenever an edge is detected, the DPLL makes a count adjustment (during the next counting cycle), producing a terminal count closer to the center of the bit cell.

For FM encoding, the DPLL still counts from 0 to 31, but with a cycle corresponding to two bit times. When the DPLL is locked, the clock edges in the data stream should occur between counts 15 and 16 and between counts 31 and 0. The DPLL looks for edges only during a time centered on the 15/16 counting transition.

The 32X clock for the DPLL can be programmed to come from either the $\overline{\text{TRxC}}$ input or the output of the baud rate generator. The DPLL output may be programmed to be echoed out of the SCC via the $\overline{\text{TRxC}}$ pin (if this pin is not being used as an input).

DATA ENCODING

The SCC may be programmed to encode and decode the serial data in four different ways (Figure 6). In NRZ encoding, a 1 is represented by a High level and a 0 is represented by a Low level. In NRZI encoding, as 1 is represented by no change in level and a 0 is represented by a change in level. In FM₁ (more properly, bi-phase mark) a transition occurs at the beginning of every bit cell. A 1 is represented by an additional transition at the center of the bit cell and a 0 is represented by no additional transition at the center of the bit cell. In FM₀ (bi-phase space), a transition occurs at the beginning of every bit cell. A 0 is represented by an additional transition at the center of the bit cell,



00970C-6

Figure 6. Data Encoding Methods

and a 1 is represented by no additional transition at the center of the bit cell. In addition to these four methods, the SCC can be used to decode Manchester (bi-phase level) data by using the DPLL in the FM mode and programming the receiver for NRZ data. Manchester encoding always produces a transition at the center of the bit cell. If the transition is 0/1 the bit is a 0. If the transition is 1/0 the bit is a 1.

AUTO ECHO AND LOCAL LOOPBACK

The SCC is capable of automatically echoing everything it receives. This feature is useful mainly in asynchronous modes, but works in synchronous and SDLC modes as well. In Auto Echo mode, TxD is RxD. Auto Echo mode can be used with NRZI or FM encoding with no additional delay, because the data stream is not decoded before retransmission. In Auto Echo mode, the CTS input is ignored as a transmitter enable (although transitions on this input can still cause interrupts if programmed to do so). In this mode, the transmitter is actually bypassed and the programmer is responsible for disabling transmitter interrupts and WAIT/REQUEST on transmit.

The SCC is also capable of local loopback. In this mode, TxD is RxD just as in Auto Echo mode. However, in Local Loopback mode, the internal transmit data is tied to the internal receive data and RxD is ignored (except to be echoed out via TxD). The CTS and DCD inputs are also ignored as transmit and receive enables. However, transitions on these inputs can still cause interrupts. Local Loopback works in asynchronous, synchronous and SDLC modes with NRZ, NRZI or FM coding of the data stream.

I/O INTERFACE CAPABILITIES

The SCC offers the choice of Polling, Interrupt (vectored or nonvectored), and Block Transfer modes to transfer data, status, and control information to and from the CPU. The Block Transfer mode can be implemented under CPU or DMA control.

POLLING

All interrupts are disabled. Three status registers in the SCC are automatically updated whenever any function is performed. For example, end-of-frame in SDLC mode sets a bit in one of these status registers. The idea behind polling is for the CPU to periodically read a status register until the register contents indicate the need for data to be transferred. Only one register needs to be read; depending on its contents, the CPU either writes data, reads data, or continues. Two bits in the register indicate the need for data transfer. An alternative is a poll of the Interrupt Pending register to determine the source of an interrupt. The status for both channels resides in one register.

INTERRUPTS

When a SCC responds to an Interrupt Acknowledge signal (INTACK) from the CPU, an interrupt vector may be placed on the data bus. This vector is written in WR2 and may be read in RR2A or RR2B (Figures 8 and 9).

To speed interrupt response time, the SCC can modify three bits in this vector to indicate status. If the vector is read in Channel A, status is never included; if it is read in Channel B, status is always included.

Each of the six sources of interrupts in the SCC (Transmit, Receive and External/Status interrupts in both channels) has three bits associated with the interrupt source: Interrupt Pending (IP), Interrupt Under Service (IUS), and Interrupt Enable (IE). Operation of the IE bit is straightforward. If the IE bit is set for a given interrupt source, then that source can request interrupts. The exception is when the MIE (Master Interrupt Enable) bit in WR9 is reset and no interrupts may be requested. The IE bits are write-only.

The other two bits are related to the Z-Bus interrupt priority chain (Figure 7). As a Z-Bus peripheral, the SCC may request an interrupt only when no higher-priority device is requesting one, e.g., when IEI is High. If the device in question requests an interrupt, it pulls down INT. The CPU then responds with INTACK, and the interrupting device places the vector on the A/D bus.

In the SCC, the IP bit signals a need for interrupt servicing. When an IP bit is 1 and the IEI input is High, the INT output is pulled Low, requesting an interrupt. In the SCC, if the IE bit is not set by enabling interrupts, then the IP for that source can never be set. The IP bits are readable in RR3A.

The IUS bits signal that an interrupt request is being serviced. If an IUS is set, all interrupt sources of lower priority in the SCC and external to the SCC are prevented from requesting interrupts. The internal interrupt sources are inhibited by the state of the internal daisy chain, while lower priority devices are inhibited by the IEO output of the SCC being pulled Low and propagated to subsequent peripherals. An IUS bit is set during an Interrupt Acknowledge cycle if there are no higher priority devices requesting interrupts.

There are three types of interrupts: Transmit, Receive and External/Status interrupts. Each interrupt type is enabled under program control with Channel A having higher priority than Channel B, and with Receiver, Transmit and External/Status interrupts prioritized in that order within each channel. When the Transmit interrupt is enabled, the CPU is interrupted when the transmit buffer becomes empty. (This implies that the transmitter must have had a data character written into it so

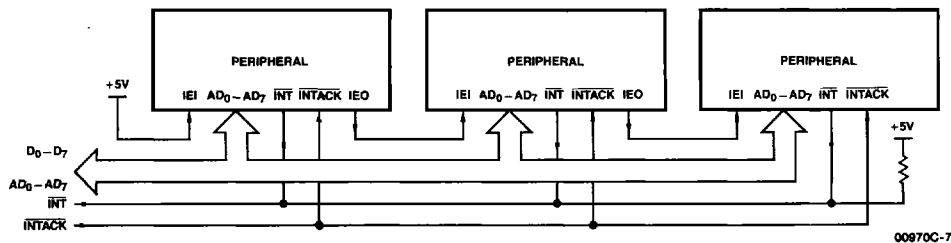


Figure 7. Z-Bus Interrupt Schedule

AmZ8030/AmZ8530

that it can become empty.) When enabled, the receiver can interrupt the CPU in one of three ways:

- Interrupt on First Receive Character or Special Receive condition.
- Interrupt on all Receive Characters or Special Receive condition.
- Interrupt on Special Receive condition only.

Interrupt on First Character or Special Condition and Interrupt on Special Condition Only are typically used with the Block Transfer mode. A Special Receive Condition is one of the following: receiver overrun, framing error in Asynchronous mode, End-of-Frame in SDLC mode and, optionally, a parity error. The Special Receive Condition interrupt is different from an ordinary receive character available interrupt only in the status placed in the vector during the Interrupt-Acknowledge cycle. In Interrupt on First Receive Character, an interrupt can occur from Special Receive conditions any time after the first receive character interrupt.

The main function of the External/Status interrupt is to monitor the signal transitions of the CTS, DCD, and SYNC pins; however, an External/Status interrupt is also caused by a Transmit Underrun condition, or a zero count in the baud rate generator, or by the detection of a Break (asynchronous mode), Abort (SDLC mode) or EOP (SDLC Loop mode) sequence in the

data stream. The interrupt caused by the Abort or EOP has a special feature allowing the SCC to interrupt when the Abort or EOP sequence is detected or terminated. This feature facilitates the proper termination of the current message, correct initialization of the next message, and the accurate timing of the Abort condition in external logic in SDLC mode. In SDLC Loop mode this feature allows secondary stations to recognize the wishes of the primary station to regain control of the loop during a poll sequence.

CPU/DMA BLOCK TRANSFER

The SCC provides a Block Transfer mode to accommodate CPU block transfer functions and DMA controllers. The Block Transfer mode uses the WAIT/REQUEST output in conjunction with the Wait/Request bits in WR1. The WAIT/REQUEST output can be defined under software control as a WAIT line in the CPU Block Transfer mode or as a REQUEST line in the DMA Block Transfer mode.

To a DMA controller, the SCC REQUEST output indicates that the SCC is ready to transfer data to or from memory. To the CPU, the WAIT line indicates that the SCC is not ready to transfer data, thereby requesting that the CPU extend the I/O cycle. The DTR/REQUEST line allows full-duplex operation under DMA control.

PROGRAMMING

Each channel has fifteen Write registers that are individually programmed from the system bus to configure the functional personality of each channel. Each channel also has eight Read registers from which the system can read Status, Baud rate, or Interrupt information.

The AmZ8030 and AmZ8530 differ in the way the system accesses these registers:

In the AmZ8030 all registers are directly addressable from the multiplexed Address Data bus. See Figure 10 and Figure 11 for timing. The AmZ8030 can operate in either of two modes: when bit 0 in Write Register 0 is reset (or after initialization with a hardware reset) Address lines AD₁ through AD₅ select the register to be read from or written into during Data Stroke \overline{DS} . (This is called left shift and is the natural AmZ8000 mode). When bit 0 in Write Register 0 is set, Address lines AD₀ through AD₄ select the register to be read from or written into. (This is called right shift and is more natural for interfacing with other microprocessors.)

Table 2 describes the register addressing for both modes.

Channel A/Channel B selection is made either by AD₀ or by AD₅.

If Bit D₀ in WR0 is reset (or after hardware reset):

AD₅ selects the channel (0 = B, 1 = A)
(this is called "Select Shift Left Mode")

If Bits D₀ and D₁ in WR0 are set, AD₀ selects the channel (0 = B, 1 = A) (this is called "Select Shift Right Mode")

In the AmZ8530 only the four data registers (Read, Write for channels A and B) are directly selected by a High on the D/C input and the appropriate levels on the RD, WR and A/B pins. All other registers are addressed indirectly by the content of Write Register 0 in conjunction with a Low on the D/C input and the appropriate levels on the RD, WR and A/B pins. If bit 4 in WW0 is 1 and bits 5 and 6 are 0 then bits 0, 1, 2 address the higher registers 8 through 15. If bits 4, 5, 6 contain a different code, bits 0, 1, 2 address the lower registers 0 through 7 as shown on Table 3.

TABLE 2. REGISTER ADDRESSING (AmZ8030 ONLY)

AD ₄	AD ₃	AD ₂	AD ₁	Write Register	Read Register
0	0	0	0	0	0
0	0	0	1	1	1
0	0	1	0	2	2
0	0	1	1	3	3
0	1	0	0	4	(0)
0	1	0	1	5	(1)
0	1	1	0	6	(2)
0	1	1	1	7	(3)
1	0	0	0	Data	Data
1	0	0	1	9	-
1	0	1	0	10	10
1	0	1	1	11	(15)
1	1	0	0	12	12
1	1	0	1	13	13
1	1	1	0	14	(10)
1	1	1	1	15	15

Writing to or reading from any register except RR0, WR0 and the Data Registers thus involves two operations:

First write the appropriate code into WR0, then follow this by a write or read operation on the register thus specified. Bits 0 through 4 in WW0 are automatically cleared after this operation, so that WW0 then points to WR0 or RR0 again.

Channel A/Channel B selection is made by the A/B input (High = A, Low = B)

In both AmZ8030 and AmZ8530 the system program first issues a series of commands to initialize the basic mode of operation. This is followed by other commands to qualify conditions within the selected mode. For example, the asynchronous mode, character length, clock rate, number of stop bits, even or odd parity might be set first. Then the interrupt mode would be set, and finally, receiver or transmitter enable.

TABLE 3. REGISTER ADDRESSING (AmZ8530 ONLY)

D/C "Point High" Code in WR0:		D ₂ In WR0:	D ₁	D ₀	Write Register	Read Register
High	Either way	X	X	X	Data	Data
Low	Not true	0	0	0	0	0
Low	Not true	0	0	1	1	1
Low	Not true	0	1	0	2	2
Low	Not true	0	1	1	3	3
Low	Not true	1	0	0	4	(0)
Low	Not true	1	0	1	5	(1)
Low	Not true	1	1	0	6	(2)
Low	Not true	1	1	1	7	(3)
Low	True	0	0	0	Data	Data
Low	True	0	0	1	9	-
Low	True	0	1	0	10	10
Low	True	0	1	1	11	(15)
Low	True	1	0	0	12	12
Low	True	1	0	1	13	13
Low	True	1	1	0	14	(10)
Low	True	1	1	1	15	15

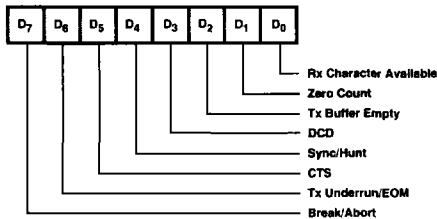
READ REGISTERS

The SCC contains eight read registers (actually nine, counting the receive buffer (RR8) in each channel). Four of these may be read to obtain status information (RR0, RR1, RR10, and RR15). Two registers (RR12 and RR13) may be read to learn the baud rate generator time constant. RR2 contains either the unmodified interrupt vector (Channel A) or the vector

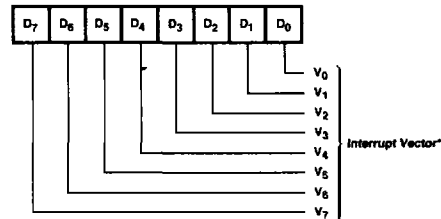
modified by status information (Channel B). RR3 contains the Interrupt Pending (IP) bits (Channel A). Figure 8 shows the formats for each read register.

The status bits of RR0 and RR1 are carefully grouped to simplify status monitoring; e.g., when the interrupt vector indicates a Special Receive Condition interrupt, all the appropriate error bits can be read from a single register (RR1).

Read Register 0

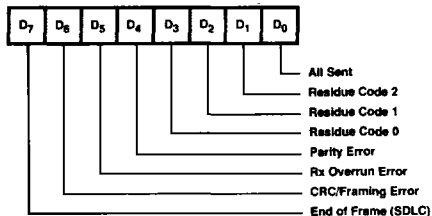


Read Register 2

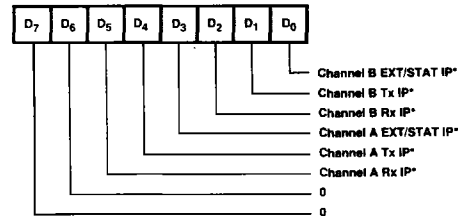


*Modified in B Channel

Read Register 1



Read Register 3

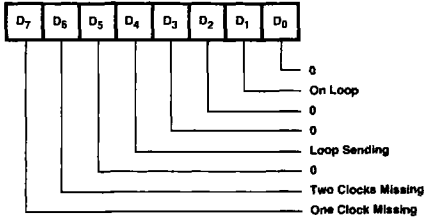


*Always 0 in B Channel

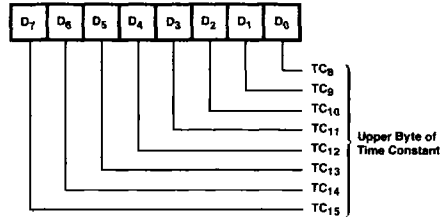
Figure 8. Read Register Bit Functions



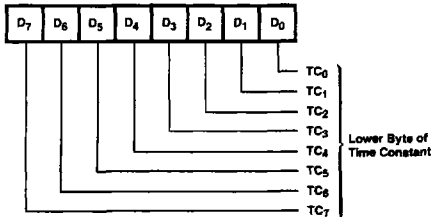
Read Register 10



Read Register 13



Read Register 12



Read Register 15

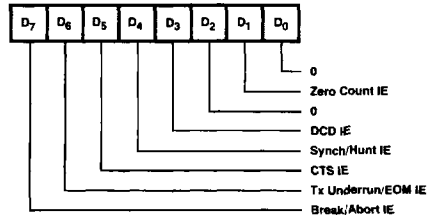


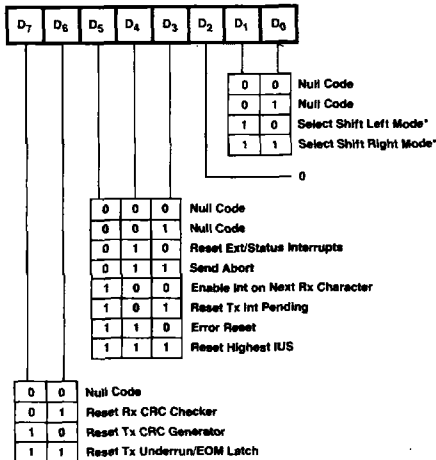
Figure 8. Read Register Bit Functions (Cont.)

WRITE REGISTERS

The SCC contains 15 write registers (16 counting WR8, the transmit buffer) in each channel. These write registers are programmed separately to configure the functional "personality" of the channels. In addition, there are two registers (WR2 and WR9)

shared by the two channels that may be accessed through either of them. WR2 contains the interrupt vector for both channels, while WR9 contains the interrupt control bits. Figure 9 shows the format of each write register.

Write Register 0 (AmZ8030)



*Channel B only

Write Register 0 (AmZ8530)

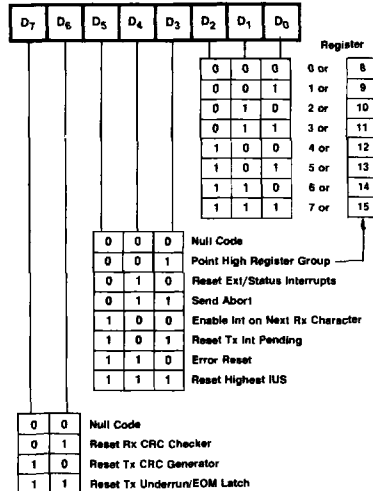
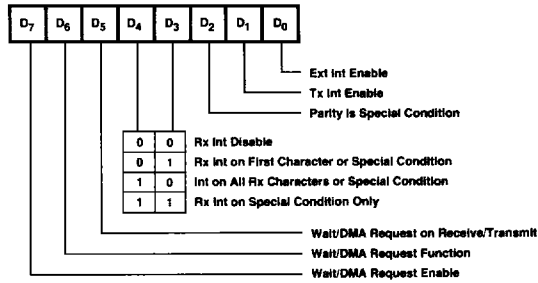
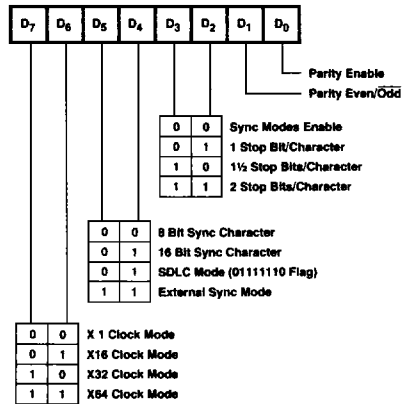


Figure 9. Write Register Bit Functions

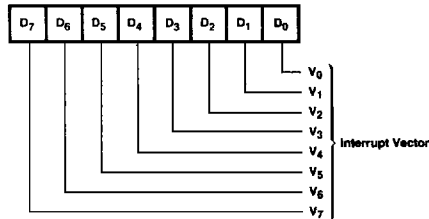
Write Register 1



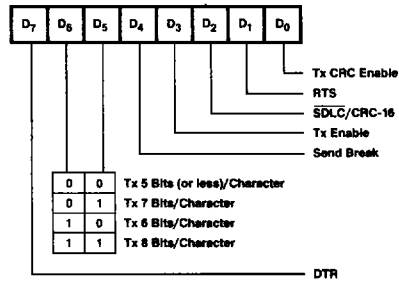
Write Register 4



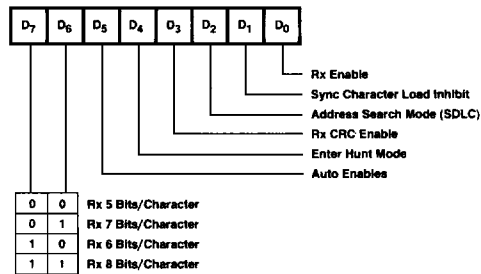
Write Register 2



Write Register 5



Write Register 3



Write Register 6

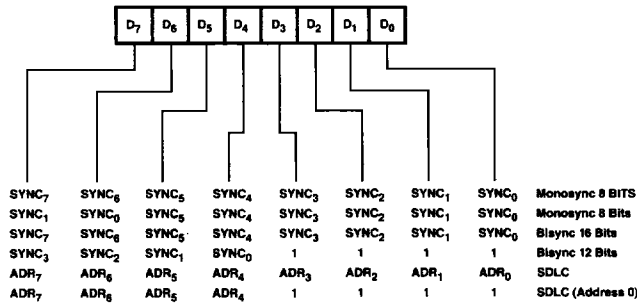
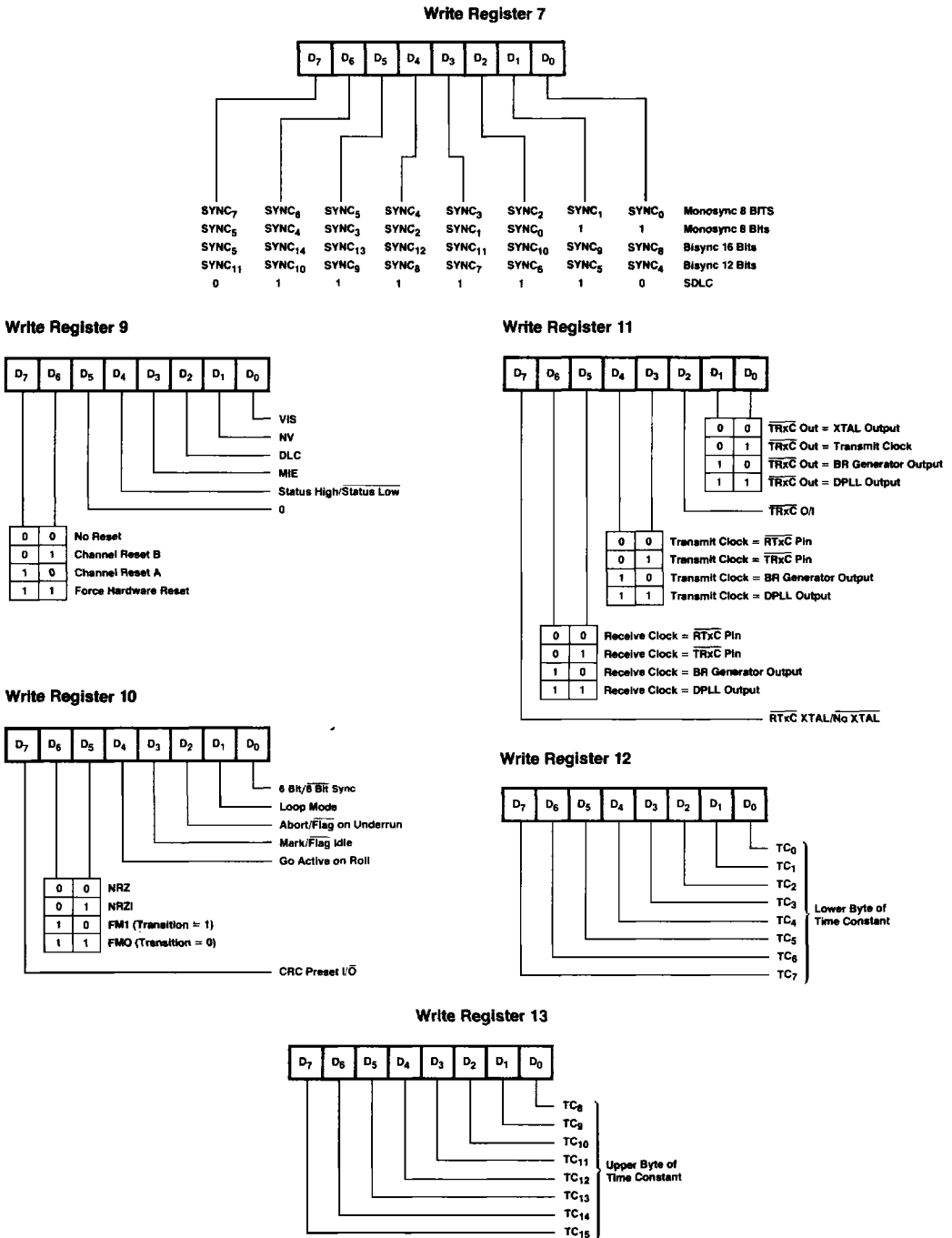


Figure 9. Write Register Bit Functions (Cont.)





Write Register 10

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
----------------	----------------	----------------	----------------	----------------	----------------	----------------	----------------

6 Bit/6 Bit Sync

Loop Mode

Abort/Flag on Underrun

Mark/Flag Idle

Go Active on Roll

0	0	NRZ
0	1	NRZI
1	0	FM1 (Transition = 1)
1	1	FMO (Transition = 0)

CRC Preset I/O

Write Register 12

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
----------------	----------------	----------------	----------------	----------------	----------------	----------------	----------------

TC₀

TC₁

TC₂

TC₃

TC₄

TC₅

TC₆

TC₇

Lower Byte of Time Constant

Write Register 13

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
----------------	----------------	----------------	----------------	----------------	----------------	----------------	----------------

TC₈

TC₉

TC₁₀

TC₁₁

TC₁₂

TC₁₃

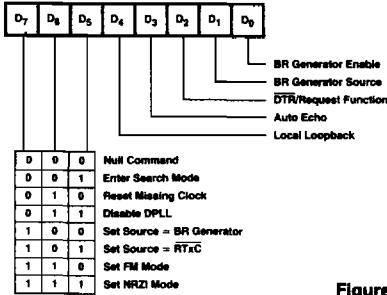
TC₁₄

TC₁₅

Upper Byte of Time Constant

Figure 9. Write Register Bit Functions (Cont.)

Write Register 14



Write Register 15

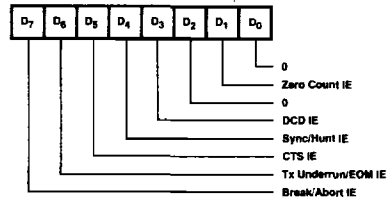


Figure 9. Write Register Bit Functions (Cont.)

AmZ8030 TIMING

The SCC generates internal control signals from \overline{AS} and \overline{DS} that are related to PCLK. Since PCLK has no phase relationship with \overline{AS} and \overline{DS} , the circuitry generating these internal control signals must provide time for metastable conditions to disappear. This gives rise to a recovery time related to PCLK. The recovery time applies only between bus transactions involving the SCC to the falling edge of \overline{DS} in the second transaction involving the SCC. This time must be at least 6 PCLK cycles plus 200 ns.

READ CYCLE TIMING

Figure 10 illustrates read cycle timing. The address on $AD_0 - AD_7$ and the state of \overline{CS}_0 and \overline{INTACK} are latched by the rising edge of \overline{AS} . R/\overline{W} must be High to indicate a read cycle. CS_1 must also be High for the read cycle to occur. The data bus drivers in the SCC are then enabled while \overline{DS} is Low.

WRITE CYCLE TIMING

Figure 11 illustrates write cycle timing. The address on $AD_0 - AD_7$ and the state of \overline{CS}_0 and \overline{INTACK} are latched by the rising

edge of \overline{AS} . R/\overline{W} must be Low to indicate a write cycle. CS_1 must be High for the write cycle to occur. \overline{DS} Low strobes the data into the SCC.

INTERRUPT ACKNOWLEDGE CYCLE TIMING

Figure 12 illustrates interrupt acknowledge cycle timing. The address on $AD_0 - AD_7$ and the state of \overline{CS}_0 and \overline{INTACK} are latched by the rising edge of \overline{AS} . However, if \overline{INTACK} is Low, the address and \overline{CS}_0 are ignored. The state of R/\overline{W} and CS_1 are also ignored for the duration of the interrupt acknowledge cycle. Between the rising edge of \overline{AS} and the falling edge of \overline{DS} , the internal and external IEI/EIO daisy chains settle. If there is an interrupt pending in the SCC and IEI is High when \overline{DS} falls, the acknowledge cycle was intended for the SCC. In this case, the SCC may be programmed to respond to \overline{DS} Low by placing its interrupt vector on $AD_0 - AD_7$. It then sets the appropriate interrupt-under-service latch internally.

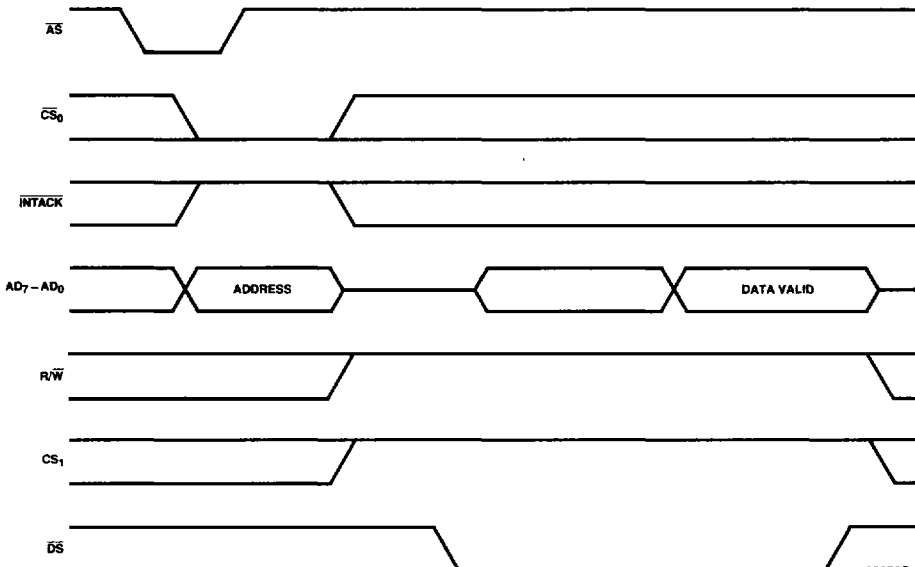
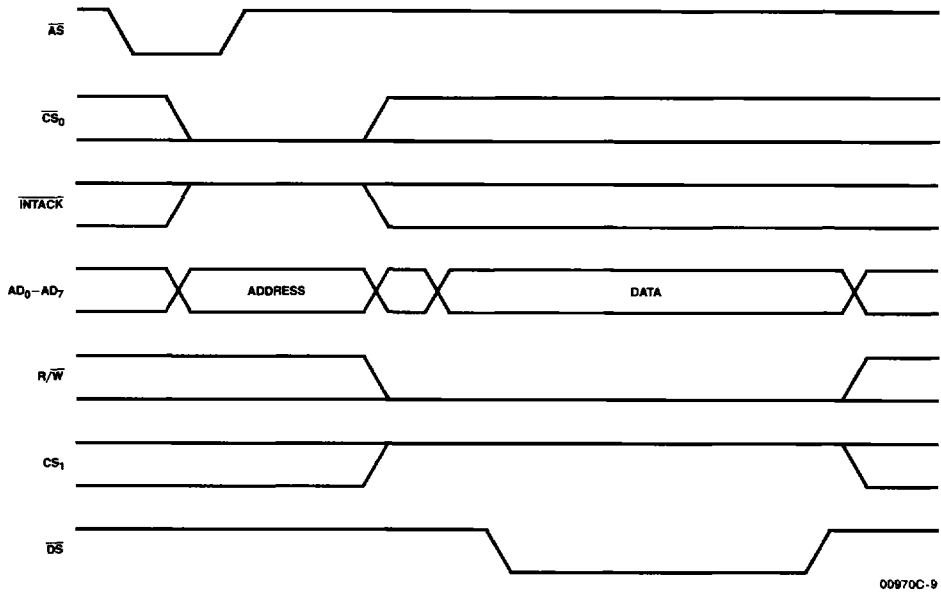


Figure 10. Read Cycle Timing

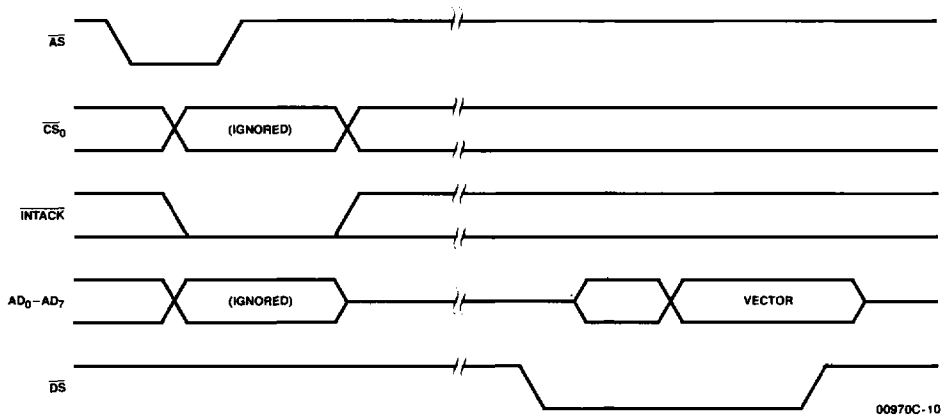
00970C-8





00970C-9

Figure 11. Write Cycle Timing



00970C-10

Figure 12. Interrupt Acknowledge Cycle Timing

AmZ8530 TIMING

The SCC generates internal control signals from \overline{WR} and \overline{RD} that are related to PCLK. Since PCLK has no phase relationship with \overline{WR} and \overline{RD} , the circuitry generating these internal control signals must provide time for metastable conditions to disappear. This gives rise to a recovery time related to PCLK. The recovery time applies only between bus transactions involving the SCC. The recovery time required for proper operation is specified from the rising edge of \overline{WR} or \overline{RD} in the first transaction involving the SCC to the falling edge of \overline{WR} or \overline{RD} in the second transaction involving the SCC. This time must be at least 6 PCLK cycles plus 200ns.

Read Cycle Timing

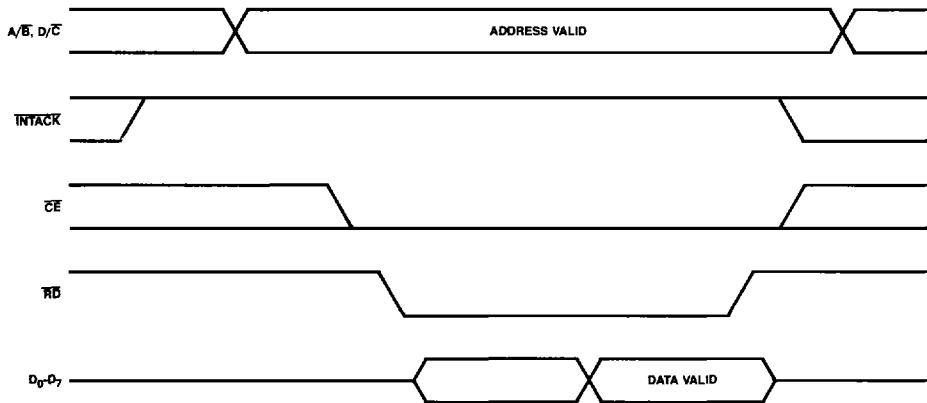
Figure 13 illustrates Read cycle timing. Addresses on A/\overline{B} and D/\overline{C} and the status on \overline{INTACK} must remain stable throughout the cycle. If \overline{CE} falls after \overline{RD} falls or if it rises before \overline{RD} rises, the effective \overline{RD} is shortened.

Write Cycle Timing

Figure 14 illustrates Write cycle timing. Addresses on A/\overline{B} and D/\overline{C} and the status on \overline{INTACK} must remain stable throughout the cycle. If \overline{CE} falls after \overline{WR} falls or if it rises before \overline{WR} rises, the effective \overline{WR} is shortened.

Interrupt Acknowledge Cycle Timing

Figure 15 illustrates Interrupt Acknowledge cycle timing. Between the time \overline{INTACK} goes Low and the falling edge of \overline{RD} , the internal and external IEI/IEO daisy chains settle. If there is an interrupt pending in the SCC and IEI is High when \overline{RD} falls, the Acknowledge cycle is intended for the SCC. In this case, the SCC may be programmed to respond to \overline{RD} Low by placing its interrupt vector on D_0-D_7 and it then sets the appropriate Interrupt-Under-Service internally.



00970C-11

Figure 13. Read Cycle Timing

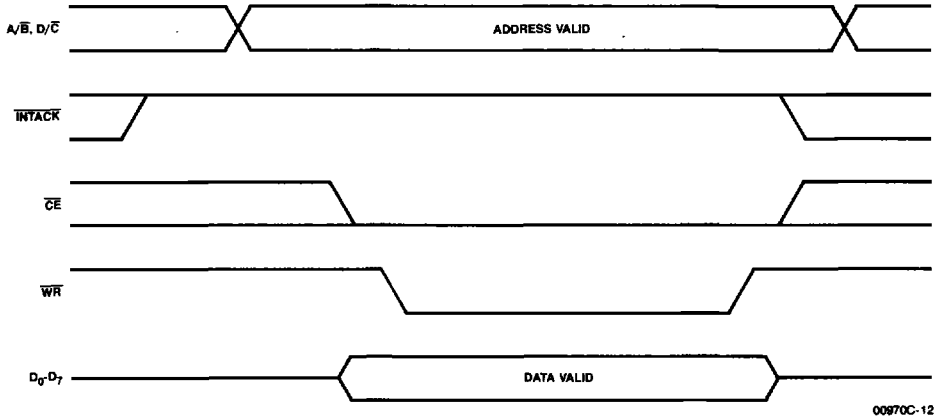


Figure 14. Write Cycle Timing

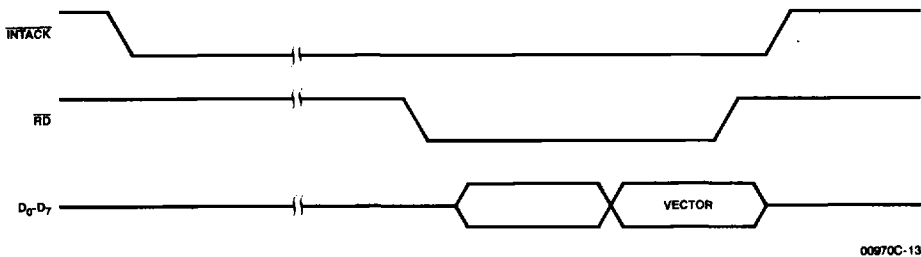


Figure 15. Interrupt Acknowledge Cycle Timing

PIN DESCRIPTIONS FOR AmZ8030

The following section describes the pin functions of the SCC. Figures 16 and 17 detail the respective pin functions and pin assignments.

V_{CC}: +5V Power Supply

GND: Ground

AD₀ – AD₇: Address/Data Bus (bidirectional, active High, 3-state).

These multiplexed lines carry register addresses to the SCC as well as data or control information to and from the SCC.

AS: Address Strobe (Input, active Low).

Addresses on AD₀ – AD₇ are latched by the rising edge of this signal.

CS₀: Chip Select 0 (Input, active Low).

This signal is latched concurrently with the addresses on AD₀ – AD₇ and must be active for the intended bus transaction to occur.

CS₁: Chip Select 1 (Input, active High).

This second select signal must also be active before the intended bus transaction can occur. CS₁ must remain active throughout the transaction.

CTSA, CTSB: Clear to Send (Inputs, active Low).

If these pins are programmed as Auto Enables, a Low on these inputs enables their respective transmitter. If not programmed as Auto Enables, they may be used as general-purpose inputs. Both inputs are Schmitt-trigger buffered to accommodate slow rise-time inputs. The SCC detects pulses on these inputs and can interrupt the CPU on both logic level transitions.

DCDA, DCDB: Data Carrier Detect (Inputs, active Low).

These pins function as receiver enables if they are programmed for Auto Enables; otherwise they may be used as general-purpose input pins. Both pins are Schmitt-trigger buffered to accommodate slow rise-time signals. The SCC detects pulses on these pins and can interrupt the CPU on both logic level transitions.

DS: Data Strobe (Input, active Low).

This signal provides timing for the transfer of data into and out of the SCC. If AS and DS coincide, this is interpreted as a reset.

DTR/REQA, DTR/REQB: Data Terminal Ready/Request (outputs, active Low).

These outputs follow the state programmed into the DTR bit. They can also be used as general-purpose outputs or as Request Lines for a DMA controller.

IEI: Interrupt Enable In (input, active High).

IEI is used with IEO to form an interrupt daisy chain when there is more than one interrupt-driven device. A High IEI indicates that no other higher priority device has an interrupt under service or is requesting an interrupt.

IEO: Interrupt Enable Out (output, active High).

IEO is High only if IEI is High and the CPU is not servicing a SCC interrupt or the SCC is not requesting an interrupt (interrupt acknowledge cycle only). IEO is connected to the next lower priority device's IEI input and thus inhibits interrupts from lower priority devices.

INT: Interrupt Request (output, open-drain, active Low).

This signal is activated when the SCC requests an interrupt.

INTACK: Interrupt Acknowledge (Input, active Low).

This signal indicates an active interrupt acknowledge cycle. During this cycle, the SCC interrupt daisy chain settles. When DS becomes active, the SCC places an interrupt vector on the data bus (if IEI is High). INTACK is latched by the rising edge of AS.

PCLK: Clock (Input)

This is the master SCC clock used to synchronize internal signals. PCLK is not required to have any phase relationship with the master system clock, although the frequency of this clock must be at least 90% of the CPU clock frequency for a Z8000. PCLK is a TTL level signal. Maximum transmit rate is 1/4 PCLK.

RxDA, RxDB: Receive Data (Inputs, active High)

These input signals receive serial data at standard TTL levels.

RTxCA, TRxCB: Receive/Transmit Clocks (Inputs, active Low)

These pins can be programmed in several different modes of operation. In each channel, RTxC may supply the receive clock,

the transmit clock, the clock for the baud-rate generator, or the clock of the digital phase-locked loop. These pins can also be programmed for use with the respective SYNC pins as a crystal oscillator. The receive clock may be 1, 16, 32, or 64 times the data rate in asynchronous modes.

RTSA, RTSB: Request to Send (outputs active Low)

When the Request to Send RTS bit in Write Register 5 (Figure 6) is set, the RTS signal goes Low. When the RTS bit is reset in the Asynchronous mode and Auto Enable is on, the signal goes High after the transmitter is empty. In Synchronous mode or in Asynchronous mode with Auto Enable off, the RTS pins strictly follow the state of the RTS bit. Both pins can be used as general-purpose outputs.

R/W: Read/Write (Input)

This signal specifies whether the operation to be performed is read or a write.

SYNCA, SYNCB: Synchronization (inputs or outputs, active Low)

These pins can act either as inputs, outputs, or part of the crystal oscillator circuit.

In the Asynchronous Receive mode (crystal oscillator option not selected), these pins are inputs similar to CTSA and DCDA. In this mode, transitions on these lines affect the state of the Synchronous/Hunt status bits in Read Register 0 (Figure 5) but have no other function.

In External Synchronization mode with the crystal oscillator not selected, these lines also act as inputs. In this mode, SYNC must be driven Low two receive clock cycles after the last bit in the Synchronous character is received. Character assembly begins on the rising edge of the receive clock immediately preceding the activation of SYNC.

In the Internal Synchronization mode (Monosync and Bisync) with the crystal oscillator not selected, these pins act as outputs and are active only during the part of the receive clock cycle in which synchronous characters are recognized. The synchronous condition is not latched, so these outputs are active each time a synchronous pattern is recognized (regardless of character boundaries). In SDLC mode, these pins act as outputs and are valid on receipt of a flag.

TxDA, TxDB: Transmit Data (outputs, active High)

These output signals transmit serial data at standard TTL levels.

TRxCA, TRxCB: Transmit/Receive Clocks (Inputs or outputs, active Low)

These pins can be programmed in several different modes of operation. TRxC may supply the receive clock or the transmit clock in the input mode or supply the output of the digital phase-locked loop, the crystal oscillator, the baud rate generator, or the transmit clock in the output mode.

W/REQA, W/REQB: Wait/Request (outputs, open-drain when programmed for a Wait function, driven High or Low when programmed for a Request function)

These dual-purpose outputs may be programmed as Request lines for a DMA controller or as Wait lines to synchronize the CPU to the SCC data rate. The reset state is Wait.

PIN DESCRIPTIONS FOR AmZ8530

The following section describes the pin functions of the SCC. Figures 18 and 19 detail the respective pin functions and pin assignments.

V_{CC}: +5V Power Supply

GND: Ground

A/ \bar{B} . *Channel A/Channel B Select* (input). This signal selects the channel in which the read or write operation occurs.

\overline{CE} . *Chip Enable* (input, active Low). This signal selects the SCC for a read or write operation.

$\overline{CTS_A}$, $\overline{CTS_B}$. *Clear To Send* (inputs, active Low). If these pins are programmed as Auto Enables, a Low on the inputs enables the respective transmitters. If not programmed as Auto Enables, they may be used as general-purpose inputs. Both inputs are Schmitt-trigger buffered to accommodate slow rise-time inputs. The SCC detects pulses on these inputs and can interrupt the CPU on both logic level transitions.

$\overline{D/C}$. *Data/Control Select* (input). This signal defines the type of information transferred to or from the SCC. A High means data is transferred; a Low indicates a command.

\overline{DCDA} , \overline{DCDB} . *Data Carrier Detect* (inputs, active Low). These pins function as receiver enables if they are programmed for Auto Enables; otherwise they may be used as general-purpose input pins. Both pins are Schmitt-trigger buffered to accommodate slow rise time signals. The SCC detects pulses on these pins and can interrupt the CPU on both logic level transitions.

D_0 - D_7 . *Data Bus* (bidirectional, 3-state). These lines carry data and commands to and from the SCC.

$\overline{DTR/REQA}$, $\overline{DTR/REQB}$. *Data Terminal Ready/Request* (outputs, active Low). These outputs follow the state programmed into the DTR bit. They can also be used as general-purpose outputs or as Request lines for a DMA controller.

IEI. *Interrupt Enable In* (input, active High). IEI is used with IEO to form an interrupt daisy chain when there is more than one interrupt-driven device. A High IEI indicates that no other higher priority device has an interrupt under service or is requesting an interrupt.

IEO. *Interrupt Enable Out* (output, active High). IEO is High only if IEI is High and the CPU is not servicing an SCC interrupt or the SCC is not requesting an interrupt (Interrupt Acknowledge cycle only). IEO is connected to the next lower priority device's IEI input and thus inhibits interrupts from lower priority devices.

\overline{INT} . *Interrupt Request* (output, open-drain, active Low). This signal is activated when the SCC requests an interrupt.

\overline{INTACK} . *Interrupt Acknowledge* (input, active Low). This signal indicates an active Interrupt Acknowledge cycle. During this cycle, the SCC interrupt daisy chain settles. When \overline{RD} becomes active, the SCC places an interrupt vector on the data bus (if IEI is High). \overline{INTACK} is latched by the rising edge of PCLK.

PCLK. *Clock* (input). This is the master SCC clock used to synchronize internal signals. PCLK is a TTL level signal.

\overline{RD} . *Read* (input, active Low). This signal indicates a read operation and when the SCC is selected, enables the SCC's bus drivers. During the Interrupt Acknowledge cycle, this signal gates the interrupt vector onto the bus if the SCC is the highest priority device requesting an interrupt.

$\overline{RxD_A}$, $\overline{RxD_B}$. *Receive Data* (inputs, active High). These input signals receive serial data at standard TTL levels.

\overline{RTxCA} , \overline{RTxCB} . *Receive/Transmit Clocks* (inputs, active Low). These pins can be programmed in several different modes of operation. In each channel, \overline{RTxC} may supply the receive clock, the transmit clock, the clock for the baud rate generator, or the clock for the Digital Phase-Locked Loop. These pins can also be programmed for use with the respective SYNC pins as a crystal oscillator. The receive clock may be 1, 16, 32, or 64 times the data rate in Asynchronous modes.

\overline{RTSA} , \overline{RTSB} . *Request To Send* (outputs active Low). When the Request to Send (RTS) bit in Write Register 5 (Figure 6) is set, the \overline{RTS} signal goes Low. When the RTS bit is reset in the Asynchronous mode and Auto Enable is on, the signal goes High after the transmitter is empty. In Synchronous mode or in Asynchronous mode with Auto Enable off, the \overline{RTS} pin strictly follows the state of the RTS bit. Both pins can be used as general-purpose outputs.

\overline{SYNCA} , \overline{SYNCB} . *Synchronization* (inputs or outputs, active Low). These pins can act either as inputs, outputs, or part of the crystal oscillator circuit. In the Asynchronous Receive mode (crystal oscillator option not selected), these pins are inputs similar to \overline{CTS} and \overline{DCD} . In this mode, transitions on these lines affect the state of the Synchronous/Hunt status bits in Read Register 0 (Figure 5) but have no other function.

In External Synchronization mode with the crystal oscillator not selected, these lines also act as inputs. In this mode, \overline{SYNC} must be driven Low two receive clock cycles after the last bit in the synchronous character is received. Character assembly begins on the rising edge of the receive clock immediately preceding the activation of \overline{SYNC} .

In the Internal Synchronization mode (Monosync and Bisync) with the crystal oscillator not selected, these pins act as outputs and are active only during the part of the receive clock cycle in which synchronous characters are recognized. The synchronous condition is not latched, so these outputs are active each time a synchronization pattern is recognized (regardless of character boundaries). In SDLC mode, these pins act as outputs and are valid on receipt of a flag.

$\overline{TxD_A}$, $\overline{TxD_B}$. *Transmit Data* (outputs, active High). These output signals transmit serial data at standard TTL levels.

\overline{TRxCA} , \overline{TRxCB} . *Transmit/Receive Clocks* (inputs or outputs, active Low). These pins can be programmed in several different modes of operation. \overline{TRxC} may supply the receive clock or the transmit clock in the input mode or supply the output of the Digital Phase-Locked Loop, the crystal oscillator, the baud rate generator, or the transmit clock in the output mode.

\overline{WR} . *Write* (input, active Low). When the SCC is selected, this signal indicates a write operation. The coincidence of \overline{RD} and \overline{WR} is interpreted as a reset.

$\overline{W/REQA}$, $\overline{W/REQB}$. *Wait/Request* (outputs, open-drain when programmed for a Wait function, driven High or Low when programmed for a Request function). These dual-purpose outputs may be programmed as Request lines for a DMA controller or as Wait lines to synchronize the CPU to the SCC data rate. The reset state is Wait.

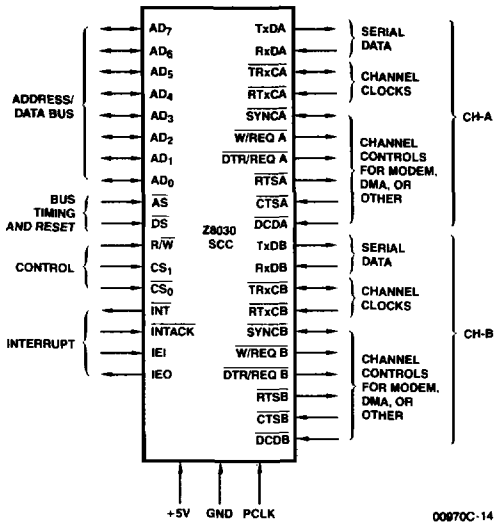
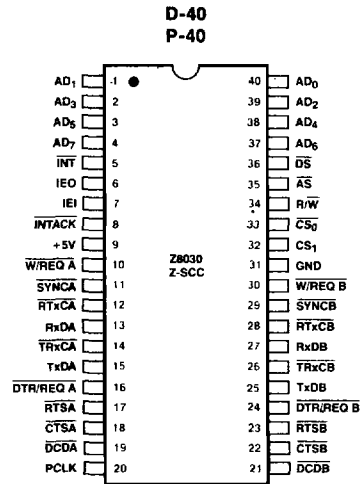


Figure 16. Logic Symbol

00670C-14



Note: Pin 1 is marked for orientation.

00670C-15

Figure 17. Connection Diagram

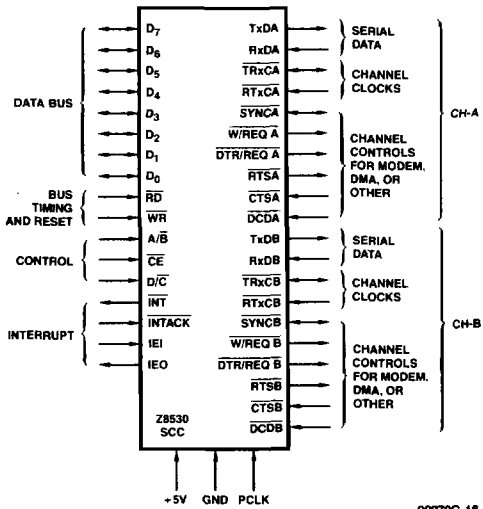
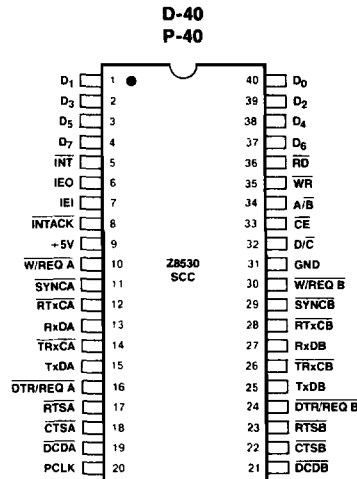


Figure 18. Logic Symbol

00670C-16

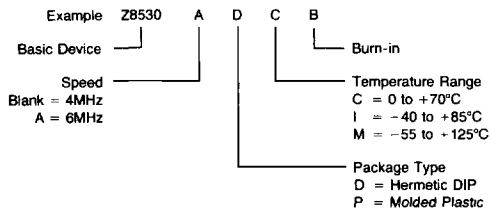
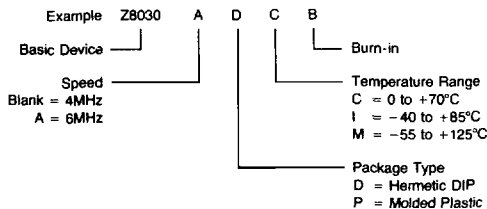


Note: Pin 1 is marked for orientation.

00670C-17

Figure 19. Connection Diagram

ORDERING INFORMATION



AmZ8030/AmZ8530

MAXIMUM RATINGS beyond which useful life may be impaired

Storage Temperature	-65 to +150°C
Voltage at any Pin Relative to V _{SS}	-0.5 to +7.0V
Power Dissipation	1.8W

The products described by this specification include internal circuitry designed to protect input devices from damaging accumulations of static charge. It is suggested, nevertheless, that conventional precautions be observed during storage, handling and use in order to avoid exposure to excessive voltages.

OPERATING RANGE

(over which the DC, switching and functional specifications apply)

	4MHz	6MHz
Commercial Operating Range T _A = 0 to +70°C V _{CC} = 5V ± 5%	Z8030DC Z8030PC Z8530DC Z8530PC	Z8030ADC Z8030APC Z8530ADC Z8530APC
Industrial Operating Range T _A = -40 to +85°C V _{CC} = 5V ± 5%	Z8030DI Z8530DI	
Military Operating Range T _A = -55 to +125°C V _{CC} = 5V ± 10%	Z8030DMB Z8530DMB	

Notes: T_A denotes ambient temperature.
Add suffix B to indicate burn-in requirement.

ELECTRICAL CHARACTERISTICS

Parameter	Description	Test Conditions	Min	Typ	Max	Units
V _{IH}	Input HIGH Voltage	Standard	2.0		V _{CC} + 0.3	V
		Military	2.2			
V _{IL}	Input LOW Voltage		-0.3		0.8	V
V _{OH}	Output HIGH Voltage	I _{OH} = -250μA	2.4			V
V _{OL}	Output LOW Voltage	I _{OL} = +2.0mA			0.4	V
I _{IL}	Input Leakage	0.4 ≤ V _{IN} ≤ +2.4V			±10.0	μA
I _{OL}	Output Leakage	0.4 ≤ V _{OUT} ≤ +2.4V			±10.0	μA
I _{CC}	V _{CC} Supply Current				250	mA
C _{IN}	Input Capacitance	Unmeasured pins returned to ground. f = 1MHz over specified temperature range.			10	pF
C _{OUT}	Output Capacitance				15	pF
C _{I/O}	Bidirectional Capacitance				20	pF

V_{CC} = 5V ± 5% unless otherwise specified, over specified temperature range.

Standard Test Conditions

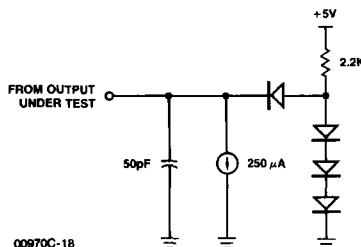
The characteristics below apply for the following standard test conditions, unless otherwise noted. All voltages are referenced to GND. Positive current flows into the referenced pin. Standard conditions are as follows:

$$+4.75V \leq V_{CC} \leq +5.25V$$

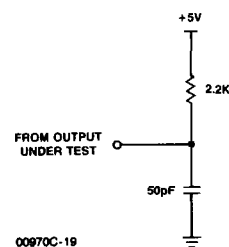
$$GND = 0V$$

$$0^\circ C \leq T_A \leq +70^\circ C$$

Standard Test Load



Open Drain Test Load



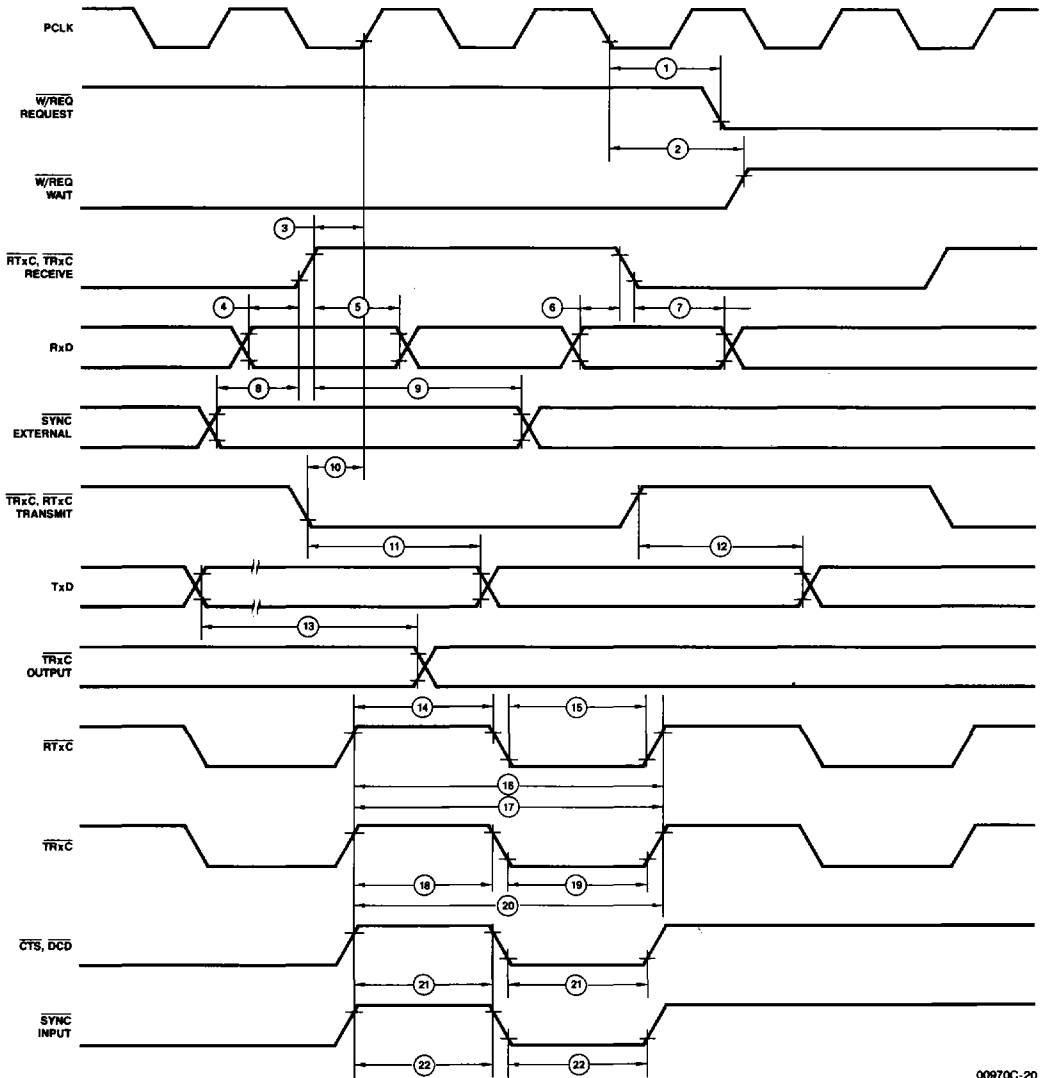
GENERAL TIMING

Number	Parameter	Description	4MHz		6MHz		Units
			Min	Max	Min	Max	
1	TdPC(REQ)	PCLK ↓ to $\overline{W/REQ}$ Valid Delay		250		250	ns
2	TdPC(W)	PCLK ↓ to Wait Inactive Delay		350		350	ns
3	TsRXC(PC)	\overline{RxC} ↑ to PCLK ↑ Setup Time (Notes 1, 4)	50		50		ns
4	TsRXD(RXCr)	RxD to \overline{RxC} ↑ Setup Time (XI Mode) (Note 1)	0		0		ns
5	ThRXD(RXCr)	RxD to \overline{RxC} ↑ Hold Time (XI Mode) (Note 1)	150		150		ns
6	TsRXD(RXCI)	RxD to \overline{RxC} ↓ Setup Time (XI Mode) (Notes 1, 5)	0		0		ns
7	ThRXD(RXCI)	RxD to \overline{RxC} ↓ Hold Time (XI Mode) (Notes 1, 5)	150		150		ns
8	TsSY(RXC)	\overline{SYNC} to \overline{RxC} ↑ Setup Time (Note 1)	-200		-200		ns
9	ThSY(RXC)	\overline{SYNC} to \overline{RxC} ↑ Hold Time (Note 1)	3TcPC +200		3TcPC +200		ns
10	TsTXC(PC)	\overline{TxC} ↓ to PCLK ↑ Setup Time (Notes 2, 4)	0		0		ns
11	TdTXC(TXD)	\overline{TxC} ↓ to TxD Delay (XI Mode) (Note 2)		300		300	ns
12	TdTXCr(TXD)	\overline{TxC} ↑ to TxD Delay (XI Mode) (Notes 2, 5)		300		300	ns
13	TdTXD(TRX)	TxD to \overline{TRxC} Delay (Send Clock Echo)					ns
14	TwRTXh	\overline{RTxC} High Width	180		180		ns
15	TwRTXI	\overline{RTxC} Low Width	180		180		ns
16	TcRTX	\overline{RTxC} Cycle Time	400		400		ns
17	TcRTXX	Crystal Oscillator Period (Note 3)	250	1000	250	1000	ns
18	TwTRXh	\overline{TRxC} High Width	180		180		ns
19	TwTRXI	\overline{TRxC} Low Width	180		180		ns
20	TcTRX	\overline{TRxC} Cycle Time	400		400		ns
21	TwEXT	DCD or CTS Pulse Width	200		200		ns
22	TwSY	\overline{SYNC} Pulse Width	200		200		ns

- Notes: 1. RxC is \overline{RTxC} or \overline{TRxC} , whichever is supplying the receive clock.
2. TxC is \overline{TRxC} or \overline{RTxC} , whichever is supplying the transmit clock.
3. Both \overline{RTxC} and \overline{SYNC} have 30pF capacitors to ground connected to them.
4. Parameter applies only if the data rate is one-fourth the PCLK rate. In all other cases, no phase relationship between \overline{RxC} and PCLK or \overline{TxC} and PCLK is required.
5. Parameter applies only to FM encoding/decoding.
6. Parameter applies only if \overline{RTxC} is used directly as Tx or Rx clock. If used as a DPLL or BR source, specifications are the same as PCLK (4MHz).

*Timings are preliminary and subject to change.

Figure 20. General Timing

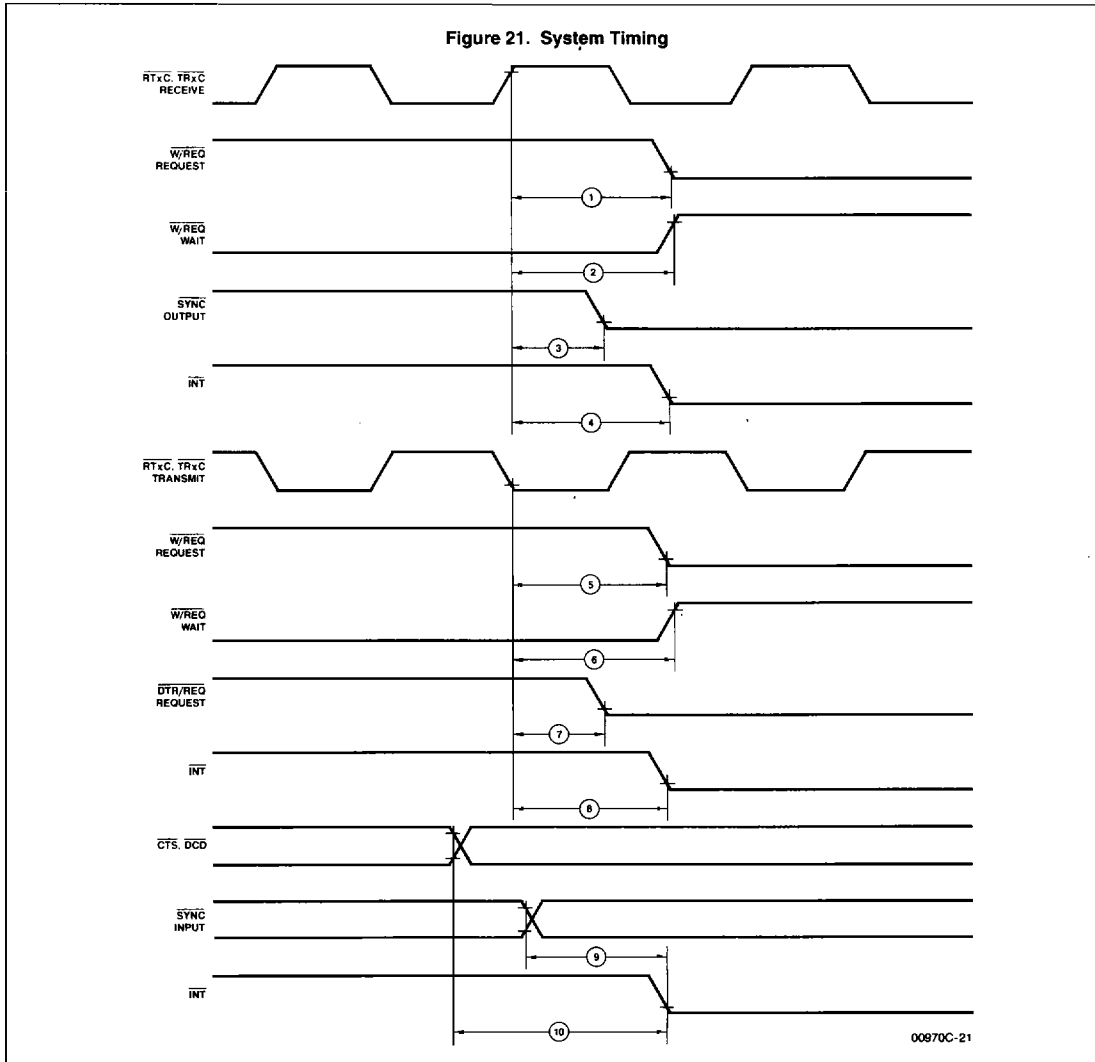


00970C-20

SYSTEM TIMING

Number	Parameter	Description	4MHz		6MHz		Units
			Min	Max	Min	Max	
1	TdRXC(REQ)	$\overline{RxC} \uparrow$ to $\overline{W/REQ}$ Valid Delay (Note 2)	8	12	8	12	TcPC
2	TdRXC(W)	$\overline{RxC} \uparrow$ to Wait Inactive Delay (Notes 1, 2)	8	12	8	12	TcPC
3	TdRXC(SY)	$\overline{RxC} \uparrow$ to \overline{SYNC} Valid Delay (Note 2)	4	7	4	7	TcPC
4	TdRXC(INT)	$\overline{RxC} \uparrow$ to \overline{INT} Valid Delay (Notes 1, 2)	10	16	10	16	TcPC
5	TdTXC(REQ)	$\overline{TxC} \downarrow$ to $\overline{W/REQ}$ Valid Delay (Note 3)	5	8	5	8	TcPC
6	TdTXC(W)	$\overline{TxC} \downarrow$ to Wait Inactive Delay (Notes 1, 3)	5	8	5 <td 8	TcPC	
7	TdTXC(DRQ)	$\overline{TxC} \downarrow$ to $\overline{DTR/REQ}$ Valid Delay (Note 3)	4	7	4	7	TcPC
8	TdTXC(INT)	$\overline{TxC} \downarrow$ to \overline{INT} Valid Delay (Notes 1, 3)	6	10	6	10	TcPC
9	TdSY(INT)	\overline{SYNC} Transition to \overline{INT} Valid Delay (Note 1)	2	6	2	6	TcPC
10	TdEXT(INT)	\overline{DCD} or \overline{CTS} Transition to \overline{INT} Valid Delay (Note 1)	2	6	2	6	TcPC

Notes: 1. Open-drain output, measured with open-drain test load. 3. \overline{TxC} is \overline{TRxC} or \overline{RTxC} , whichever is supplying the transmit clock.
 2. \overline{RxC} is \overline{RTxC} or \overline{TRxC} , whichever is supplying the receive clock. *Timings are preliminary and subject to change.

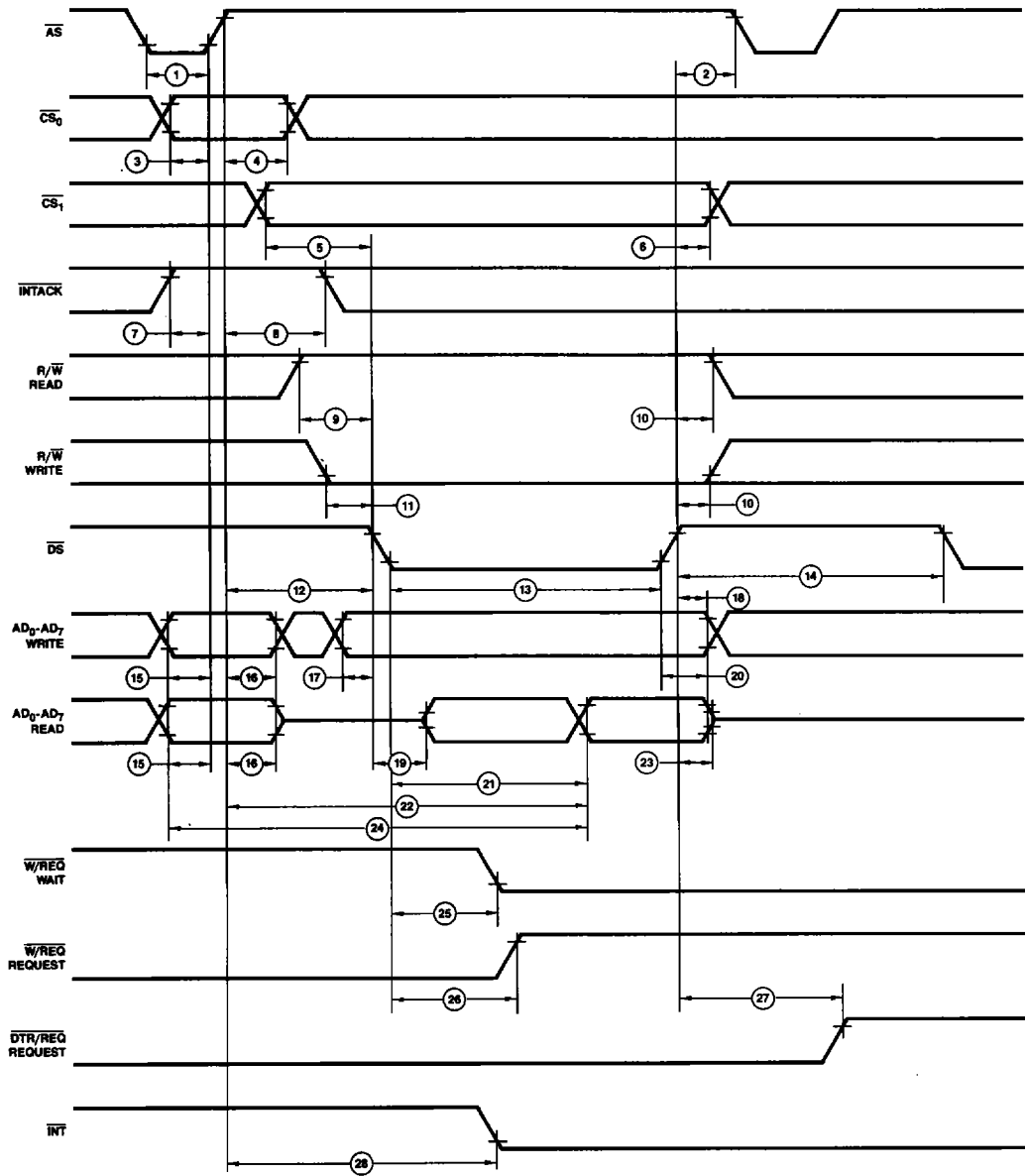


AmZ8030/AmZ8530
READ AND WRITE TIMING (AmZ8030)

Number	Parameter	Description	4MHz		6MHz		Units
			Min	Max	Min	Max	
1	TwAS	\overline{AS} LOW Width	70		50		ns
2	TdDS(AS)	$\overline{DS} \uparrow$ to $\overline{AS} \downarrow$ Delay	50		25		ns
3	TsCS0(AS)	\overline{CS}_0 to $\overline{AS} \uparrow$ Setup Time (Note 1)	0		0		ns
4	ThCS0(AS)	\overline{CS}_0 to $\overline{AS} \uparrow$ Hold Time (Note 1)	60		40		ns
5	TsCS1(DS)	CS_1 to $\overline{DS} \downarrow$ Setup Time (Note 1)	100		80		ns
6	ThCS1(DS)	CS_1 to $\overline{DS} \uparrow$ Hold Time (Note 1)	55		40		ns
7	TsIA(AS)	\overline{INTACK} to $\overline{AS} \uparrow$ Setup Time	0		0		ns
8	ThIA(AS)	\overline{INTACK} to $\overline{AS} \uparrow$ Hold Time	250		250		ns
9	TsRWR(DS)	R/\overline{W} (Read) to $\overline{DS} \downarrow$ Setup Time	100		80		ns
10	ThRW(DS)	R/\overline{W} to $\overline{DS} \uparrow$ Hold Time	55		40		ns
11	TsRWW(DS)	R/\overline{W} (Write) to $\overline{DS} \downarrow$ Setup Time	0		0		ns
12	TdAS(DS)	$\overline{AS} \uparrow$ to $\overline{DS} \downarrow$ Delay	60		40		ns
13	TwDSI	\overline{DS} LOW Width	390		250		ns
14	TrC	Valid Access Recovery Time (Note 2)	6TcPC +200		6TcPC +130		ns
15	TsA(AS)	Address to $\overline{AS} \uparrow$ Setup Time (Note 1)	30		10		ns
16	ThA(AS)	Address to $\overline{AS} \uparrow$ Hold Time (Note 1)	50		30		ns
17	TsDW(DS)	Write Data to $\overline{DS} \downarrow$ Setup Time	30		20		ns
18	ThDW(DS)	Write Data to $\overline{DS} \uparrow$ Hold Time	30		20		ns
19	TdDS(DA)	$\overline{DS} \downarrow$ to Data Active Delay	0		0		ns
20	TdDSr(DR)	$\overline{DS} \uparrow$ to Read Data Not Valid Delay	0		0		ns
21	TdDSf(DR)	$\overline{DS} \downarrow$ to Read Data Valid Delay		250		180	ns
22	TdAS(DR)	$\overline{AS} \uparrow$ to Read Data Valid Delay		520		335	ns

- Notes: 1. Parameter does not apply to Interrupt Acknowledge transactions.
2. Parameter applies only between transactions involving the 8030.

Figure 22. Read and Write Timing (AmZ8030)



00970C-22

AmZ8030/AmZ8530

INTERRUPT ACKNOWLEDGE TIMING, RESET TIMING, CYCLE TIMING (AmZ8030)

Number	Parameter	Description	4MHz		6MHz		Units
			Min	Max	Min	Max	
23	TdDS(DRz)	$\overline{DS} \uparrow$ to Read Data Float Delay (Note 3)		70		45	ns
24	TdA(DR)	Address Required Valid to Read Data Valid Delay		570		420	ns
25	TdDS(W)	$\overline{DS} \downarrow$ to Wait Valid Delay (Note 4)		240		200	ns
26	TdDSf(REQ)	$\overline{DS} \downarrow$ to $\overline{W}/\overline{REQ}$ Not Valid Delay		240		200	ns
27	TdDSr(REQ)	$\overline{DS} \downarrow$ to $\overline{DTR}/\overline{REQ}$ Not Valid Delay		5TcPC +300		5TcPC +250	ns
28	TdAS(INT)	$\overline{AS} \uparrow$ to \overline{INT} Valid Delay (Note 4)		500		500	ns
29	TdAS(DSA)	$\overline{AS} \uparrow$ to $\overline{DS} \downarrow$ (Acknowledge) Delay (Note 5)					ns
30	TwDSA	\overline{DS} (Acknowledge) Low Width	390		250		ns
31	TdDSA(DR)	$\overline{DS} \downarrow$ (Acknowledge) to Read Data Valid Delay		250		180	ns
32	TsIEI(DSA)	IEI to $\overline{DS} \downarrow$ (Acknowledge) Setup Time	120		100		ns
33	ThIEI(DSA)	IEI to $\overline{DS} \uparrow$ (Acknowledge) Hold Time	0		0		ns
34	TdIEI(IEO)	IEI to IEO Delay		120		100	ns
35	TdAS(IEO)	$\overline{AS} \uparrow$ to IEO Delay (Note 6)		250		250	ns
36	TdDSA(INT)	$\overline{DS} \downarrow$ (Acknowledge) to \overline{INT} Inactive Delay (Note 4)		500		500	ns
37	TdDS(ASQ)	$\overline{DS} \uparrow$ to $\overline{AS} \downarrow$ Delay for No Reset	30		15		ns
38	TdASQ(DS)	$\overline{AS} \uparrow$ to $\overline{DS} \downarrow$ Delay for No Reset	30		30		ns
39	TwRES	\overline{AS} and \overline{DS} Coincident Low for Reset (Note 7)	250		250		ns
40	TwPCI	PCLK Low Width	105	2000	70	1000	ns
41	TwPCh	PCLK High Width	105	2000	70	1000	ns
42	TcPC	PCLK Cycle Time	250	4000	165	2000	ns
43	TrPC	PCLK Rise Time		20		15	ns
44	TfPC	PCLK Fall Time		20		10	ns

Notes: 3. Float delay is defined as the time required for a $\pm 0.5V$ change in the output with a maximum dc load and minimum ac load.

4. Open-drain output, measured with open-drain test load.

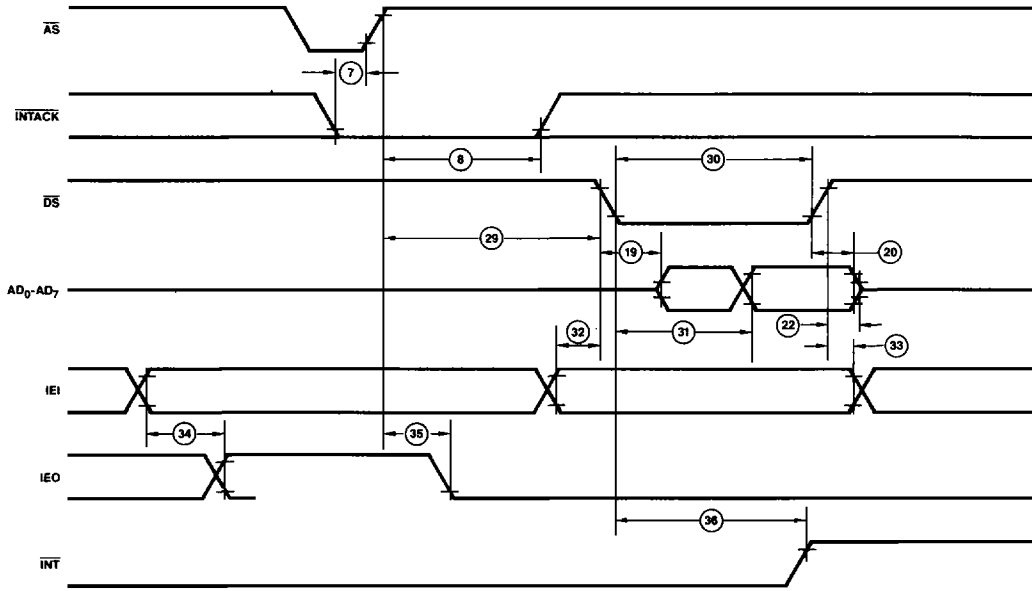
5. Parameter is system dependent. For any 8030 in the daisy chain, TdAS(DSA) must be greater than the sum of TdAS(IEO) for the highest priority device in the daisy chain, TsIEI(DSA) for the 8030, and TdIEI(IEO) for each device separating them in the daisy chain.

6. Parameter applies only to a 8030 pulling \overline{INT} Low at the beginning of the Interrupt Acknowledge transaction.

7. Internal circuitry allows for the reset provided by the Z8 to be recognized as a reset by the 8030.

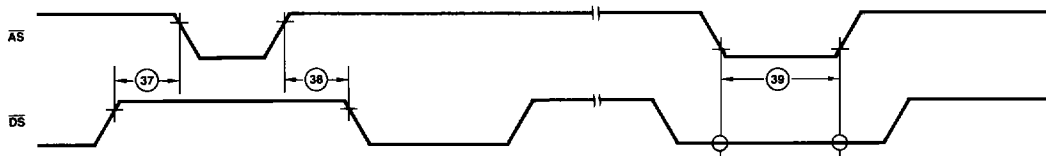
All timing references assume 2.0V for a logic "1" and 0.8V for a logic.

Figure 23. Interrupt Acknowledge Timing (AmZ8030)



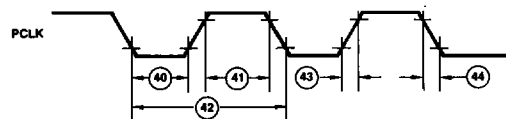
00970C-23

Figure 24. Reset Timing (AmZ8030)



00970C-24

Figure 25. Cycle Timing (AmZ8030)



00970C-25

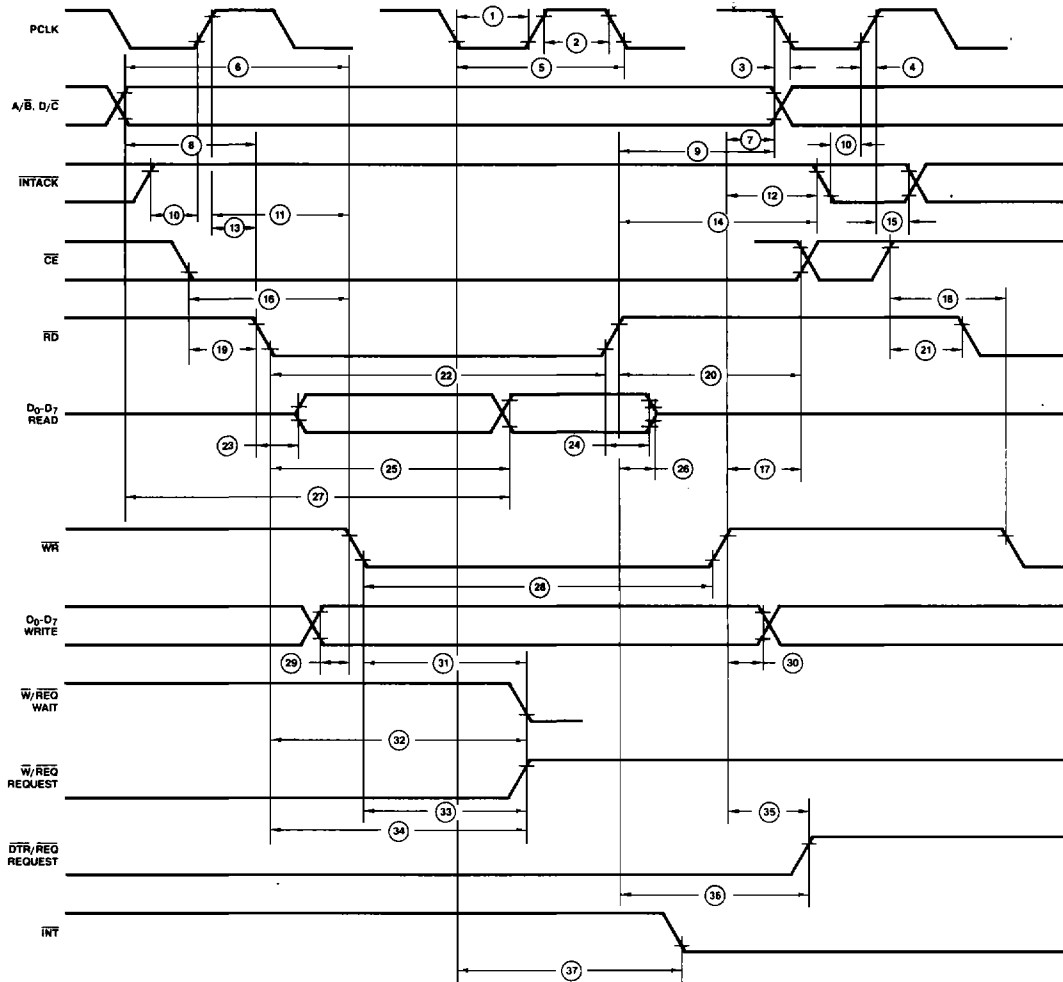
AmZ8030/AmZ8530
READ AND WRITE TIMING (AmZ8530)

Number	Parameter	Description	4MHz		6MHz		Units
			Min	Max	Min	Max	
1	TwPCL	PCLK Low Width	105	2000	70	1000	ns
2	TwPCH	PCLK High Width	105	2000	70	1000	ns
3	TfPCL	PCLK Fall Time		20		10	ns
4	TrPCL	PCLK Rise Time		20		15	ns
5	TcPCL	PCLK Cycle Time	250	4000	165	2000	ns
6	TsA(WR)	Address to \overline{WR} ↓ Setup Time	80		80		ns
7	ThA(WR)	Address to \overline{WR} ↑ Hold Time	0		0		ns
8	TsA(RD)	Address to \overline{RD} ↓ Setup Time	80		80		ns
9	ThA(RD)	Address to \overline{RD} ↑ Hold Time	0		0		ns
10	TsIA(PC)	\overline{INTACK} to PCLK ↑ Setup Time	0		0		ns
11	TsIAi(WR)	\overline{INTACK} to \overline{WR} ↓ Setup Time (Note 1)	200		200		ns
12	ThIA(WR)	\overline{INTACK} to \overline{WR} ↑ Hold Time	0		0		ns
13	TsIAi(RD)	\overline{INTACK} to \overline{RD} ↓ Setup Time (Note 1)	200		200		ns
14	ThIA(RD)	\overline{INTACK} to \overline{RD} ↑ Hold Time	0		0		ns
15	ThIA(PC)	\overline{INTACK} to PCLK ↑ Hold Time	100		100		ns
16	TsCEi(WR)	\overline{CE} Low to \overline{WR} ↓ Setup Time	0		0		ns
17	ThCE(WR)	\overline{CE} to \overline{WR} ↑ Hold Time	0		0		ns
18	TsCEh(WR)	\overline{CE} High to \overline{WR} ↓ Setup Time	100		70		ns
19	TsCEi(RD)	\overline{CE} Low to \overline{RD} ↓ Setup Time (Note 1)	0		0		ns
20	ThCE(RD)	\overline{CE} to \overline{RD} ↑ Hold Time (Note 1)	0		0		ns
21	TsCEh(RD)	\overline{CE} High to \overline{RD} ↓ Setup Time (Note 1)	100		70		ns
22	TwRDI	\overline{RD} Low Width (Note 1)	390		250		ns
23	TdRD(DRA)	\overline{RD} ↓ to Read Data Active Delay	0		0		ns
24	TdRDr(DR)	\overline{RD} ↑ to Read Data Not Valid Delay	0		0		ns
25	TdRD(DR)	\overline{RD} ↓ to Read Data Valid Delay		250		180	ns
26	TdRD(DRz)	\overline{RD} ↑ to Read Data Float Delay (Note 2)		70		45	ns

Notes: 1. Parameter does not apply to Interrupt Acknowledge transactions.

2. Float delay is defined as the time required for a ±0.5V change in the output with a maximum dc load and minimum ac load.

Figure 26. Read and Write Timing (AmZ8530)



00870C-28



AmZ8030/AmZ8530

INTERRUPT ACKNOWLEDGE TIMING, RESET TIMING, CYCLE TIMING (AmZ8530)

Number	Parameter	Description	4MHz		6MHz		Units
			Min	Max	Min	Max	
27	TdA(DR)	Address Required Valid to Read Data Valid Delay		590		420	ns
28	TwWRI	\overline{WR} Low Width	390		250		ns
29	TsDW(WR)	Write Data to \overline{WR} ↓ Setup Time	0		0		ns
30	ThDW(WR)	Write Data to \overline{WR} ↑ Hold Time	0		0		ns
31	TdWR(W)	\overline{WR} ↓ to Wait Valid Delay (Note 4)		240		200	ns
32	TdRD(W)	\overline{RD} ↓ to Wait Valid Delay (Note 4)		240		200	ns
33	TdWRf(REQ)	\overline{WR} ↓ to $\overline{W}/\overline{REQ}$ Not Valid Delay		240		200	ns
34	TdRDf(REQ)	\overline{RD} ↓ to $\overline{W}/\overline{REQ}$ Not Valid Delay		240		200	ns
35	TdWRr(REQ)	\overline{WR} ↑ to $\overline{DTR}/\overline{REQ}$ Not Valid Delay		5TcPC +300		5TcPC +250	ns
36	TdRD r(REQ)	\overline{RD} ↑ to $\overline{DTR}/\overline{REQ}$ Not Valid Delay		5TcPC +300		5TcPC +250	ns
37	TdPC(INT)	PCLK ↓ to \overline{INT} Valid Delay (Note 4)		500		500	ns
38	TdIaI(RD)	\overline{INTACK} to \overline{RD} ↓ (Acknowledge) Delay (Note 5)					ns
39	TwRDA	\overline{RD} (Acknowledge) Width	285		250		ns
40	TdRDA(DR)	\overline{RD} ↓ (Acknowledge) to Read Data Valid Delay		190		180	ns
41	TsIEI(RDA)	IEI to \overline{RD} ↓ (Acknowledge) Setup Time	120		100		ns
42	ThIEI(RDA)	IEI to \overline{RD} ↑ (Acknowledge) Hold Time	0		0		ns
43	TdIEI(IEO)	IEI to IEO Delay Time		120		100	ns
44	TdPC(IEO)	PCLK ↑ to IEO Delay		250		250	ns
45	TdRDA(INT)	\overline{RD} ↓ to \overline{INT} Inactive Delay (Note 4)		500		500	ns
46	TdRD(WRQ)	\overline{RD} ↑ to \overline{WR} ↓ Delay for No Reset	30		15		ns
47	TdWRQ(RD)	\overline{WR} ↑ to \overline{RD} ↓ Delay for No Reset	30		30		ns
48	TwRES	\overline{WR} and \overline{RD} Coincident Low for Reset	250		250		ns
49	Trc	Valid Access Recovery Time (Note 3)	6TcPC +200		6TcPC +130		ns

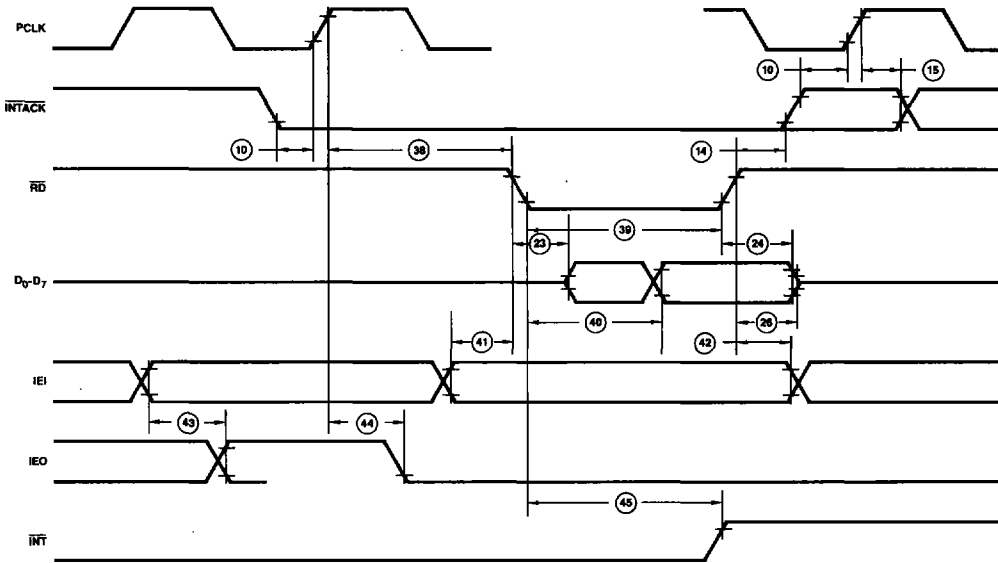
Notes: 3. Parameter applies only between transactions involving the SCC.

4. Open-drain output, measured with open-drain test load.

5. Parameter is system dependent. For any SCC in the daisy chain, TdIaI(RD) must be greater than the sum of TdPC(IEO) for the highest priority device in the daisy chain, TsIEI(RDA) for the SCC, and TdIEI(IEO) for each device separating them in the daisy chain.

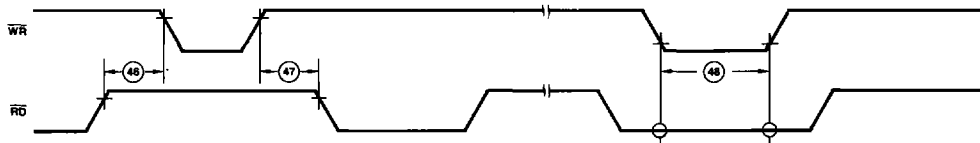
*Timings are preliminary and subject to change.

Figure 27. Interrupt Acknowledge Timing (AmZ8530)



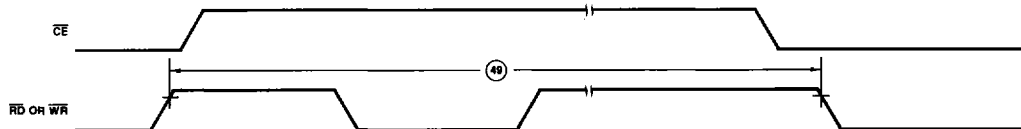
00970C-29

Figure 28. Reset Timing (AmZ8530)



00970C-30

Figure 29. Cycle Timing (AmZ8530)



00970C-31