# Z8030/Z8530(H)

Serial Communications Controller

## DISTINCTIVE CHARACTERISTICS

- **Two 0 to 2 Mbps full duplex serial channels**
  Each channel has independent oscillator, baud-rate generator, and PLL for clock recovery, dramatically reducing external components.
- **Programmable protocols**
  NRZ, NRZI, and FM data encoding supported under program control.
- **Programmable Asynchronous Modes**
  5- to 8-bit characters with programmable stop bits, clock, break detect, and error conditions.
- **Z8000* compatible**
  The Z8030 interfaces directly with the Z8000 CPU bus and to the Z8000 interrupt structure.
- **Programmable Synchronous Modes**
  SDLC and HDLC and SDLC loop supported with frame control, zero insertion and deletion, abort, and residue handling. CRC-16 and CCITT generators and checkers.
- **Compatible with non-multiplexed bus**
  The Z8530(H) interfaces easily to most other CPUs.
- **Enhanced Version**
  The Z8530(H) is an enhanced version whose features include 8-MHz operation and an improved Valid Access Recovery Time ($t_{RC}$) specification.

## GENERAL DESCRIPTION

The SCC Serial Communications Controller is a dual-channel, multi-protocol data communications peripheral designed for use with 8- and 16-bit microprocessors. The SCC functions as a serial-to-parallel, parallel-to-serial converter/controller. The SCC can be software-configured to satisfy a wide variety of serial communications applications. The device contains a variety of new, sophisticated internal functions, including on-chip baud rate generators, digital phase-locked loops, and crystal oscillators, which dramatically reduce the need for external logic.

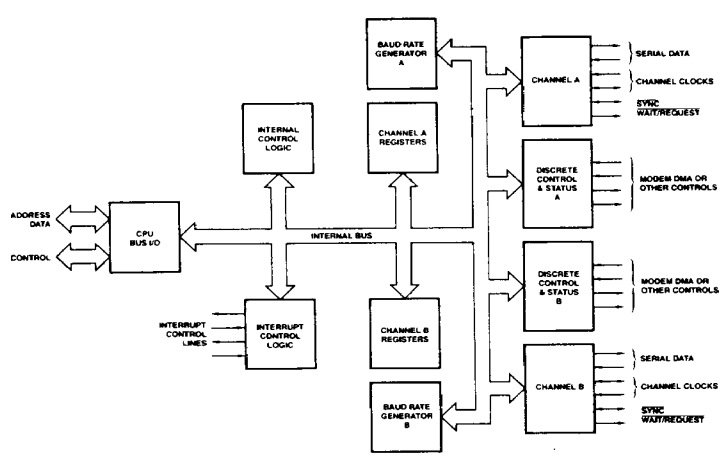
The SCC handles asynchronous formats, synchronous byte-oriented protocols, such as IBM Bisync, and synchronous bit-oriented protocols, such as HDLC and IBM SDLC.

This versatile device supports virtually any serial data transfer application (cassette, diskette, tape drivers, etc.).

The device can generate and check CRC codes in any synchronous mode and can be programmed to check data integrity in various modes. The SCC also has facilities for modem controls in both channels. In applications where these controls are not needed, the modem controls can be used for general-purpose I/O.

The SCC is offered in two versions. The Z8030 is directly compatible with the Z8000 and 8086 CPUs. The Z8530(H) is designed for non-multiplexed buses and is easily interfaced with most other CPUs, such as 8080, Z80, 6800, 68000, and MULTIBUS.†

## BLOCK DIAGRAM




BD003520

**Figure 1.**

* Z8000, Z8030 and Z8530 are trademarks of Zilog, Inc.
†MULTIBUS is a trademark of Intel, Corp.



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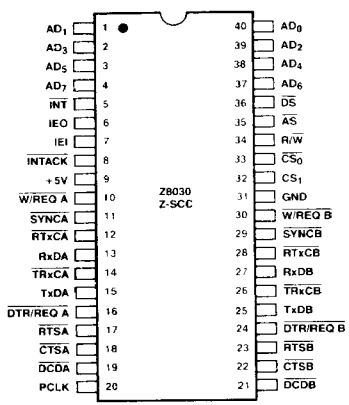
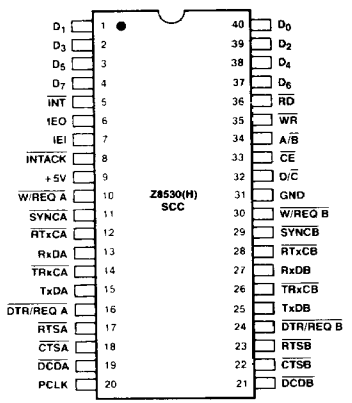
## RELATED AMD PRODUCTS

| Part No. | Description |
|---|---|
| Am79C12 | Full Duplex 1200 bps Modem |
| Am7960 | Coded Data Transceiver |
| 80186 | Highly Integrated 16-Bit Microprocessor |
| 80286 | High-Performance 16-Bit Microprocessor |
| 8080A | 8-Bit Microprocessor |
| Am9517A | DMA Controller |

## CONNECTION DIAGRAMS
### Top View
### DIPs



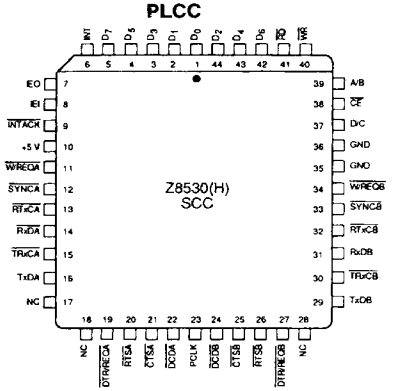

CD005350




CD005361

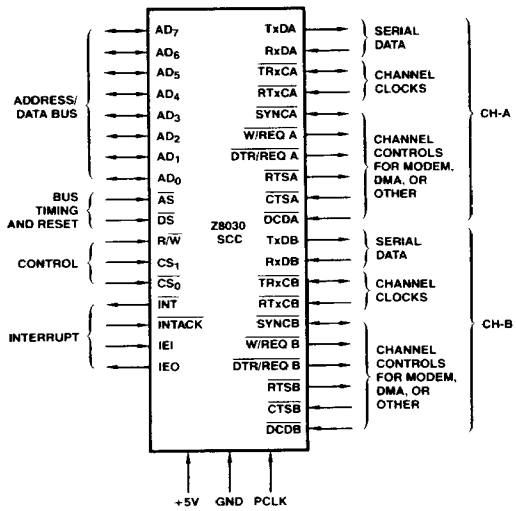
Note: Pin 1 is marked for orientation.

### PLCC

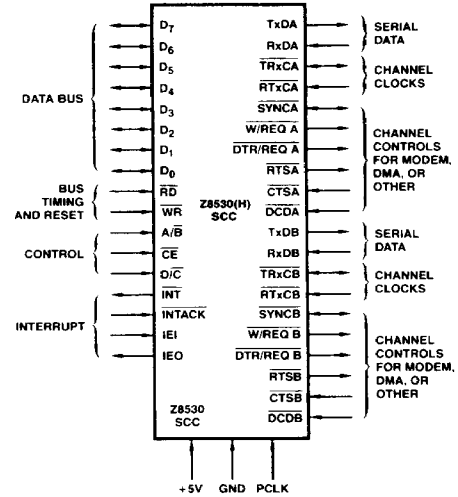



CD010931

## LOGIC SYMBOL




LS001300




LS001312

### Summary of Difference Between Z8530 and Z8530H

| No. | Parameter Symbol | | Z8530 | | Z8530H | |
|---|---|---|---|---|---|---|
| | | | Min. | Max | Min. | Max. |
| 3 | TsRxC (PC) | 4 MHz | 80 | TWPCL | 80 | TWPCL |
| | | 6 MHz | 70 | TWPCL | 70 | TWPCL |
| 27 | Tda (DR) | 4 MHz | | 400 | | 300 |
| | | 6 MHz | | 350 | | 280 |
| 49 | Trc (Note 1) | 4 MHz | 6 TcPC + 200 ns | | 4 TcPC | |
| | | 6 MHz | 6 TcPC + 130 ns | | 4 TcPC | |

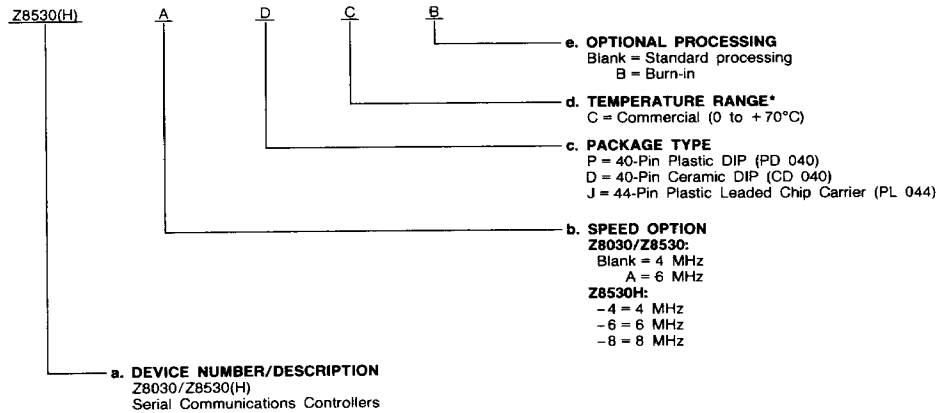
Notes: 1. Z8530 is measured from Rising Edge to Falling Edge:
Z8530H is measured from Falling Edge to Falling Edge.

*The Z8530H is available in an 8-MHz version; the Z8530 is not.

# ORDERING INFORMATION

## Commodity Products

AMD commodity products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of: **a. Device Number**
**b. Speed Option** (if applicable)
**c. Package Type**
**d. Temperature Range**
**e. Optional Processing**




| Valid Combinations | |
|---|---|
| Z8030 | PC, DC, DCB |
| Z8030A | |
| Z8530 | PC, DC, DCB, JC |
| Z8530A | |
| Z8530H-4 | |
| Z8530H-6 | |
| Z8530H-8 | |

### Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

*This device is also available in Military temperature range. See MOS Microprocessors and Peripherals Military Handbook (Order #09275A/0) for electrical performance characteristics.

## Z8030 PIN DESCRIPTION

| Pin No. | Name | I/O | Description |
|---|---|---|---|
| 9 | $V_{CC}$ | | +5V Power Supply. |
| 31 | GND | | Ground. |
| 40, 1, 39, 2, 38, 3, 37, 4 | $AD_0$-$AD_7$ | I/O | Address/Data Bus (bidirectional, active High, 3-state). These multiplexed lines carry register addresses to the SCC as well as data or control information to and from the SCC. |
| 35 | $\overline{AS}$ | I | Address Strobe (active Low). Addresses on $AD_0$-$AD_7$ are latched by the rising edge of this signal. |
| 33 | $\overline{CS_0}$ | I | Chip Select 0 (active Low). This signal is latched concurrently with the addresses on $AD_0$-$AD_7$ and must be active for the intended bus transaction to occur. |
| 32 | $CS_1$ | I | Chip Select 1 (active High). This second select signal must also be active before the intended bus transaction can occur. $CS_1$ must remain active throughout the transaction. |
| 18, 22 | $\overline{CTSA}$, $\overline{CTSB}$ | I | Clear to Send (active Low). If these pins are programmed as Auto Enables, a LOW on these inputs enables their respective transmitter. If not programmed as Auto Enables, they may be used as general-purpose inputs. Both inputs are Schmitt-trigger buffered to accommodate slow rise-time inputs. The SCC detects pulses on these inputs and can interrupt the CPU on both logic level transitions. |
| 19, 21 | $\overline{DCDA}$, $\overline{DCDB}$ | I | Data Carrier Detect (active Low). These pins function as receiver enables if they are programmed for Auto Enables; otherwise, they may be used as general-purpose input pins. Both pins are Schmitt-trigger buffered to accommodate slow rise-time signals. The SCC detects pulses on these pins and can interrupt the CPU on both logic level transitions. |
| 36 | $\overline{DS}$ | I | Data Strobe (active Low). This signal provides timing for the transfer of data into and out of the SCC. If $\overline{AS}$ and $\overline{DS}$ coincide, this is interpreted as a reset. |
| 16, 24 | $\overline{DTR/REQA}$, $\overline{DTR/REQB}$ | O | Data Terminal Ready/Request (active Low). These outputs follow the state programmed into the DTR bit. They can also be used as general-purpose outputs or as Request Lines for a DMA controller. |
| 7 | IEI | I | Interrupt Enable In (active High). IEI is used with IEO to form an interrupt daisy chain when there is more than one interrupt-driven device. A High IEI indicates that no other higher priority device has an interrupt under service or is requesting an interrupt. |
| 6 | IEO | O | Interrupt Enable Out (active High). IEO is HIGH only if IEI is HIGH and the CPU is not servicing a SCC interrupt or the SCC is not requesting an interrupt (interrupt acknowledge cycle only). IEO is connected to the next lower priority device's IEI input and thus inhibits interrupts from lower priority devices. |
| 5 | $\overline{INT}$ | O | Interrupt Request (open-drain, active Low). This signal is activated when the SCC requests an interrupt. |
| 8 | $\overline{INTACK}$ | I | Interrupt Acknowledge (active Low). This signal indicates an active interrupt acknowledge cycle. During this cycle, the SCC interrupt daisy chain settles. When $\overline{DS}$ becomes active, the SCC places an interrupt vector on the data bus (if IEI is High). $\overline{INTACK}$ is latched by the rising edge of $\overline{AS}$. |
| 20 | PCLK | I | Clock. This is the master SCC clock used to synchronize internal signals. PCLK is not required to have any phase relationship with the master system clock, although the frequency of this clock must be at least 90% of the CPU clock frequency for a Z8000. PCLK is a TTL level signal. Maximum transmit rate is ¼ PCLK. |
| 13, 27 | RxDA, RxDB | I | Receive Data (active High). These input signals receive serial data at standard TTL levels. |
| 12, 28 | $\overline{RTxCA}$, $\overline{RTxCB}$ | I | Receive/Transmit Clocks (active Low). These pins can be programmed in several different modes of operation. In each channel, RTxC may supply the receive clock, the transmit clock, the clock for the baud-rate generator, or the clock of the digital phase-locked loop. These pins can also be programmed for use with the respective SYNC pins as a crystal oscillator. The receive clock may be 1, 16, 32, or 64 times the data rate in asynchronous modes. |
| 17, 23 | $\overline{RTSA}$, $\overline{RTSB}$ | O | Request to Send (active Low). When the Request to Send RTS bit in Write Register 5 is set, the $\overline{RTS}$ signal goes LOW. When the RTS bit is reset in the asynchronous mode and Auto Enable is on, the signal goes HIGH after the transmitter is empty. In synchronous mode or in asynchronous mode with Auto Enable off, the $\overline{RTS}$ pins strictly follow the state of the RTS bit. Both pins can be used as general-purpose outputs. |
| 34 | R/$\overline{W}$ | I | Read/Write. This signal specifies whether the operation to be performed is read or a write. |
| 11, 29 | $\overline{SYNCA}$, $\overline{SYNCB}$ | I or O | Synchronization (active Low). These pins can act either as inputs, outputs, or part of the crystal oscillator circuit. In the Asynchronous Receive mode (crystal oscillator option not selected), these pins are inputs similar to $\overline{CTS}$ and $\overline{DCD}$. In this mode, transitions on these lines affect the state of the Synchronous/Hunt status bits in Read Register 0 but have no other function.<br>In External Synchronization mode with the crystal oscillator not selected, these lines also act as inputs. In this mode, $\overline{SYNC}$ must be driven LOW two receive clock cycles after the last bit in the synchronous character is received. Character assembly begins on the rising edge of the receive clock immediately preceding the activation of $\overline{SYNC}$.<br>In the Internal Synchronization mode (Monosync and Bisync) with the crystal oscillator not selected, these pins act as outputs and are active only during the part of the receive clock cycle in which synchronous characters are recognized. The synchronous condition is not latched, so these outputs are active each time a synchronous pattern is recognized (regardless of character boundaries). In SDLC mode, these pins act as outputs and are valid on receipt of a flag. |
| 15, 25 | TxDA, TxDB | O | Transmit Data (active High). These output signals transmit serial data at standard TTL levels. |
| 14, 26 | $\overline{TRxCA}$, $\overline{TRxCB}$ | I or O | Transmit/Receive Clocks (active Low). These pins can be programmed in several different modes of operation. $\overline{TRxC}$ may supply the receive clock or the transmit clock in the input mode or supply the output of the digital phase-locked loop, the crystal oscillator, the baud rate generator, or the transmit clock in the output mode. |
| 10, 30 | $\overline{W/REQA}$, $\overline{W/REQB}$ | O | Wait/Request (open-drain when programmed for a Wait function, driven HIGH or LOW when programmed for a Request function). These dual-purpose outputs may be programmed as Request lines for a DMA controller or as Wait lines to synchronize the CPU to the SCC data rate. The reset state is Wait. |

## Z8530(H) PIN DESCRIPTION

| Pin No.* | Name | I/O | Description |
|---|---|---|---|
| 9 | $V_{CC}$ | | +5V Power Supply. |
| 31 | GND | | Ground. |
| 34 | A/$\overline{B}$ | I | Channel A/Channel B Select. This signal selects the channel in which the read or write operation occurs. |
| 33 | $\overline{CE}$ | I | Chip Enable (active Low). This signal selects the SCC for a read or write operation. |
| 18, 22 | $\overline{CTSA}$, $\overline{CTSB}$ | I | Clear To Send (active Low). If these pins are programmed as Auto Enables, a LOW on the inputs enables the respective transmitters. If not programmed as Auto Enables, they may be used as general-purpose inputs. Both inputs are Schmitt-trigger buffered to accommodate slow rise-time inputs. The SCC detects pulses on these inputs and can interrupt the CPU on both logic level transitions. |
| 32 | D/$\overline{C}$ | I | Data/Control Select. This signal defines the type of information transferred to or from the SCC. A HIGH means data is transferred; a LOW indicates a command. |
| 19, 21 | $\overline{DCDA}$, $\overline{DCDB}$ | I | Data Carrier Detect (active Low). These pins function as receiver enables if they are programmed for Auto Enables; otherwise, they may be used as general-purpose input pins. Both pins are Schmitt-trigger buffered to accommodate slow rise-time signals. The SCC detects pulses on these pins and can interrupt the CPU on both logic level transitions. |
| 40, 1, 39, 2, 38, 3, 37, 4 | $D_0$-$D_7$ | I/O | Data Bus (3-state). These lines carry data and commands to and from the SCC. |
| 16, 24 | $\overline{DTR}$/$\overline{REQA}$, $\overline{DTR}$/$\overline{REQB}$ | O | Data Terminal Ready/Request (active Low). These outputs follow the state programmed into the DTR bit. They can also be used as general-purpose outputs or as Request lines for a DMA controller. |
| 7 | IEI | I | Interrupt Enable In (active High). IEI is used with IEO to form an interrupt daisy chain when there is more than one interrupt-driven device. A High IEI indicates that no other higher priority device has an interrupt under service or is requesting an interrupt. |
| 6 | IEO | O | Interrupt Enable Out (active High). IEO is HIGH only if IEI is HIGH and the CPU is not servicing an SCC interrupt or the SCC is not requesting an interrupt (Interrupt Acknowledge cycle only). IEO is connected to the next lower priority device's IEI input and thus inhibits interrupts from lower priority devices. |
| 5 | $\overline{INT}$ | O | Interrupt Request (open-drain, active Low). This signal is activated when the SCC requests an interrupt. |
| 8 | $\overline{INTACK}$ | I | Interrupt Acknowledge (active Low). This signal indicates an active Interrupt Acknowledge cycle. During this cycle, the SCC interrupt daisy chain settles. When $\overline{RD}$ becomes active, the SCC places an interrupt vector on the data bus (if IEI is HIGH). $\overline{INTACK}$ is latched by the rising edge of PCLK. |
| 20 | PCLK | I | Clock. This is the master SCC clock used to synchronize internal signals; PCLK is a TTL level signal. |
| 36 | $\overline{RD}$ | I | Read (active Low). This signal indicates a read operation and, when the SCC is selected, enables the SCC's bus drivers. During the Interrupt Acknowledge cycle, this signal gates the interrupt vector onto the bus if the SCC is the highest priority device requesting an interrupt. |
| 13, 27 | RxDA, RxDB | I | Receive Data (active High). These input signals receive serial data at standard TTL levels. |
| 12, 28 | $\overline{RTxCA}$, $\overline{RTxCB}$ | I | Receive/Transmit Clocks (active Low). These pins can be programmed in several different modes of operation. In each channel, $\overline{RTxC}$ may supply the receive clock, the transmit clock, the clock for the baud rate generator, or the clock for the Digital Phase-Locked Loop. These pins can also be programmed for use with the respective $\overline{SYNC}$ pins as a crystal oscillator. The receive clock may be 1, 16, 32, or 64 times the data rate in asynchronous modes. |
| 17, 23 | $\overline{RTSA}$, $\overline{RTSB}$ | O | Request To Send (active Low). When the Request to Send (RTS) bit in Write Register 5 is set, the $\overline{RTS}$ signal goes LOW. When the RTS bit is reset in the asynchronous mode and Auto Enable is on, the signal goes HIGH after the transmitter is empty. In synchronous mode or in asynchronous mode with Auto Enable off, the $\overline{RTS}$ pin strictly follows the state of the RTS bit. Both pins can be used as general-purpose outputs. |
| 11, 29 | $\overline{SYNCA}$, $\overline{SYNCB}$ | I or O | Synchronization (active Low). These pins can act either as inputs, outputs, or part of the crystal oscillator circuit. In the Asynchronous Receive mode (crystal oscillator option not selected), these pins are inputs similar to $\overline{CTS}$ and $\overline{DCD}$. In this mode, transitions on these lines affect the state of the Synchronous/Hunt status bits in Read Register 0 but have no other function.<br>In External Synchronization mode with the crystal oscillator not selected, these lines also act as inputs. In this mode, $\overline{SYNC}$ must be driven LOW two receive clock cycles after the last bit in the synchronous character is received. Character assembly begins on the rising edge of the receive clock immediately preceding the activation of $\overline{SYNC}$.<br>In the Internal Synchronizaton mode (Monosync and Bisync) with the crystal oscillator not selected, these pins act as outputs and are active only during the part of the receive clock cycle in which synchronous characters are recognized. The synchronous condition is not latched, so these outputs are active each time a synchronization pattern is recognized (regardless of character boundaries). In SDLC mode, these pins act as outputs and are valid on receipt of a flag. |
| 15, 25 | TxDA, TxDB | O | Transmit Data (active High). These output signals transmit serial data at standard TTL levels. |
| 14, 26 | $\overline{TRxCA}$, $\overline{TRxCB}$ | I or O | Transmit/Receive Clocks (active Low). These pins can be programmed in several different modes of operation. $\overline{TRxC}$ may supply the receive clock or the transmit clock in the input mode or supply the output of the Digital Phase-Locked Loop, the crystal oscillator, the baud rate generator, or the transmit clock in the output mode. |
| 35 | $\overline{WR}$ | I | Write (active Low). When the SCC is selected, this signal indicates a write operation. The coincidence of $\overline{RD}$ and $\overline{WR}$ is interpreted as a reset. |
| 10, 30 | $\overline{W}$/$\overline{REQA}$, $\overline{W}$/$\overline{REQB}$ | O | Wait/Request (open-drain when programmed for a Wait function, driven HIGH or LOW when programmed for a Request function). These dual-purpose outputs may be programmed as Request lines for a DMA controller or as Wait lines to synchronize the CPU to the SCC data rate. The reset state is Wait. |

*Pin numbers correspond to DIPs only.

## ARCHITECTURE

The SCC internal structure includes two full-duplex channels, two baud rate generators, internal control and interrupt logic, and a bus interface to the Z8000 CPU (Z8030) or to a non-multiplexed CPU bus (Z8530(H)). Associated with each channel are a number of read and write registers for mode control and status information, as well as logic necessary to interface with modems or other external devices (Figure 1).

The logic for both channels provides formats, synchronization, and validation for data transferred to and from the channel interface. The modem control inputs are monitored by the control logic under program control. All of the modem control signals are general-purpose in nature and can optionally be used for functions other than modem control.

The register set for each channel includes ten control (write) registers, two synchronous character (write) registers, and four status (read) registers. In addition, each baud rate generator has two (read/write) registers for holding the time constant that determines the baud rate. Finally, associated with the interrupt logic is a write register for the interrupt vector accessible through either channel, a write-only Master Interrupt Control register and three read registers: one containing the vector with status information (Channel B only), one containing the vector without status (A only), and one containing the Interrupt Pending bits (A only).

The registers for each channel are designated as follows:

WR0 – WR15 – Write Registers 0 through 15.
RR0 – RR3, RR10, RR12, RR13, RR15 – Read Registers 0 through 3, 10, 12, 13, 15.

The following table lists the functions assigned to each read or write register. The SCC contains only one WR2 and WR9, but they can be accessed by either channel. All other registers are paired (one for each channel).

### Data Path

The transmit and receive data path illustrated in Figure 2 is identical for both channels. The receiver has three 8-bit buffer registers in a FIFO arrangement, in addition to the 8-bit receive shift register. This scheme creates additional time for the CPU to service an interrupt at the beginning of a block of high-speed data. Incoming data is routed through one of several paths (data or CRC) depending on the selected mode (the character length in asynchronous modes also determines the data path).

The transmitter has an 8-bit transmit data buffer register loaded from the internal data bus and a 20-bit transmit shift register that can be loaded either from the sync-character registers or from the transmit data register. Depending on the operational mode, outgoing data is routed through one of four main paths before it is transmitted from the Transmit Data output (TxD).

**TABLE 1. READ AND WRITE REGISTER FUNCTIONS**

**READ REGISTER FUNCTIONS**

**RR0** Transmit/Receive buffer status and External status

**RR1** Special Receive Condition status

**RR2** Modified interrupt vector (Channel B only)
Unmodified interrupt vector (Channel A only)

**RR3** Interrupt Pending bits (Channel A only)

**RR8** Receive buffer

**RR10** Miscellaneous status

**RR12** Lower byte of baud rate generator time constant

**RR13** Upper byte of baud rate generator time constant

**RR15** External/Status interrupt information

**WRITE REGISTER FUNCTIONS**

**WR0** CRC initialize, initialization commands for the various modes, shift right/shift left command

**WR1** Transmit/Receive interrupt and data transfer mode definition

**WR2** Interrupt vector (accessed through either channel)

**WR3** Receive parameters and control

**WR4** Transmit/Receive miscellaneous parameters and modes

**WR5** Transmit parameters and controls

**WR6** Sync characters or SDLC address field

**WR7** Sync character or SDLC flag

**WR8** Transmit buffer

**WR9** Master interrupt control and reset (accessed through either channel)

**WR10** Miscellaneous transmitter/receiver control bits

**WR11** Clock mode control

**WR12** Lower byte of baud rate generator time constant

**WR13** Upper byte of baud rate generator time constant

**WR14** Miscellaneous control bits

**WR15** External/Status interrupt control

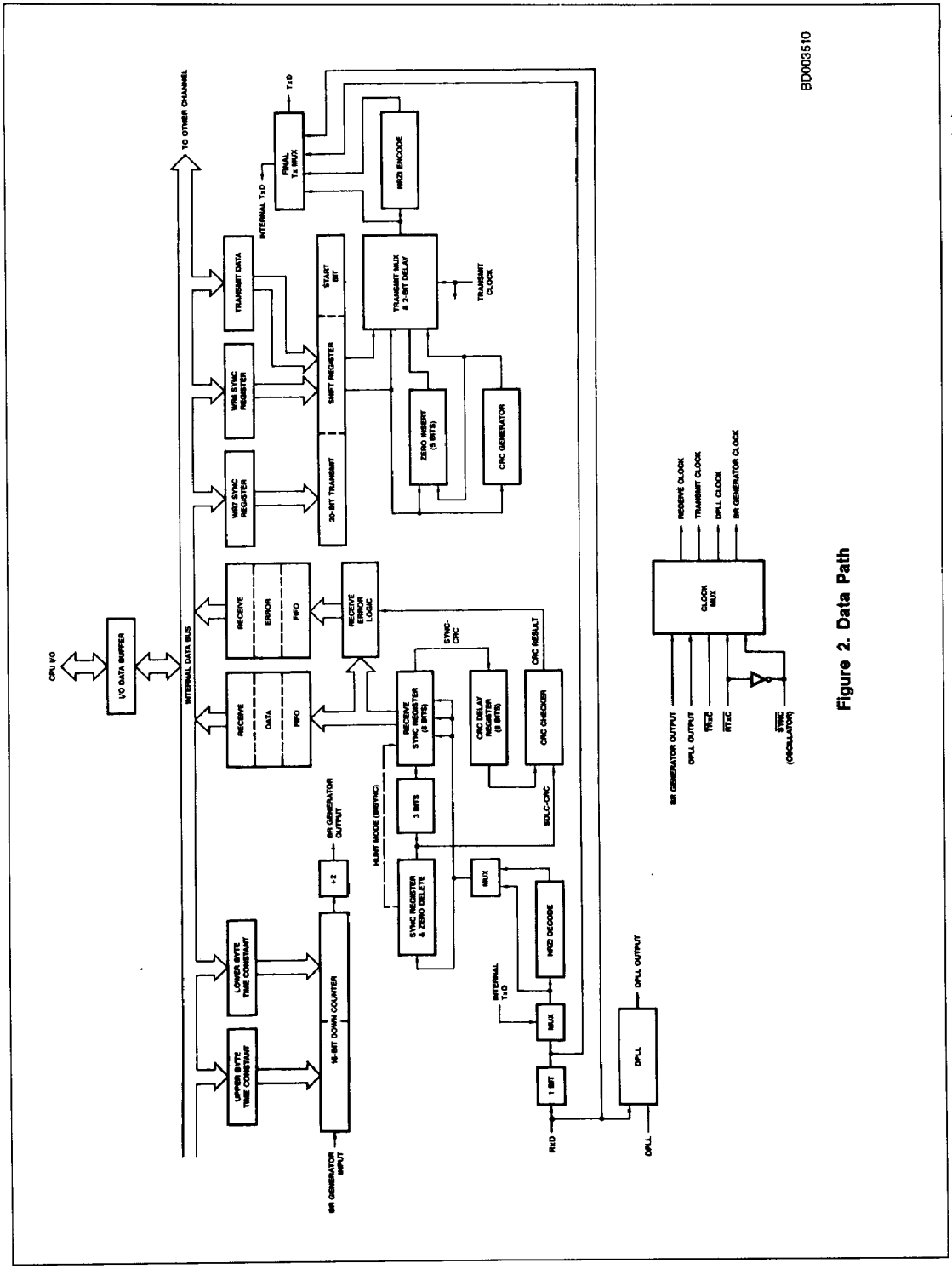



Figure 2. Data Path

## DETAILED DESCRIPTION

The functional capabilities of the SCC can be described from two different points of view: as a data communications device, it transmits and receives data in a wide variety of data communications protocols; as a microprocessor peripheral, it interacts with the CPU and provides vectored interrupts and handshaking signals.

### Data Communications Capabilities

The SCC provides two independent full-duplex channels programmable for use in any common asynchronous or synchronous data-communication protocol. Figure 3 and the following description briefly detail these protocols.

### Asynchronous Modes

Transmission and reception can be accomplished independently on each channel with five to eight bits per character, plus optional even or odd parity. The transmitters can supply one, one-and-a-half or two stop bits per character and can provide a break output at any time. The receiver break-detection logic interrupts the CPU both at the start and at the end of a received break. Reception is protected from spikes by a transient spike-rejection mechanism that checks the signal one-half a bit time after a Low level is detected on the receive data input (RxDA or RxDB in the Z8530(H) Logic Symbol). If the LOW does not persist (as in the case of a transient), the character assembly process does not start.

Framing errors and overrun errors are detected and buffered together with the partial character on which they occur. Vectored interrupts allow fast servicing or error conditions using dedicated routines. Furthermore, a built-in checking process avoids the interpretation of framing error as a new start bit: a framing error results in the addition of one-half a bit time to the point at which the search for the next start bit begins.

The SCC does not require symmetric transmit and receive clock signals – a feature allowing use of the wide variety of clock sources. The transmitter and receiver can handle data at a rate of 1, 1/16, 1/32, or 1/64 of the clock rate supplied to the receive and transmit clock inputs. In asynchronous modes, the SYNC pin may be programmed as an input used for functions, such as monitoring a ring indicator.

### Synchronous Modes

The SCC supports both byte-oriented and bit-oriented synchronous communication. Synchronous byte-oriented protocols can be handled in several modes, allowing character synchronization with a 6-bit or 8-bit synchronous character (Monosync), any 12-bit synchronous pattern (Bisync), or with an external synchronous signal. Leading synchronous characters can be removed without interrupting the CPU.

5- or 7-bit synchronous characters are detected with 8- or 16-bit patterns in the SCC by overlapping the larger pattern across multiple incoming synchronous characters as shown in Figure 4.

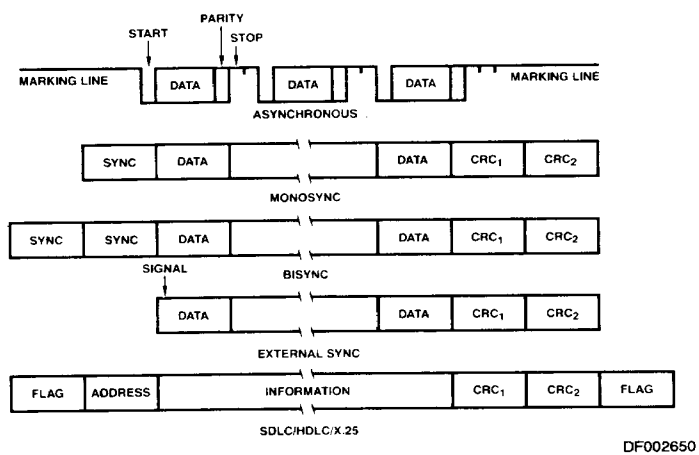



**Figure 3. SCC Protocols**

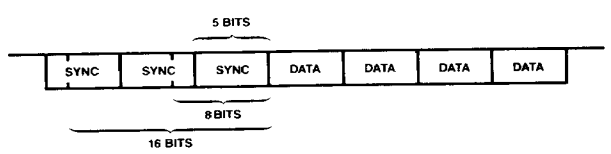



**Figure 4. Detecting 5- or 7-Bit Synchronous Characters**

CRC checking for Synchronous byte-oriented modes is delayed by one character time so that the CPU may disable CRC checking on specific characters. This permits the implementation of protocols, such as IBM Bisync.

Both CRC-16 ($X^{16} + X^{15} + X^2 + 1$) and CCITT ($X^{16} + X^{12} + X^5 + 1$) error checking polynomials are supported. Either polynomial may be selected in all synchronous modes. Users may preset the CRC generator and checker to all 1s or all 0s. The SCC also provides a feature that automatically transmits CRC data when no other data is available for transmission. This allows for high-speed transmissions under DMA control with no need for CPU intervention at the end of a message. When there is no data or CRC to send in synchronous modes, the transmitter inserts 6-, 8-, or 16-bit synchronous characters, regardless of the programmed character length.

The SCC supports synchronous bit-oriented protocols, such as SDLC and HDLC, by performing automatic flag sending, zero insertion, and CRC generation. A special command can be used to abort a frame in transmission. At the end of a message, the SCC automatically transmits the CRC and trailing flag when the transmitter underruns. The transmitter may also be programmed to send an idle line consisting of continuous flag characters or a steady marking condition.

If a transmit underrun occurs in the middle of a message, an external/status interrupt warns the CPU of this status change so that an abort may be issued. The SCC may also be programmed to send an abort itself in case of an underrun, relieving the CPU of this task. One to eight bits per character can be sent allowing reception of a message with no prior information about the character structure in the information field of a frame.

The receiver automatically acquires synchronization on the leading flag of a frame in SDLC or HDLC and provides a synchronization signal on the $\overline{SYNC}$ pin (an interrupt can also be programmed). The receiver can be programmed to search for frames addressed by a single byte (or four bits within a byte) of a user-selected address or to a global broadcast address. In this mode, frames not matching either the user-selected or broadcast address are ignored. The number of address bytes can be extended under software control. For receiving data, an interrupt on the first received character, or an interrupt on every character, or on special condition only (end-of-frame) can be selected. The receiver automatically deletes all 0s inserted by the transmitter during character assembly. CRC is also calculated and is automatically checked to validate frame transmission. At the end of transmission, the status of a received frame is available in the status registers. In SDLC mode, the SCC must be programmed to use the SDLC CRC polynomial, but the generator and checker may be preset to all 1s or all 0s. The CRC is inverted before transmission and the receiver checks against the bit pattern 0001110100001111.

NRZ, NRZI or FM coding may be used in any 1X mode. The parity options available in asynchronous modes are available in synchronous modes.

The SCC can be conveniently used under DMA control to provide high-speed reception or transmission. In reception, for example, the SCC can interrupt the CPU when the first character of a message is received. The CPU then enables the DMA to transfer the message to memory. The SCC then issues an end-of-frame interrupt and the CPU can check the status of the received message. Thus, the CPU is freed for other service while the message is being received. The CPU may also enable the DMA first and have the SCC interrupt only on end-of-frame. This procedure allows all data to be transferred via the DMA.

## SDLC LOOP MODE

The SCC supports SDLC Loop mode in addition to normal SDLC. In an SDLC Loop, there is a primary controller station that manages the message traffic flow and any number of secondary stations. In SDLC Loop mode, the SCC performs the functions of a secondary station while an SCC operating in regular SDLC mode can act as a controller (Figure 5).

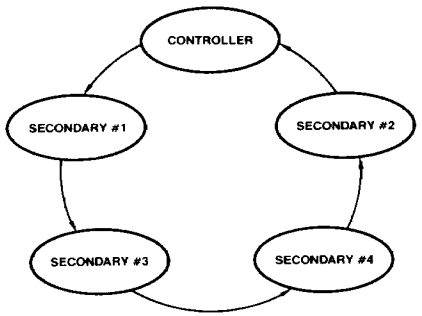



**Figure 5. An SDLC Loop**

A secondary station in an SDLC Loop is always listening to the messages being sent around the loop and, in fact, must pass these messages to the rest of the loop by retransmitting them with a one-bit-time delay. The secondary station can place its own message on the loop only at specific times. The controller signals that secondary stations may transmit messages by sending a special character, called an EOP (End of Poll), around the loop. The EOP character is the bit pattern 11111110. Because of zero insertion during messages, this bit pattern is unique and easily recognized.

When a secondary station has a message to transmit and recognizes an EOP on the line, it changes the last binary one of the EOP to a zero before transmission. This has the effect of turning the EOP into a flag sequence. The secondary station now places its message on the loop and terminates the message with an EOP. Any secondary stations further down the loop with messages to transmit can then append their messages to the message of the first secondary station by the same process. Any secondary stations without messages to send merely echo the incoming messages and are prohibited from placing messages on the loop (except upon recognizing an EOP).

SDLC Loop mode is a programmable option in the SCC. NRZ, NRZI, and FM coding may all be used in SDLC Loop mode.

### Baud Rate Generator

Each channel in the SCC contains a programmable baud rate generator. Each generator consists of two 8-bit time constant registers that form a 16-bit time constant, a 16-bit down counter, and a flip-flop on the output producing a square wave. On start-up, the flip-flop on the output is set in a High state; the value in the time constant register is loaded into the counter; and the counter starts counting down. The output of the baud rate generator toggles upon reaching zero; the value in the time constant register is loaded into the counter; and the process is repeated. The time constant may be changed at any time, but the new value does not take effect until the next load of the counter.

The output of the baud rate generator may be used as either the transmit clock, the receive clock, or both. It can also drive the digital phase-locked loop (see next section).

If the receive clock or transmit clock is not programmed to come from the $\overline{TRxC}$ pin, the output of the baud rate generator may be echoed out via the $\overline{TRxC}$ pin.

The following formula relates the time constant to the baud rate. (The baud rate is in bits/second and the BR clock period is in seconds.)

$$\text{baud rate} = \frac{1}{2\ (\text{time constant} + 2) \times (\text{BR clock period})}$$

**Time-Constant Values for Standard Baud Rates at BR Clock = 3.9936MHz**

| Rate (Baud) | Time Constant (decimal notation) | Error |
|---|---|---|
| 19200 | 102 | – |
| 9600 | 206 | – |
| 7200 | 275 | 0.12% |
| 4800 | 414 | – |
| 3600 | 553 | 0.06% |
| 2400 | 830 | – |
| 2000 | 996 | 0.04% |
| 1800 | 1107 | 0.03% |
| 1200 | 1662 | – |
| 600 | 3326 | – |
| 300 | 6654 | – |
| 150 | 13310 | – |
| 134.5 | 14844 | 0.0007% |
| 110 | 18151 | 0.0015% |
| 75 | 26622 | – |
| 50 | 39934 | – |

## Digital Phase-Locked Loop

The SCC contains a digital phase-locked loop (DPLL) to recover clock information from a data stream with NRZI or FM encoding. The DPLL is driven by a clock that is nominally 32 (NRZI) or 16 (FM) times the data rate. The DPLL uses this clock, along with the data stream, to construct a clock for the data. This clock may then be used as the SCC receive clock, the transmit clock, or both.

For NRZI encoding, the DPLL counts the 32X clock to create nominal bit times. As the 32X clock is counted, the DPLL is searching the incoming data stream for edges (either 1/0 or 0/1). Whenever an edge is detected, the DPLL makes a count adjustment (during the next counting cycle), producing a terminal count closer to the center of the bit cell.

For FM encoding, the DPLL still counts from 0 to 31, but with a cycle corresponding to two bit times. When the DPLL is locked, the clock edges in the data stream should occur between counts 15 and 16 and between counts 31 and 0. The DPLL looks for edges only during a time centered on the 15/16 counting transition.

The 32X clock for the DPLL can be programmed to come from either the RTxC input or the output of the baud rate generator. The DPLL output may be programmed to be echoed out of the SCC via the $\overline{TRxC}$ pin (if this pin is not being used as an input).

## Data Encoding

The SCC may be programmed to encode and decode the serial data in four different ways (Figure 6). In NRZ encoding, a 1 is represented by a High level, and a 0 is represented by a Low level. In NRZI encoding, a 1 is represented by no change in level, and a 0 is represented by a change in level. In $FM_1$ (more properly, bi-phase mark), a transition occurs at the beginning of every bit cell. A 1 is represented by an additional transition at the center of the bit cell, and a 0 is represented by no additional transition at the center of the bit cell. In $FM_0$ (bi-phase space), a transition occurs at the beginning of every bit cell. A 0 is represented by an additional transition at the center of the bit cell, and a 1 is represented by no additional transition at the center of the bit cell. In addition to these four methods, the SCC can be used to decode Manchester (bi-phase level) data by using the DPLL in the FM mode and programming the receiver for NRZ data. Manchester encoding always produces a transition at the center of the bit cell. If the transition is 0/1, the bit is a 0. If the transition is 1/0, the bit is a 1.

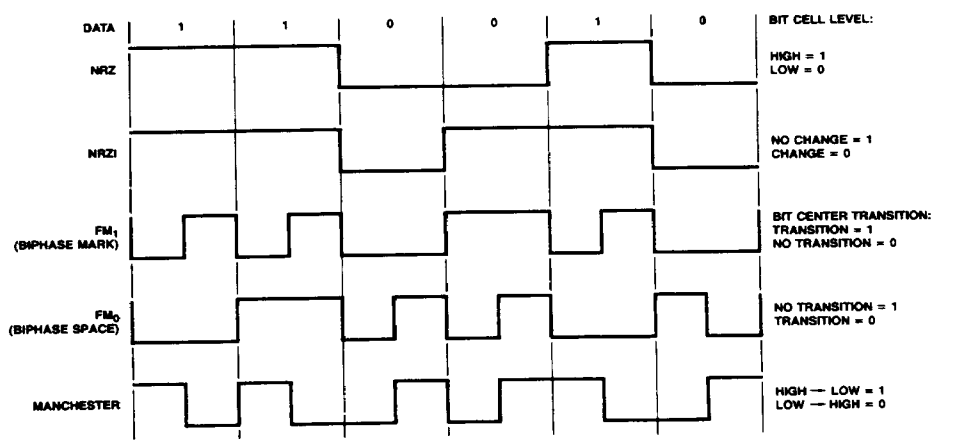



**Figure 6. Data Encoding Methods**

### Auto Echo and Local Loopback

The SCC is capable of automatically echoing everything it receives. This feature is useful mainly in asynchronous modes but works in synchronous and SDLC modes as well. In Auto Echo mode, TxD is RxD. Auto Echo mode can be used with NRZI or FM encoding with no additional delay, because the data stream is not decoded before retransmission. In Auto Echo mode, the $\overline{CTS}$ input is ignored as a transmitter enable (although transitions on this input can still cause interrupts if programmed to do so). In this mode, the transmitter is actually bypassed, and the programmer is responsible for disabling transmitter interrupts and $\overline{WAIT}/\overline{REQUEST}$ on transmit.

The SCC is also capable of local loopback. In this mode, TxD is RxD just as in Auto Echo mode. However, in Local Loopback mode, the internal transmit data is tied to the internal receive data, and RxD is ignored (except to be echoed out via TxD). The CTS and DCD inputs are also ignored as transmit and receive enables. However, transitions on these inputs can still cause interrupts. Local Loopback works in asynchronous, synchronous and SDLC modes with NRZ, NRZI or FM coding of the data stream.

### I/O Interface Capabilities

The SCC offers the choice of Polling, Interrupt (vectored or nonvectored), and Block Transfer modes to transfer data, status, and control information to and from the CPU. The Block Transfer mode can be implemented under CPU or DMA control.

### Polling

All interrupts are disabled. Three status registers in the SCC are automatically updated whenever any function is performed. For example, end-of-frame in SDLC mode sets a bit in one of these status registers. The idea behind polling is for the CPU to periodically read a status register until the register contents indicate the need for data to be transferred. Only one register needs to be read; depending on its contents, the CPU either writes data, reads data, or continues. Two bits in the register indicate the need for data transfer. An alternative is a poll of the Interrupt Pending register to determine the source of an interrupt. The status for both channels resides in one register.

### Interrupts

When a SCC responds to an Interrupt Acknowledge signal ($\overline{INTACK}$) from the CPU, an interrupt vector may be placed on the data bus. This vector is written in WR2 and may be read in RR2A or RR2B (Figures 8 and 9).

To speed interrupt response time, the SCC can modify three bits in this vector to indicate status. If the vector is read in Channel A, status is never included; if it is read in Channel B, status is always included.

Each of the six sources of interrupts in the SCC (Transmit, Receive and External/Status interrupts in both channels) has three bits associated with the interrupt source: Interrupt Pending (IP), Interrupt Under Service (IUS), and Interrupt Enable (IE). Operation of the IE bit is straightforward. If the IE bit is set for a given interrupt source, then that source can request interrupts. The exception is when the MIE (Master Interrupt Enable) bit in WR9 is reset and no interrupts may be requested. The IE bits are write-only.

The other two bits are related to the Z-Bus interrupt priority chain (Figure 7). As a Z-Bus peripheral, the SCC may request an interrupt only when no higher priority device is requesting one; e.g., when IEI is HIGH. If the device in question requests an interrupt, it pulls down $\overline{INT}$. The CPU then responds with $\overline{INTACK}$, and the interrupting device places the vector on the A/D bus.

In the SCC, the IP bit signals a need for interrupt servicing. When an IP bit is 1 and the IEI input is HIGH, the INT output is pulled LOW, requesting an interrupt. In the SCC, if the IE bit is not set by enabling interrupts, then the IP for that source can never be set. The IP bits are readable in RR3A.

The IUS bits signal that an interrupt request is being serviced. If an IUS is set, all interrupt sources of lower priority in the SCC and external to the SCC are prevented from requesting interrupts. The internal interrupt sources are inhibited by the state of the internal daisy chain, while lower priority devices are inhibited by the IEO output of the SCC being pulled LOW and propagated to subsequent peripherals. An IUS bit is set during an Interrupt Acknowledge cycle if there are no higher priority devices requesting interrupts.

There are three types of interrupts: Transmit, Receive and External/Status. Each interrupt type is enabled under program control with Channel A having higher priority than Channel B, and with Receive, Transmit and External/Status interrupts prioritized in that order within each channel. When the Transmit interrupt is enabled, the CPU is interrupted when the transmit buffer becomes empty. (This implies that the transmitter must have had a data character written into it so that it can become empty.) When enabled, the Receive can interrupt the CPU in one of three ways:

- Interrupt on First Receive Character or Special Receive condition.
- Interrupt on all Receive Characters or Special Receive condition.
- Interrupt on Special Receive condition only.

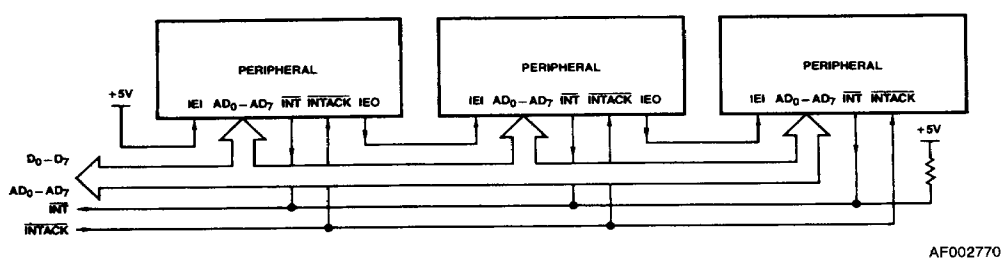



**Figure 7. Z-Bus Interrupt Schedule**

Interrupt on First Character or Special Condition and Interrupt on Special Condition Only are typically used with the Block Transfer mode. A Special Receive Condition is one of the following: receiver overrun, framing error in asynchronous mode, End-of-Frame in SDLC mode, and optionally, a parity error. The Special Receive Condition interrupt is different from an ordinary receive character available interrupt only in the status placed in the vector during the Interrupt Acknowledge cycle. In Interrupt on First Receive Character, an interrupt can occur from Special Receive conditions any time after the first receive character interrupt.

The main function of the External/Status interrupt is to monitor the signal transitions of the $\overline{CTS}$, $\overline{DCD}$, and $\overline{SYNC}$ pins; however, an External/Status interrupt is also caused by a Transmit Underrun condition, a zero count in the baud rate generator, the detection of a Break (asynchronous mode), Abort (SDLC mode) or EOP (SDLC Loop mode) sequence in the data stream. The interrupt caused by the Abort or EOP has a special feature allowing the SCC to interrupt when the Abort or EOP sequence is detected or terminated. This feature facilitates the proper termination of the current message, correct initialization of the next message, and the accurate timing of the Abort condition in external logic in SDLC mode. In SDLC Loop mode, this feature allows secondary stations to recognize the wishes of the primary station to regain control of the loop during a poll sequence.

### CPU/DMA Block Transfer

The SCC provides a Block Transfer mode to accommodate CPU block transfer functions and DMA controllers. The Block Transfer mode uses the $\overline{WAIT}/\overline{Request}$ output in conjunction with the Wait/Request bits in WR1. The $\overline{WAIT}/\overline{REQUEST}$ output can be defined under software control as a $\overline{WAIT}$ line in the CPU Block Transfer mode or as a $\overline{REQUEST}$ line in the DMA Block Transfer mode.

To a DMA controller, the SCC $\overline{REQUEST}$ output indicates that the SCC is ready to transfer data to or from memory. To the CPU, the $\overline{WAIT}$ line indicates that the SCC is not ready to transfer data, thereby requesting that the CPU extend the I/O cycle. The $\overline{DTR}/\overline{REQUEST}$ line allows full-duplex operation under DMA control.

## PROGRAMMING INFORMATION

Each channel has fifteen Write registers that are individually programmed from the system bus to configure the functional personality of each channel. Each channel also has eight Read registers from which the system can read Status, Baud rate, or Interrupt information.

The Z8030 and Z8530(H) differ in the way the system accesses these registers:

In the Z8030 all registers are directly addressable from the multiplexed Address Data bus. See Figure 10 and Figure 11 for timing. The Z8030 can operate in either of two modes: when bit 0 in Write Register 0 is reset (or after initialization with a hardware reset), Address lines $AD_1$ through $AD_5$ select the register to be read from or written into during Data Strobe $\overline{DS}$. (This is called left shift and is the natural Z8000 mode.) When bit 0 in Write Register 0 is set, Address lines $AD_0$ through $AD_4$ select the register to be read from or written into. (This is called right shift and is more natural for interfacing with other microprocessors.)

Table 2 describes the register addressing for both modes.

Channel A/Channel B selection is made either by $AD_0$ or by $AD_5$.

If Bit $D_0$ in WR0 is reset (or after hardware reset):
$AD_5$ selects the channel (0 = B, 1 = A)
(this is called "Select Shift Left Mode").

If Bits $D_0$ and $D_1$ in WR0 are set:
$AD_0$ selects the channel (0 = B, 1 = A)
(this is called "Select Shift Right Mode).

In the Z8530(H) only the four data registers (Read and Write for Channels A and B) are directly selected by a HIGH on the D/$\overline{C}$ input and the appropriate levels on the $\overline{RD}$, $\overline{WR}$ and A/$\overline{B}$ pins. All other registers are addressed indirectly by the content of Write Register 0 in conjunction with a LOW on the D/$\overline{C}$ input and the appropriate levels on the $\overline{RD}$, $\overline{WR}$ and A/$\overline{B}$ pins. If bit D3 in WR0 is 1 and bits 5 and 6 are 0, then bits 0, 1, 2 address the higher registers 8 through 15. If bits 4, 5, 6 contain a different code, bits 0, 1, 2 address the lower registers 0 through 7 as shown in Table 3.

**TABLE 2. REGISTER ADDRESSING (Z8030 ONLY)**

| $AD_4$ | $AD_3$ | $AD_2$ | $AD_1$ | Write Register | Read Register |
|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 0 | 1 | 1 | 1 |
| 0 | 0 | 1 | 0 | 2 | 2 |
| 0 | 0 | 1 | 1 | 3 | 3 |
| 0 | 1 | 0 | 0 | 4 | (0) |
| 0 | 1 | 0 | 1 | 5 | (1) |
| 0 | 1 | 1 | 0 | 6 | (2) |
| 0 | 1 | 1 | 1 | 7 | (3) |
| 1 | 0 | 0 | 0 | Data | Data |
| 1 | 0 | 0 | 1 | 9 | – |
| 1 | 0 | 1 | 0 | 10 | 10 |
| 1 | 0 | 1 | 1 | 11 | (15) |
| 1 | 1 | 0 | 0 | 12 | 12 |
| 1 | 1 | 0 | 1 | 13 | 13 |
| 1 | 1 | 1 | 0 | 14 | (10) |
| 1 | 1 | 1 | 1 | 15 | 15 |

Writing to or reading from any register except RR0, WR0 and the Data Registers thus involves two operations:

First, write the appropriate code into WR0, then follow this by a write or read operation on the register thus specified. Bits 0 through 4 in WW0 are automatically cleared after this operation, so that WW0 then points to WR0 or RR0 again.

Channel A/Channel B selection is made by the A/$\overline{B}$ input (HIGH = A, LOW = B)

In both Z8030 and Z8530(H), the system program first issues a series of commands to initialize the basic mode of operation. This is followed by other commands to qualify conditions within the selected mode. For example, the asynchronous mode, character length, clock rate, number of stop bits, even or odd parity might be set first. Then the interrupt mode would be set and, finally, receiver or transmitter enable.

**TABLE 3. REGISTER ADDRESSING (Z8530(H) ONLY)**

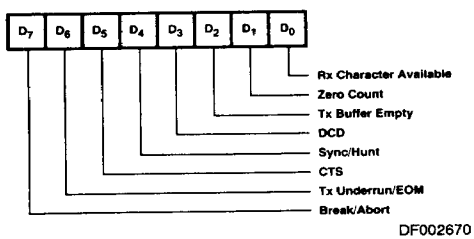
| D/C "Point High" Code in WR0: | | $D_2$ | $D_1$ in WR0: | $D_0$ | Write Register | Read Register |
|---|---|---|---|---|---|---|
| HIGH | Either way | X | X | X | Data | Data |
| LOW | Not true | 0 | 0 | 0 | 0 | 0 |
| LOW | Not true | 0 | 0 | 1 | 1 | 1 |
| LOW | Not true | 0 | 1 | 0 | 2 | 2 |
| LOW | Not true | 0 | 1 | 1 | 3 | 3 |
| LOW | Not true | 1 | 0 | 0 | 4 | (0) |
| LOW | Not true | 1 | 0 | 1 | 5 | (1) |
| LOW | Not true | 1 | 1 | 0 | 6 | (2) |
| LOW | Not true | 1 | 1 | 1 | 7 | (3) |
| LOW | True | 0 | 0 | 0 | Data | Data |
| LOW | True | 0 | 0 | 1 | 9 | – |
| LOW | True | 0 | 1 | 0 | 10 | 10 |
| LOW | True | 0 | 1 | 1 | 11 | (15) |
| LOW | True | 1 | 0 | 0 | 12 | 12 |
| LOW | True | 1 | 0 | 1 | 13 | 13 |
| LOW | True | 1 | 1 | 0 | 14 | (10) |
| LOW | True | 1 | 1 | 1 | 15 | 15 |

## Read Registers

The SCC contains eight read registers (actually nine, counting the receive buffer (RR8) in each channel). Four of these may be read to obtain status information (RR0, RR1, RR10, and RR15). Two registers (RR12 and RR13) may be read to learn the baud rate generator time constant. RR2 contains either the unmodified interrupt vector (Channel A) or the vector modified by status information (Channel B). RR3 contains the Interrupt Pending (IP) bits (Channel A). Figure 8 shows the formats for each read register.

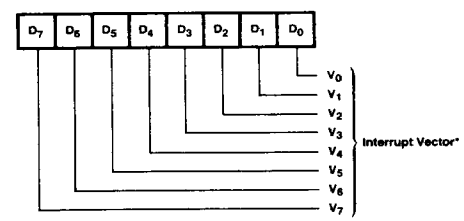
The status bits of RR0 and RR1 are carefully grouped to simplify status monitoring; e.g., when the interrupt vector indicates a Special Receive Condition interrupt, all the appropriate error bits can be read from a single register (RR1).

**Read Register 0**




DF002670

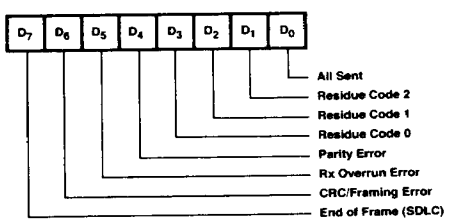
**Read Register 2**




*Modified in B Channel

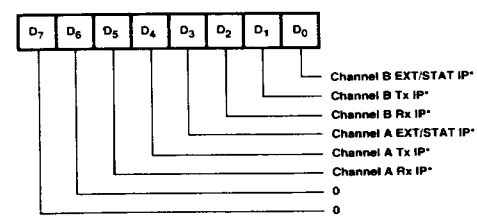
DF002680

**Read Register 1**




DF002690

**Read Register 3**




*Always 0 in B Channel

DF002700

**Figure 8. Read Register Bit Functions**

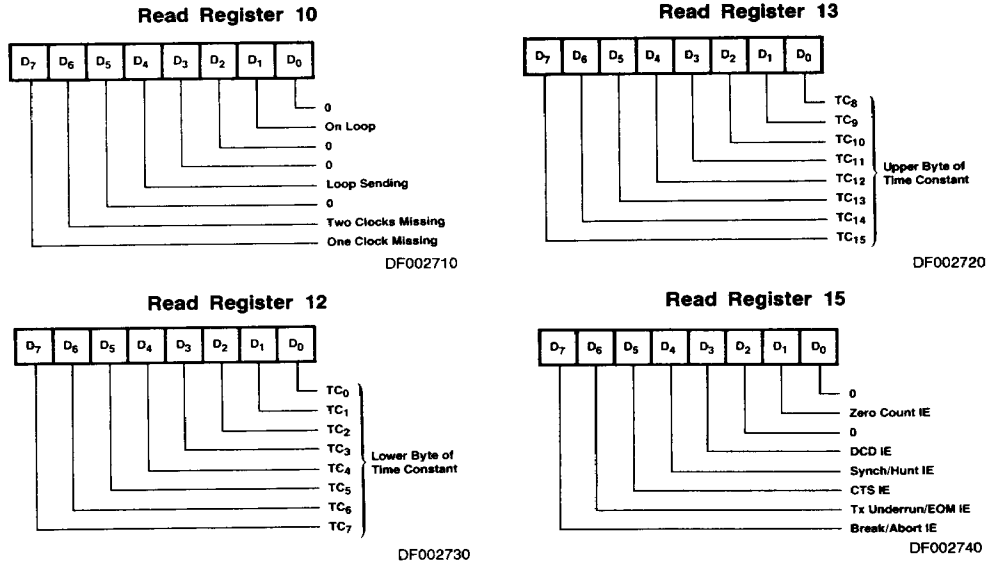



**Figure 8. Read Register Bit Functions (Cont.)**

## Write Registers

The SCC contains 15 write registers (16 counting WR8, the transmit buffer) in each channel. These write registers are programmed separately to configure the functional "personality" of the channels. In addition, there are two registers (WR2 and WR9) shared by the two channels that may be accessed through either of them. WR2 contains the interrupt vector for both channels, while WR9 contains the interrupt control bits. Figure 9 shows the format of each write register.

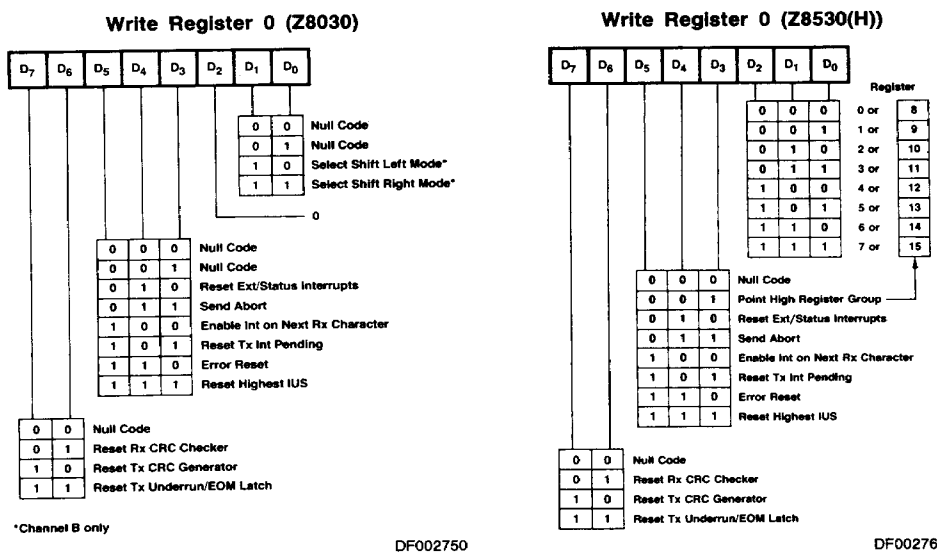
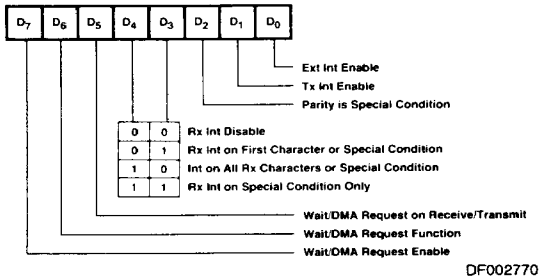


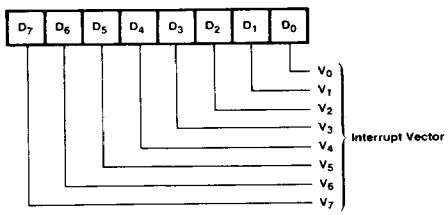

**Figure 9. Write Register Bit Functions**

### Write Register 1



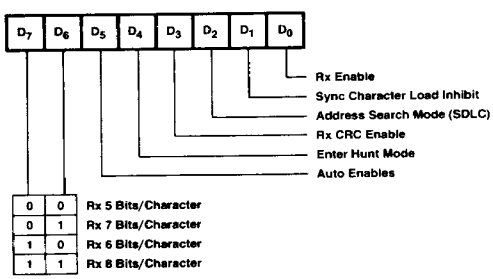

DF002770

### Write Register 2



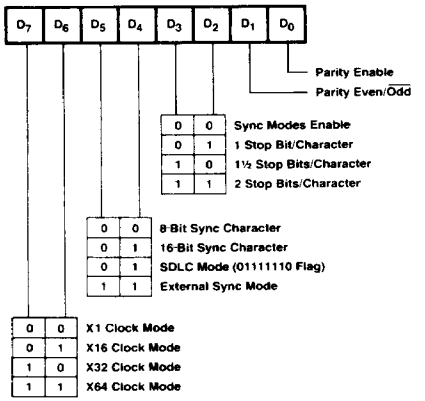

DF002780

### Write Register 3



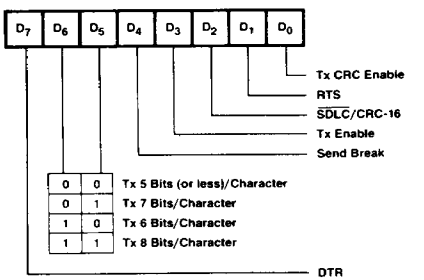

DF002790

### Write Register 4



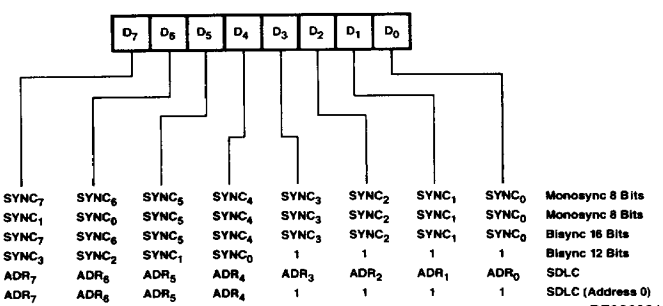

DF002811

### Write Register 5




DF002820

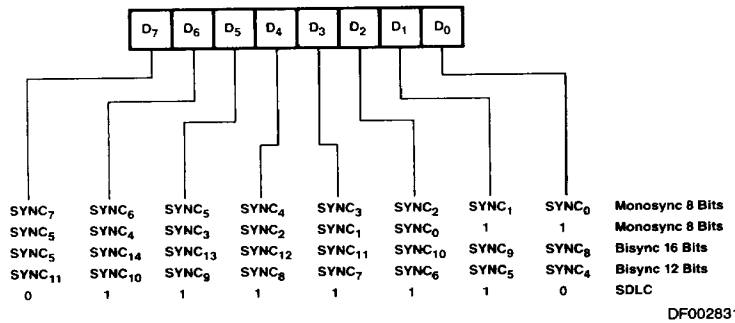
### Write Register 6




DF002801

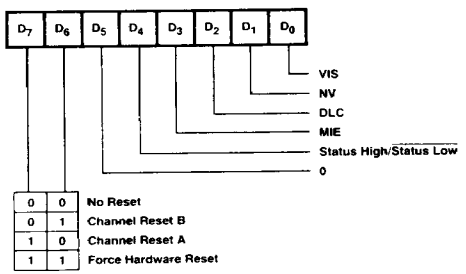
**Figure 9. Write Register Bit Functions (Cont.)**

### Write Register 7



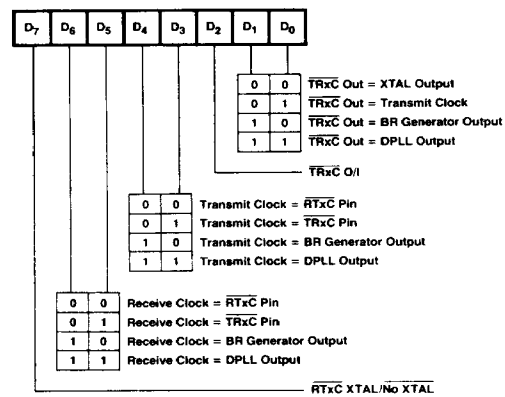

DF002831

### Write Register 9



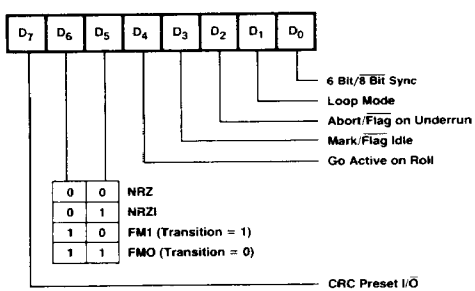

DF002840

### Write Register 11



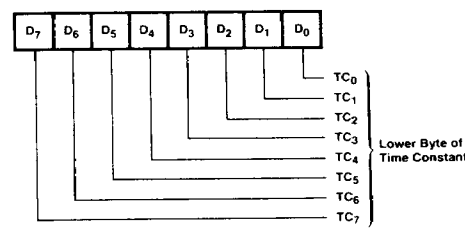

DF002850

### Write Register 10




DF002860

### Write Register 12




DF002870

**Figure 9. Write Register Bit Functions (Cont.)**

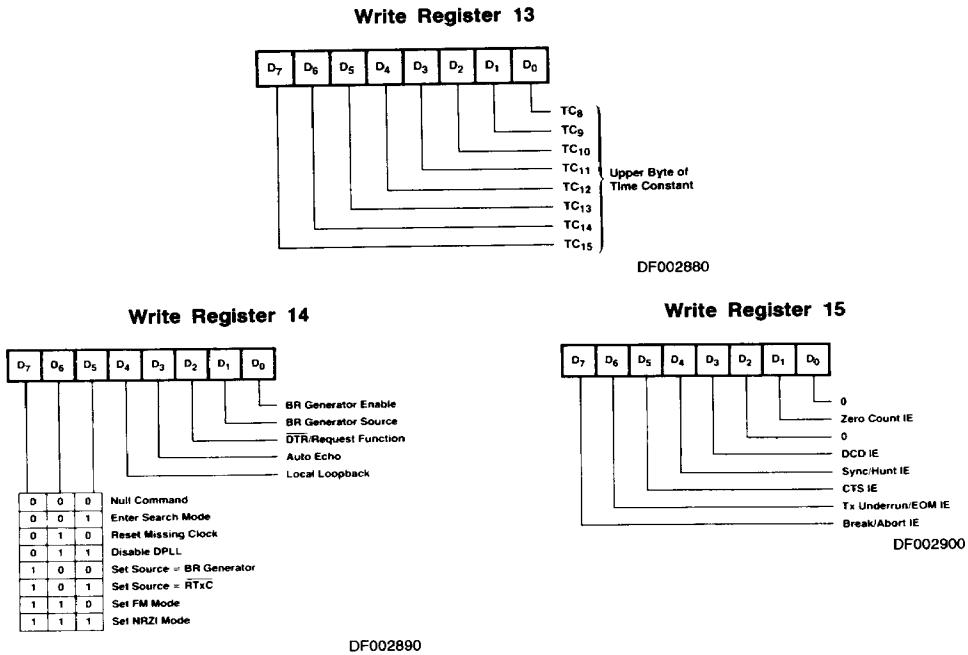



**Figure 9. Write Register Bit Functions (Cont.)**

## Z8030 Timing

The SCC generates internal control signals from $\overline{AS}$ and $\overline{DS}$ that are related to PCLK. Since PCLK has no phase relationship with $\overline{AS}$ and $\overline{DS}$, the circuitry generating these internal control signals must provide time for metastable conditions to disappear. This gives rise to a recovery time related to PCLK. The recovery time applies only between bus transactions involving the SCC to the falling edge of $\overline{DS}$ in the second transaction involving the SCC. This time must be at least 6 PCLK cycles plus 200ns.

## Read Cycle Timing

Figure 10 illustrates read cycle timing. The address on $AD_0 - AD_7$ and the state of $\overline{CS_0}$ and $\overline{INTACK}$ are latched by the rising edge of $\overline{AS}$. R/$\overline{W}$ must be HIGH to indicate a read cycle. $CS_1$ must also be HIGH for the read cycle to occur. The data bus drivers in the SCC are then enabled while $\overline{DS}$ is LOW.

## Write Cycle Timing

Figure 11 illustrates write cycle timing. The address on $AD_0 - AD_7$ and the state of $\overline{CS_0}$ and $\overline{INTACK}$ are latched by the rising edge of $\overline{AS}$. R/$\overline{W}$ must be LOW to indicate a write cycle. $CS_1$ must be HIGH for the write cycle to occur. $\overline{DS}$ Low strobes the data into the SCC.

## Interrupt Acknowledge Cycle Timing

Figure 12 illustrates interrupt acknowledge cycle timing. The address on $AD_0 - AD_7$ and the state of $\overline{CS_0}$ and $\overline{INTACK}$ are latched by the rising edge of $\overline{AS}$. However, if $\overline{INTACK}$ is LOW, the address and $\overline{CS_0}$ are ignored. The state of R/$\overline{W}$ and $CS_1$ are also ignored for the duration of the interrupt acknowledge cycle. Between the rising edge of $\overline{AS}$ and the falling edge of $\overline{DS}$, the internal and external IEI/IEO daisy chains settle. If there is an interrupt pending in the SCC and IEI is HIGH when $\overline{DS}$ falls, the acknowledge cycle was intended for the SCC. In this case, the SCC may be programmed to respond to $\overline{DS}$ Low by placing its interrupt vector on $AD_0 - AD_7$. It then sets the appropriate interrupt-under-service latch internally.

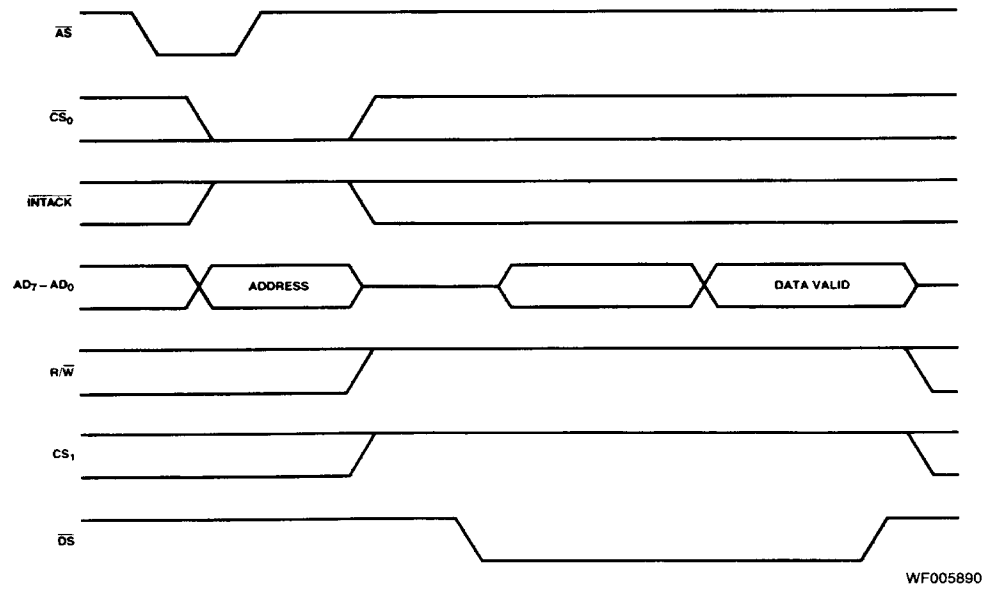



**Figure 10. Read Cycle Timing**

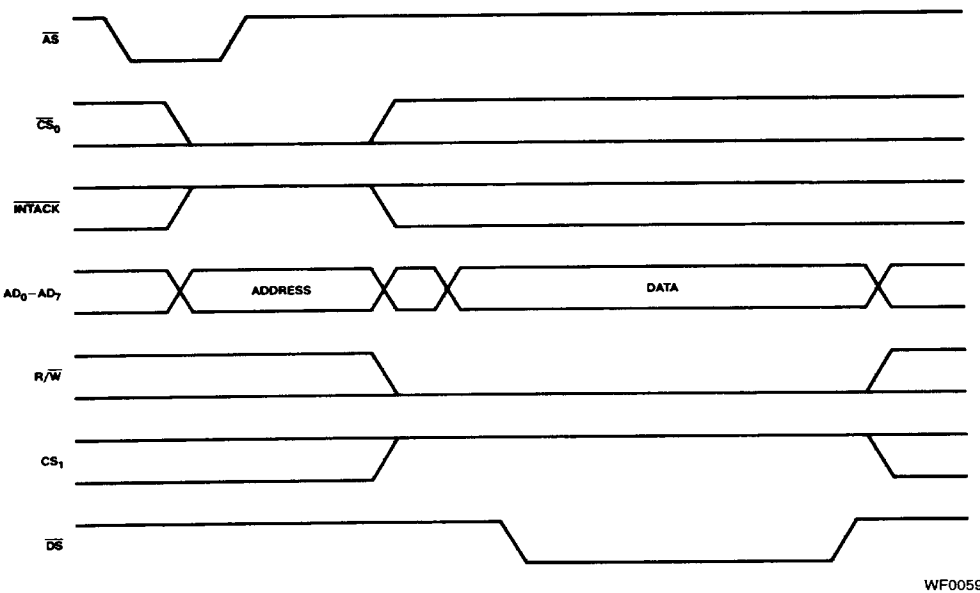



**Figure 11. Write Cycle Timing**

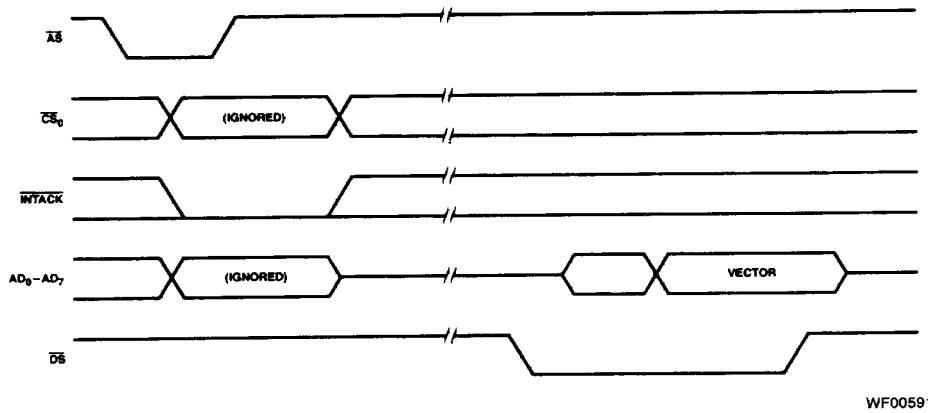



**Figure 12. Interrupt Acknowledge Cycle Timing**

## Z8530(H) Timing

The SCC generates internal control signals from $\overline{WR}$ and $\overline{RD}$ that are related to PCLK. Since PCLK has no phase relationship with $\overline{WR}$ and $\overline{RD}$, the circuitry generating these internal control signals must provide time for metastable conditions to disappear. This gives rise to a recovery time related to PCLK. The recovery time applies only between bus transactions involving the SCC. The recovery time required for proper operation is specified from the rising edge of $\overline{WR}$ or $\overline{RD}$ in the first transaction involving the SCC to the falling edge of $\overline{WR}$ or $\overline{RD}$ in the second transaction involving the SCC. This time must be at least 6 PCLK cycles plus 200ns.

## Read Cycle Timing

Figure 13 illustrates Read cycle timing. Addresses on A/$\overline{B}$ and D/$\overline{C}$ and the status on $\overline{INTACK}$ must remain stable throughout the cycle. If $\overline{CE}$ falls after $\overline{RD}$ falls or if it rises before $\overline{RD}$ rises, the effective $\overline{RD}$ is shortened.

## Write Cycle Timing

Figure 14 illustrates Write cycle timing. Addresses on A/$\overline{B}$ and D/$\overline{C}$ and the status on $\overline{INTACK}$ must remain stable throughout the cycle. If $\overline{CE}$ falls after $\overline{WR}$ falls or if it rises before $\overline{WR}$ rises, the effective $\overline{WR}$ is shortened

## Interrupt Acknowledge Cycle Timing

Figure 15 illustrates Interrupt Acknowledge cycle timing. Between the time $\overline{INTACK}$ goes LOW and the falling edge of $\overline{RD}$, the internal and external IEI/IEO daisy chains settle. If there is an interrupt pending in the SCC and IEI is HIGH when $\overline{RD}$ falls, the Acknowledge cycle is intended for the SCC. In this case, the SCC may be programmed to respond to $\overline{RD}$ Low by placing its interrupt vector on $D_0 - D_7$, and it then sets the appropriate Interrupt-Under-Service internally.

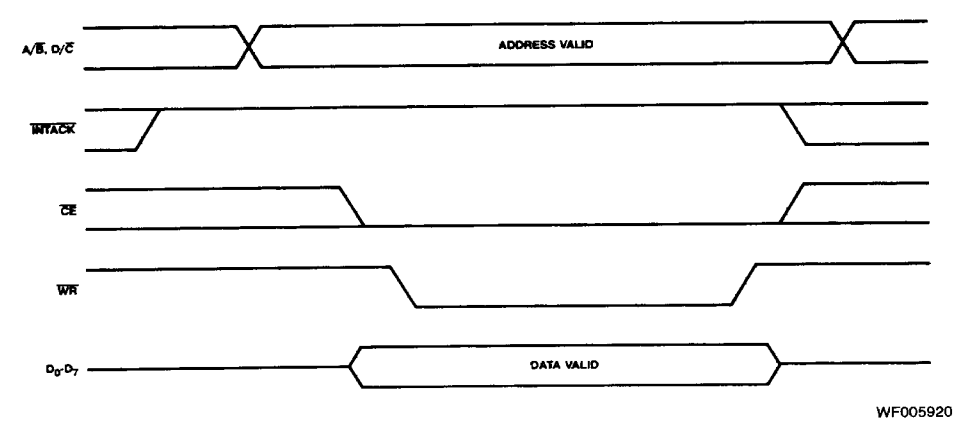



**Figure 13. Read Cycle Timing**

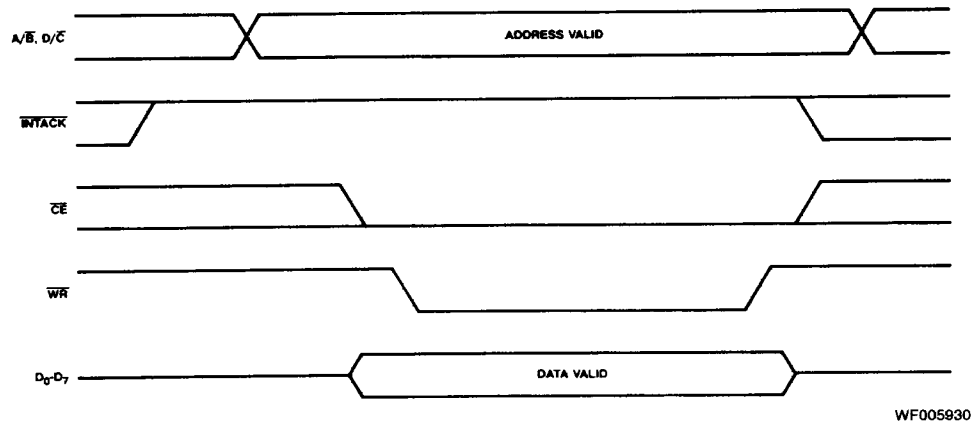



**Figure 14. Write Cycle Timing**

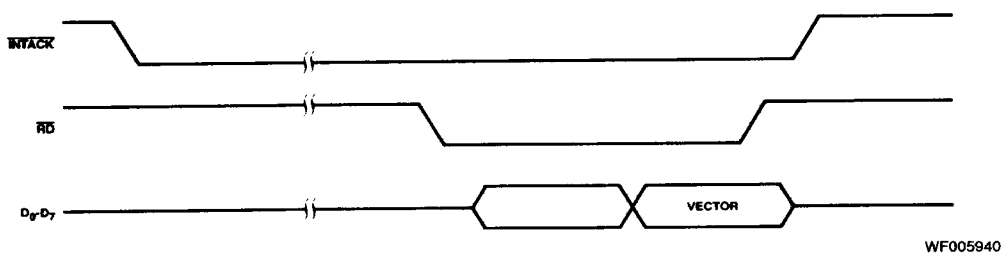



**Figure 15. Interrupt Acknowledge Cycle Timing**

## ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65 to +150°C
Voltage at any Pin
Relative to $V_{SS}$ ..... −0.5 to +7.0V
Power Dissipation ..... 1.8W

*Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.*

## OPERATING RANGES

Commercial (C) Devices
Temperature ($T_A$) ..... 0 to +70°C
Supply Voltage ($V_{CC}$) ..... 5 V ± 5%

*Operating ranges define those limits between which the functionality of the device is guaranteed.*

## DC CHARACTERISTICS over operating range

| Parameters | Description | Test Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $V_{IH}$ | Input HIGH Voltage | Commercial | 2.0 | | $V_{CC}$+0.3 | V |
| $V_{IL}$ | Input LOW Voltage | | −0.3 | | 0.8 | V |
| $V_{OH}$ | Output HIGH Voltage | $I_{OH}$ = −250μA | 2.4 | | | V |
| $V_{OL}$ | Output LOW Voltage | $I_{OL}$ = +2.0mA | | | 0.4 | V |
| $I_{IL}$ | Input Leakage | 0.4 V ≤ $V_{IN}$ ≤ 2.4 V | | | ±10.0 | μA |
| $I_{OL}$ | Output Leakage | 0.4 V ≤ $V_{OUT}$ ≤ 2.4 V | | | ±10.0 | μA |
| $I_{CC}$ | $V_{CC}$ Supply Current | | | | 250 | mA |
| $C_{IN}$ | Input Capacitance | Unmeasured pins returned to ground. f = 1MHz at $T_A$ = 25°C. | | | 10 | pF |
| $C_{OUT}$ | Output Capacitance | | | | 15 | pF |
| $C_{I/O}$ | Bidirectional Capacitance | | | | 20 | pF |

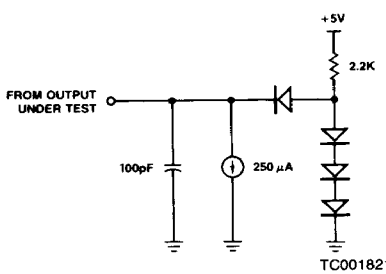
## Standard Test Conditions

The characteristics below apply for the following standard test conditions, unless otherwise noted. All voltages are referenced to GND. Positive current flows into the referenced pin. Standard conditions are as follows:

+4.75V ≤ $V_{CC}$ ≤ +5.25V
GND = 0V
0°C ≤ $T_A$ ≤ 70°C

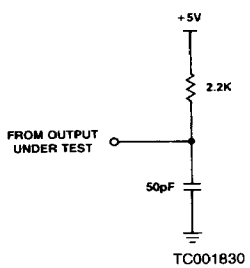
## SWITCHING TEST CIRCUITS

### Standard Test Load



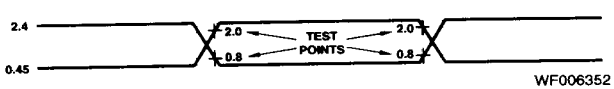

TC001821

### Open Drain Test Load




TC001830

## SWITCHING TEST INPUT/OUTPUT WAVEFORM




WF006352

AC testing: Inputs are driven at 2.4 V for a logic "1" and 0.45 V for a logic "0". Timing measurements are made at 2.0 V for a logic "1" and 0.8 V for logic "0".

See Section 6 for Thermal Characteristics Information.

## SWITCHING CHARACTERISTICS over operating range

### GENERAL TIMING

| Number | Parameters | Description | | 4 MHz Min | 4 MHz Max | 6 MHz Min | 6 MHz Max | 8 MHz Z8530H Only Min | 8 MHz Z8530H Only Max | Units |
|---|---|---|---|---|---|---|---|---|---|---|
| 1 | TdPC(REQ) | PCLK ↓ to W/REQ Valid Delay | | | 250 | | 250 | | 250 | ns |
| 2 | TdPC(W) | PCLK ↓ to Wait Inactive Delay | | | 350 | | 350 | | 350 | ns |
| 3 | TsRXC(PC) | RxC ↑ to PCLK ↑ Set-up Time (Notes 1, 4) | Z8530 | 80 | TWPCL | 70 | TWPCL | NA | NA | ns |
| | | | Z8530H | 80 | TWPCL | 70 | TWPCL | 60 | TWPCL | |
| 4 | TsRXD(RXCr) | RxD to RxC ↑ Set-up Time (XI Mode) (Note 1) | | 0 | | 0 | | 0 | | ns |
| 5 | ThRXD(RXCr) | RxD to RxC ↑ Hold Time (XI Mode) (Note 1) | | 150 | | 150 | | 150 | | ns |
| 6 | TsRXD(RXCf) | RxD to RxC ↓ Set-up Time (XI Mode) (Notes 1, 5) | | 0 | | 0 | | 0 | | ns |
| 7 | ThRXD(RXCf) | RxD to RxC ↓ Hold Time (XI Mode) (Notes 1, 5) | | 150 | | 150 | | 150 | | ns |
| 8 | TsSY(RXC) | SYNC to RxC ↑ Set-up Time (Note 1) | | −200 | | −200 | | −200 | | ns |
| 9 | ThSY(RXC) | SYNC to RxC ↑ Hold Time (Note 1) | | 3TcPC + 400 | | 3TcPC + 320 | | 3TcPC + 250 | | ns |
| 10 | TsTXC(PC) | TxC ↓ to PCLK ↑ Set-up Time (Notes 2, 4) | | 0 | | 0 | | 0 | | ns |
| 11 | TdTXCf(TXD) | TxC ↓ to TxD Delay (XI Mode) (Note 2) | | | 300 | | 230 | | 200 | ns |
| 12 | TdTXCr(TXD) | TxC ↑ to TxD Delay (XI Mode) (Notes 2, 5) | | | 300 | | 230 | | 200 | ns |
| 13 | TdTXD(TRX) | TxD to TRxC Delay (Send Clock Echo) | | | 200 | | 200 | | 200 | ns |
| 14 | TwRTXh | RTxC High Width (Note 6) | | 180 | | 180 | | 150 | | ns |
| 15 | TwRTXl | RTxC Low Width (Note 6) | | 180 | | 180 | | 150 | | ns |
| 16 | TcRTX | RTxC Cycle Time (Notes 6, 7) | | 1000 | | 660 | | 500 | | ns |
| 17 | TcRTXX | Crystal Oscillator Period (Note 3) | | 250 | 1000 | 165 | 1000 | 125 | 1000 | ns |
| 18 | TwTRXh | TRxC High Width (Note 6) | | 180 | | 180 | | 150 | | ns |
| 19 | TwTRXl | TRxC Low Width (Note 6) | | 180 | | 180 | | 150 | | ns |
| 20 | TcTRX | TRxC Cycle Time (Notes 6, 7) | | 1000 | | 660 | | 500 | | ns |
| 21 | TwEXT | DCD or CTS Pulse Width | | 200 | | 200 | | 200 | | ns |
| 22 | TwSY | SYNC Pulse Width | | 200 | | 200 | | 200 | | ns |

Notes:
1. RxC is RTxC or TRxC, whichever is supplying the receive clock.
2. TxC is TRxC or RTxC, whichever is supplying the transmit clock.
3. Both RTxC and SYNC have 18 pF capacitors to ground connected to them.
4. Parameter applies only if the data rate is one-fourth the PCLK rate. In all other cases, no phase relationship between RxC and PCLK or TxC and PCLK is required.
5. Parameter applies only to FM encoding/decoding.
6. Parameter applies only for transmitter and receiver; DPLL and baud rate generator timing requirements are identical to chip PCLK requirements.
7. The maximum receive or transmit data is 1/4 PCLK.

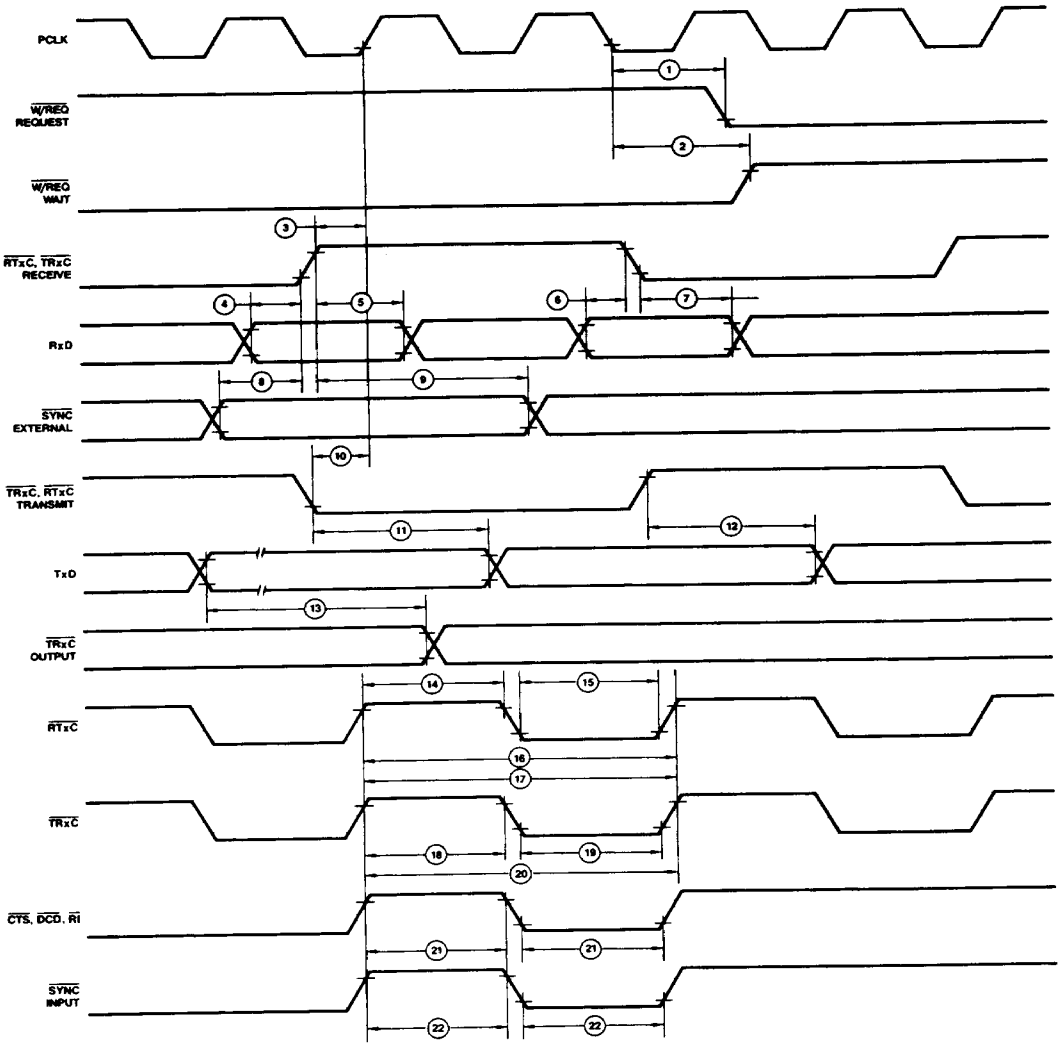



**Figure 16. General Timing**

## SWITCHING CHARACTERISTICS over operating range
### SYSTEM TIMING (Z8030)

| Number | Parameters | Description | 4 MHz Min | 4 MHz Max | 6 MHz Min | 6 MHz Max | Units |
|---|---|---|---|---|---|---|---|
| 1 | TdRXC(REQ) | $\overline{RxC}$ ↑ to $\overline{W/REQ}$ Valid Delay (Note 2) | 8 | 12 | 8 | 12 | TcPC |
| 2 | TdRXC(W) | $\overline{RxC}$ ↑ Wait Inactive Delay (Notes 1, 2) | 8 | 14 | 8 | 14 | TcPC |
| 3 | TdRXC(SY) | $\overline{RxC}$ ↑ to $\overline{SYNC}$ Valid Delay (Note 2) | 4 | 7 | 4 | 7 | TcPC |
| 4 | TdRXC(INT) | $\overline{RxC}$ ↑ $\overline{INT}$ Valid Delay (Notes 1, 2) | 8 +2 | 12 +3 | 8 +2 | 12 +3 | TcPC $\overline{AS}$ |
| 5 | TdTXC(REQ) | $\overline{TxC}$ ↓ to $\overline{W/REQ}$ Valid Delay (Note 3) | 5 | 8 | 5 | 8 | TcPC |
| 6 | TdTXC(W) | $\overline{TxC}$ ↓ to Wait Inactive Delay (Notes 1, 3) | 5 | 11 | 5 | 11 | TcPC |
| 7 | TdTXC(DRQ) | $\overline{TxC}$ ↓ to $\overline{DTR/REQ}$ Valid Delay (Note 3) | 4 | 7 | 4 | 7 | TcPC |
| 8 | TdTXC(INT) | $\overline{TxC}$ ↓ to $\overline{INT}$ Valid Delay (Notes 1, 3) | 4 +2 | 6 +3 | 4 +2 | 6 +3 | TcPC $\overline{AS}$ |
| 9 | TdSY(INT) | $\overline{SYNC}$ Transition to $\overline{INT}$ Valid Delay (Note 1) | 2 | 3 | 2 | 3 | TcPC |
| 10 | TdEXT(INT) | $\overline{DCD}$ or $\overline{CTS}$ Transition to $\overline{INT}$ Valid Delay (Note 1) | 2 | 3 | 2 | 3 | TcPC |

Notes: 1. Open-drain output, measured with open-drain test load.
2. $\overline{RxC}$ is $\overline{RTxC}$ or $\overline{TRxC}$, whichever is supplying the receive clock.
3. $\overline{TxC}$ is $\overline{TRxC}$ or $\overline{RTxC}$, whichever is supplying the transmit clock.

## SWITCHING CHARACTERISTICS over operating range
### SYSTEM TIMING (Z8530, Z8530H)

| Number | Parameters | Description | 4 MHz Min | 4 MHz Max | 6 MHz Min | 6 MHz Max | 8 MHz Z8530H Only Min | 8 MHz Z8530H Only Max | Units |
|---|---|---|---|---|---|---|---|---|---|
| 1 | TdRXC(REQ) | $\overline{RxC}$ ↑ $\overline{W/REQ}$ Valid Delay (Note 2) | 8 | 12 | 8 | 12 | 8 | 12 | TcPC |
| 2 | TdRXC(W) | $\overline{RxC}$ ↑ to Wait Inactive Delay (Notes 1, 2) | 8 | 14 | 8 | 14 | 8 | 14 | TcPC |
| 3 | TdRXC(SY) | $\overline{RxC}$ ↑ to $\overline{SYNC}$ Valid Delay (Note 2) | 4 | 7 | 4 | 7 | 4 | 7 | TcPC |
| 4 | TdRXC(INT) | $\overline{RxC}$ ↑ to $\overline{INT}$ Valid Delay (Notes 1, 2) | 10 | 16 | 10 | 16 | 10 | 16 | TcPC |
| 5 | TdTXC(REQ) | $\overline{TxC}$ ↓ to $\overline{W/REQ}$ Valid Delay (Note 3) | 5 | 8 | 5 | 8 | 5 | 8 | TcPC |
| 6 | TdTXC(W) | $\overline{TxC}$ ↓ to Wait Inactive Delay (Notes 1, 3) | 5 | 11 | 5 | 11 | 5 | 11 | TcPC |
| 7 | TdTXC(DRQ) | $\overline{TxC}$ ↓ to $\overline{DTR/REQ}$ Valid Delay (Note 3) | 4 | 7 | 4 | 7 | 4 | 7 | TcPC |
| 8 | TdTXC(INT) | $\overline{TxC}$ ↓ to $\overline{INT}$ Valid Delay (Notes 1, 3) | 6 | 10 | 6 | 10 | 6 | 10 | TcPC |
| 9 | TdSY(INT) | $\overline{SYNC}$ Transition to $\overline{INT}$ Valid Delay (Note 1) | 2 | 6 | 2 | 6 | 2 | 6 | TcPC |
| 10 | TdEXT(INT) | $\overline{DCD}$ or $\overline{CTS}$ Transition to $\overline{INT}$ Valid Delay (Note 1) | 2 | 6 | 2 | 6 | 2 | 6 | TcPC |

Notes: 1. Open-drain output, measured with open-drain test load.
2. $\overline{RxC}$ is $\overline{RTxC}$ or $\overline{TRxC}$, whichever is supplying the receive clock.
3. $\overline{TxC}$ is $\overline{TRxC}$ or $\overline{RTxC}$, whichever is supplying the transmit clock.

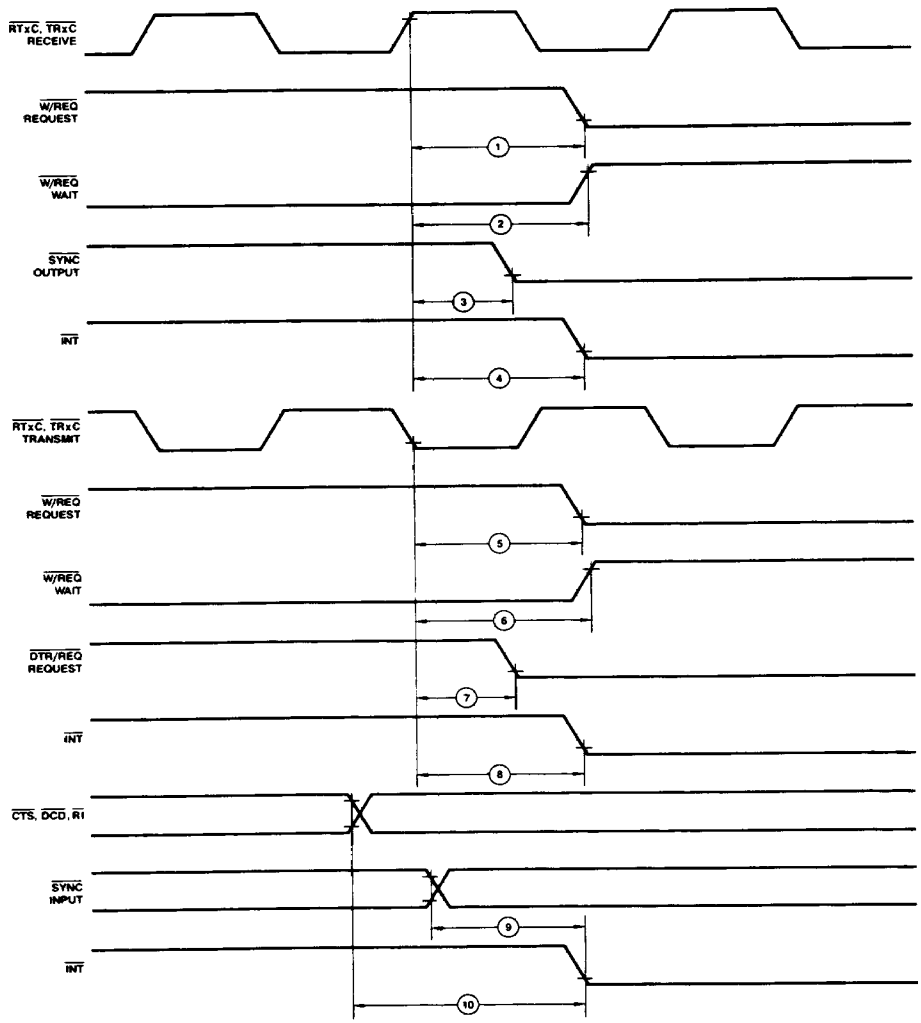



**Figure 17. System Timing**

## SWITCHING CHARACTERISTICS over operating range
### READ AND WRITE TIMING (Z8030)

| Number | Parameters | Description | 4 MHz | | 6 MHz | | Units |
|---|---|---|---|---|---|---|---|
| | | | Min | Max | Min | Max | |
| 1 | TwAS | $\overline{AS}$ LOW Width | 70 | | 50 | | ns |
| 2 | TdDS(AS) | $\overline{DS}$ ↑ to $\overline{AS}$ ↓ Delay | 50 | | 25 | | ns |
| 3 | TsCS0(AS) | $\overline{CS_0}$ to $\overline{AS}$ ↑ Set-up Time (Note 1) | 0 | | 0 | | ns |
| 4 | ThCS0(AS) | $\overline{CS_0}$ to $\overline{AS}$ ↑ Hold Time (Note 1) | 60 | | 40 | | ns |
| 5 | TsCS1(DS) | $CS_1$ to $\overline{DS}$ ↓ Set-up Time (Note 1) | 100 | | 80 | | ns |
| 6 | ThCS1(DS) | $CS_1$ to $\overline{DS}$ ↑ Hold Time (Note 1) | 55 | | 40 | | ns |
| 7 | TsIA(AS) | $\overline{INTACK}$ to $\overline{AS}$ ↑ Set-up Time | 10 | | 10 | | ns |
| 8 | ThIA(AS) | $\overline{INTACK}$ to $\overline{AS}$ ↑ Hold Time | 250 | | 200 | | ns |
| 9 | TsRWR(DS) | R/$\overline{W}$ (Read) to $\overline{DS}$ ↓ Set-up Time | 100 | | 80 | | ns |
| 10 | ThRW(DS) | R/$\overline{W}$ to $\overline{DS}$ ↑ Hold Time | 55 | | 40 | | ns |
| 11 | TsRWW(DS) | R/$\overline{W}$ (Write) to $\overline{DS}$ ↓ Set-up Time | 0 | | 0 | | ns |
| 12 | TdAS(DS) | $\overline{AS}$ ↑ to $\overline{DS}$ ↓ Delay | 60 | | 40 | | ns |
| 13 | TwDSI | $\overline{DS}$ LOW Width | 390 | | 250 | | ns |
| 14 | TrC | Valid Access Recovery Time (Note 2) | 6TcPC + 200 | | 6TcPC + 130 | | ns |
| 15 | TsA(AS) | Address to $\overline{AS}$ ↑ Set-up Time (Note 1) | 30 | | 10 | | ns |
| 16 | ThA(AS) | Address to $\overline{AS}$ ↑ Hold Time (Note 1) | 50 | | 30 | | ns |
| 17 | TsDW(DS) | Write Data to $\overline{DS}$ ↓ Set-up Time | 30 | | 20 | | ns |
| 18 | ThDW(DS) | Write Date to $\overline{DS}$ ↑ Hold Time | 30 | | 20 | | ns |
| 19 | TdDS(DA) | $\overline{DS}$ ↓ to Data Active Delay | 0 | | 0 | | ns |
| 20 | TdDSr(DR) | $\overline{DS}$ ↑ to Read Data Not Valid Delay | 0 | | 0 | | ns |
| 21 | TdDSf(DR) | $\overline{DS}$ ↓ to Read Data Valid Delay | | 250 | | 180 | ns |
| 22 | TdAS(DR) | $\overline{AS}$ ↑ to Read Data Valid Delay | | 520 | | 335 | ns |

Notes: 1. Parameter does not apply to Interrupt Acknowledge transactions.
2. Parameter applies only between transactions involving the $S_{CC}$.

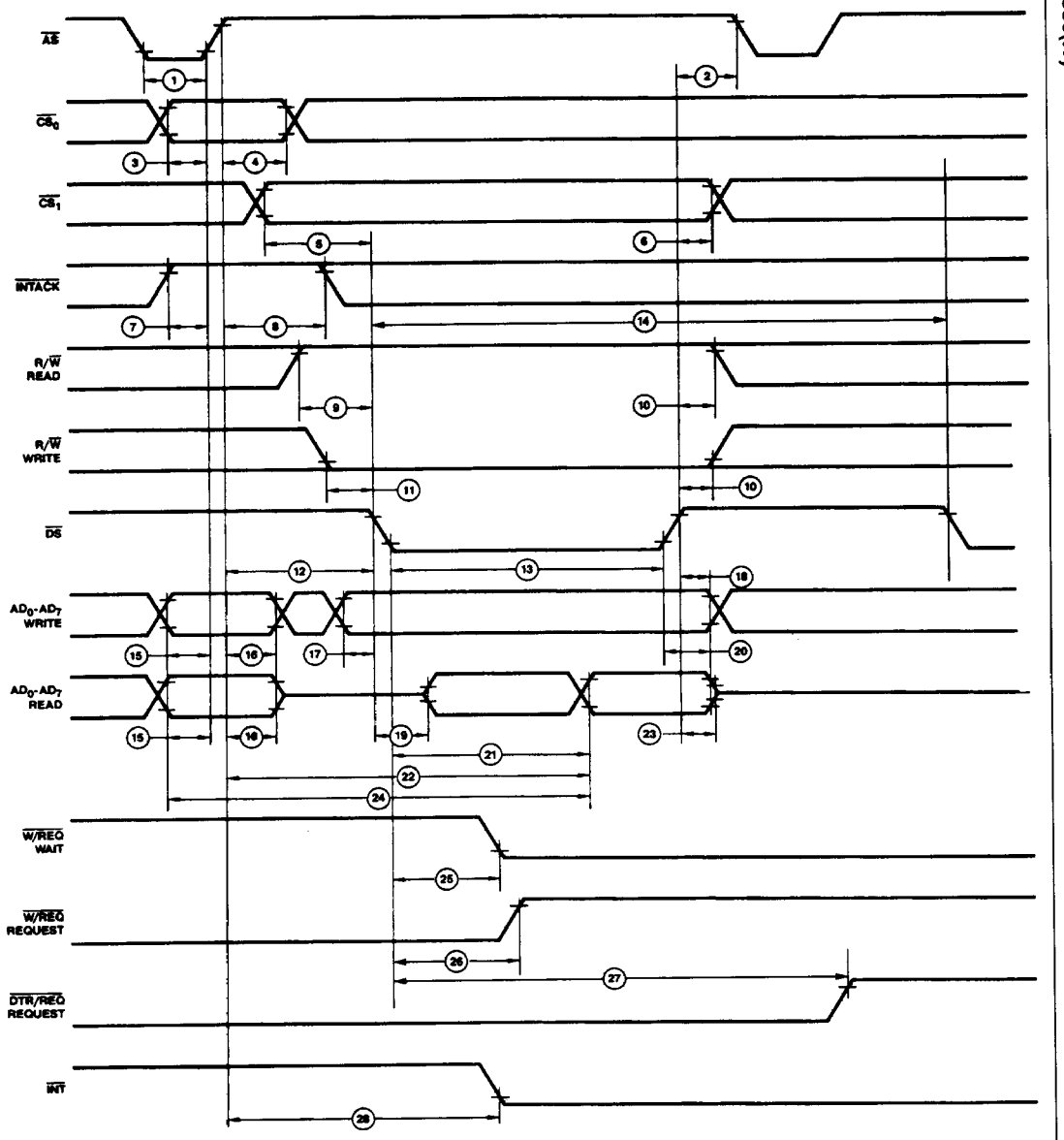



**Figure 18. Read and Write Timing (Z8030)**

## SWITCHING CHARACTERISTICS over operating range
### READ AND WRITE TIMING (Z8530, Z8530H)

| Number | Parameters | Description | 4 MHz | | 6 MHz | | 8 MHz Z8530H Only | | Units |
|---|---|---|---|---|---|---|---|---|---|
| | | | Min | Max | Min | Max | Min | Max | |
| 1 | TwPCl | PCLK Low Width | 105 | 2000 | 70 | 1000 | 50 | 1000 | ns |
| 2 | TwPCh | PCLK High Width | 105 | 2000 | 70 | 1000 | 50 | 1000 | ns |
| 3 | TfPC | PCLK Fall Time | | 20 | | 10 | | 10 | ns |
| 4 | TrPC | PCLK Rise Time | | 20 | | 10 | | 10 | ns |
| 5 | TcPC | PCLK Cycle Time | 250 | 4000 | 165 | 2000 | 125 | 2000 | ns |
| 6 | TsA(WR) | Address to $\overline{WR}$ ↓ Set-up Time | 80 | | 80 | | 70 | | ns |
| 7 | ThA(WR) | Address to $\overline{WR}$ ↑ Hold Time | 0 | | 0 | | 0 | | ns |
| 8 | TsA(RD) | Address to $\overline{RD}$ ↓ Set-up Time | 80 | | 80 | | 70 | | ns |
| 9 | ThA(RD) | Address to $\overline{RD}$ ↑ Hold Time | 0 | | 0 | | 0 | | ns |
| 10 | TsIA(PC) | $\overline{INTACK}$ to PCLK ↑ Set-up Time | 10 | | 10 | | 10 | | ns |
| 11 | TsIAi(WR) | $\overline{INTACK}$ to $\overline{WR}$ ↓ Set-up Time (Note 1) | 200 | | 160 | | 145 | | ns |
| 12 | ThIA(WR) | $\overline{INTACK}$ to $\overline{WR}$ ↑ Hold Time | 0 | | 0 | | 0 | | ns |
| 13 | TsIAi(RD) | $\overline{INTACK}$ to $\overline{RD}$ ↓ Set-up Time (Note 1) | 200 | | 160 | | 145 | | ns |
| 14 | ThIA(RD) | $\overline{INTACK}$ to $\overline{RD}$ ↑ Hold Time | 0 | | 0 | | 0 | | ns |
| 15 | ThIA(PC) | $\overline{INTACK}$ to PCLK ↑ Hold Time | 100 | | 100 | | 85 | | ns |
| 16 | TsCEl(WR) | $\overline{CE}$ Low to $\overline{WR}$ ↓ Set-up Time | 0 | | 0 | | 0 | | ns |
| 17 | ThCE(WR) | $\overline{CE}$ to $\overline{WR}$ ↑ Hold Time | 0 | | 0 | | 0 | | ns |
| 18 | TsCEh(WR) | $\overline{CE}$ High to $\overline{WR}$ ↓ Set-up Time | 100 | | 70 | | 60 | | ns |
| 19 | TsCEl(RD) | $\overline{CE}$ Low to $\overline{RD}$ ↓ Set-up Time (Note 1) | 0 | | 0 | | 0 | | ns |
| 20 | ThCE(RD) | $\overline{CE}$ to $\overline{RD}$ ↑ Hold Time (Note 1) | 0 | | 0 | | 0 | | ns |
| 21 | TsCEh(RD) | $\overline{CE}$ High to $\overline{RD}$ ↓ Set-up Time (Note 1) | 100 | | 70 | | 60 | | ns |
| 22 | TwRDl | $\overline{RD}$ Low Width (Note 1) | 240 | | 200 | | 150 | | ns |
| 23 | TdRD(DRA) | $\overline{RD}$ ↓ to Read Data Active Delay | 0 | | 0 | | 0 | | ns |
| 24 | TdRDr(DR) | $\overline{RD}$ ↑ to Read Data Not Valid Delay | 0 | | 0 | | 0 | | ns |
| 25 | TdRDf(DR) | $\overline{RD}$ ↓ to Read Data Valid Delay | | 250 | | 180 | | 140 | ns |
| 26 | TdRD(DRz) | $\overline{RD}$ ↑ to Read Data Float Delay (Note 2) | | 70 | | 45 | | 140 | ns |

Notes: 1. Parameter does not apply to Interrupt Acknowledge transactions.
2. Float delay is defined as the time required for a ±0.5V change in the output with a maximum DC load and minimum AC load.

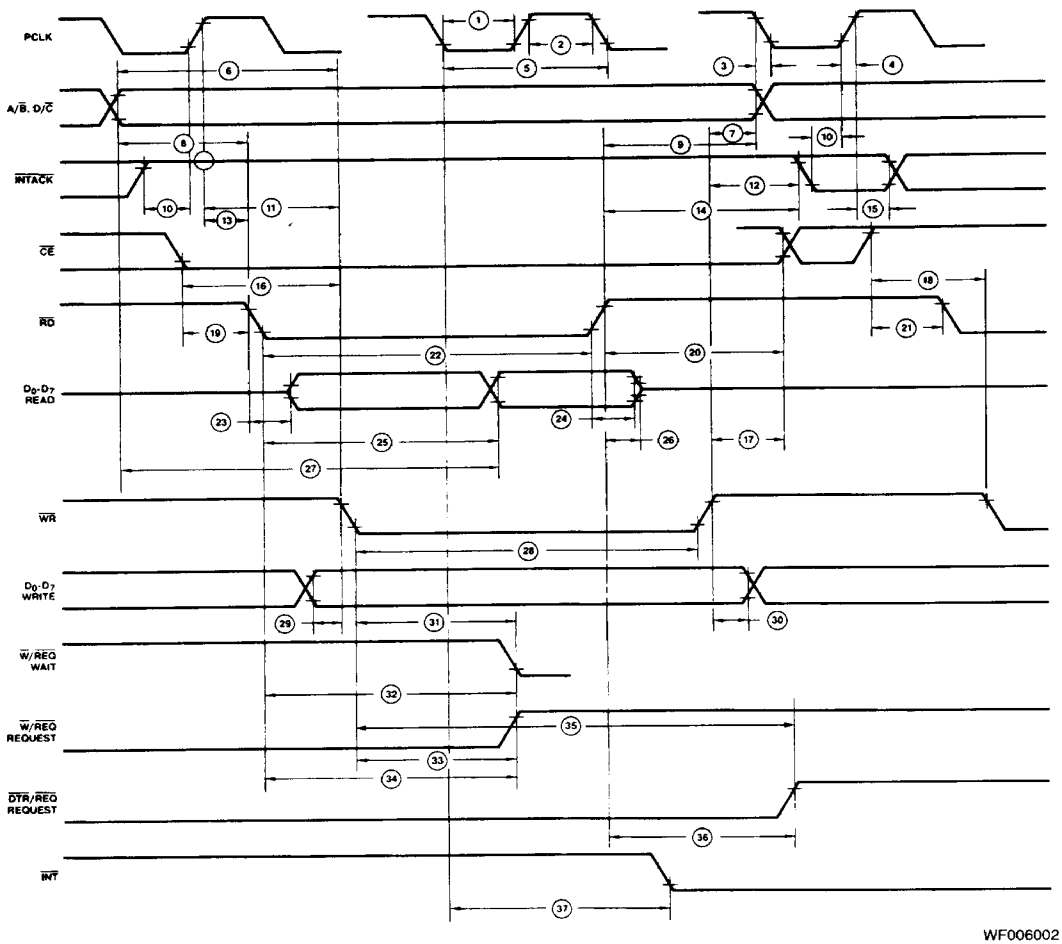



**Figure 19. Read and Write Timing (Z8530, Z8530,H)**

## SWITCHING CHARACTERISTICS over operating range
### INTERRUPT ACKNOWLEDGE TIMING, RESET TIMING, CYCLE TIMING (Z8030)

| Number | Parameters | Description | 4MHz | | 6MHz | | Units |
|---|---|---|---|---|---|---|---|
| | | | Min | Max | Min | Max | |
| 23 | TdDS(DRz) | $\overline{DS}$ ↑ to Read Data Float Delay (Note 3) | | 70 | | 45 | ns |
| 24 | TdA(DR) | Address Required Valid to Read Data Valid Delay | | 570 | | 310 | ns |
| 25 | TdDS(W) | $\overline{DS}$ ↓ to Wait Valid Delay (Note 4) | | 240 | | 200 | ns |
| 26 | TdDSf(REQ) | $\overline{DS}$ ↓ to $\overline{W/REQ}$ Not Valid Delay | | 240 | | 200 | ns |
| 27 | TdDSr(REQ) | $\overline{DS}$ ↓ to $\overline{DTR/REQ}$ Not Valid Delay | | 5TcPC + 300 | | 5TcPC + 250 | ns |
| 28 | TdAS(INT) | $\overline{AS}$ ↑ to $\overline{INT}$ Valid Delay (Note 4) | | 500 | | 500 | ns |
| 29 | TdAS(DSA) | $\overline{AS}$ ↑ to $\overline{DS}$ ↓ (Acknowledge) Delay (Note 5) | 250 | | 250 | | ns |
| 30 | TwDSA | $\overline{DS}$ (Acknowledge) Low Width | 390 | | 250 | | ns |
| 31 | TdDSA(DR) | $\overline{DS}$ ↓ (Acknowledge) to Read Data Valid Delay | | 250 | | 180 | ns |
| 32 | TsIEI(DSA) | IEI to $\overline{DS}$ ↓ (Acknowledge) Set-up Time | 120 | | 100 | | ns |
| 33 | ThIEI(DSA) | IEI to $\overline{DS}$ ↑ (Acknowledge) Hold Time | 0 | | 0 | | ns |
| 34 | TdIEI(IEO) | IEI to IEO Delay | | 120 | | 100 | ns |
| 35 | TdAS(IEO) | $\overline{AS}$ ↑ to IEO Delay (Note 6) | | 250 | | 250 | ns |
| 36 | TdDSA(INT) | $\overline{DS}$ ↓ (Acknowledge) to $\overline{INT}$ Inactive Delay (Note 4) | | 500 | | 500 | ns |
| 37 | TdDS(ASQ) | $\overline{DS}$ ↑ to $\overline{AS}$ ↓ Delay for No Reset | 30 | | 15 | | ns |
| 38 | TdASQ(DS) | $\overline{AS}$ ↑ to $\overline{DS}$ ↓ Delay for No Reset | 30 | | 30 | | ns |
| 39 | TwRES | $\overline{AS}$ and $\overline{DS}$ Coincident Low for Reset (Note 7) | 250 | | 200 | | ns |
| 40 | TwPCl | PCLK Low Width | 105 | 2000 | 70 | 1000 | ns |
| 41 | TwPCh | PCLK High Width | 105 | 2000 | 70 | 1000 | ns |
| 42 | TcPC | PCLK Cycle Time | 250 | 4000 | 165 | 2000 | ns |
| 43 | TrPC | PCLK Rise Time | | 20 | | 10 | ns |
| 44 | TfPC | PCLK Fall Time | | 20 | | 10 | ns |

Notes: 3. Float delay is defined as the time required for a ±0.5V change in the output with a maximum DC load and minimum AC load.
4. Open-drain output, measured with open-drain test load.
5. Parameter is system dependent. For any Z-SCC in the daisy chain, TdAS(DSA) must be greater than the sum of TdAS(IEO) for the highest priority device in the daisy chain, TsIEI(DSA) for the Z-SCC, and TdIEIf(IEO) for each device separating them in the daisy chain.
6. Parameter applies only to a Z-SCC pulling $\overline{INT}$ LOW at the beginning of the Interrupt Acknowledge transaction.
7. Internal circuitry allows for the reset provided by the Z8 to be recognized as a reset by the Z-SCC.

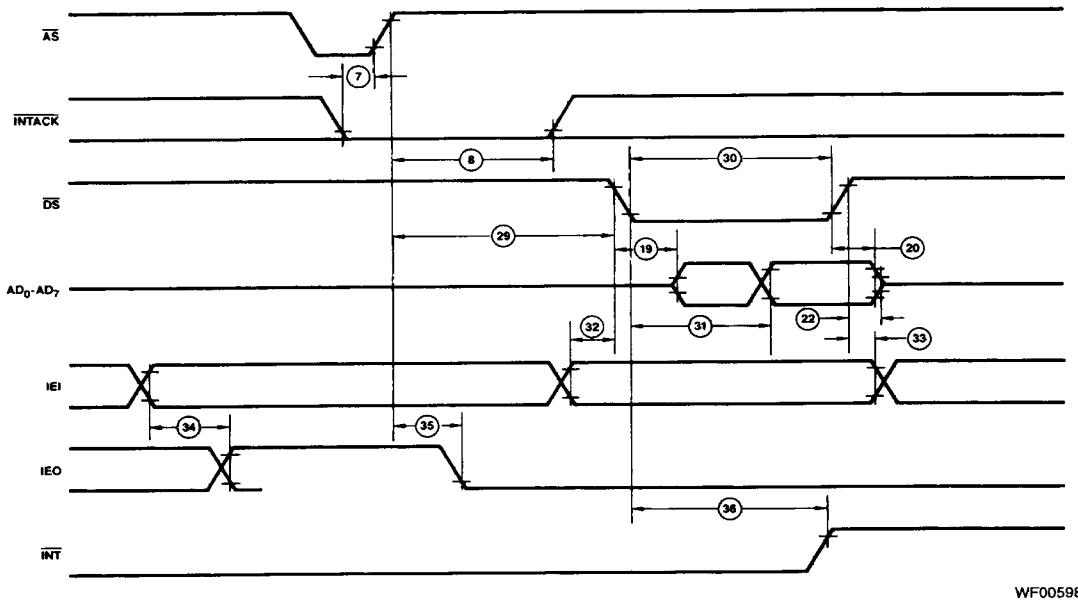



Figure 20. Interrupt Acknowledge Timing (Z8030)

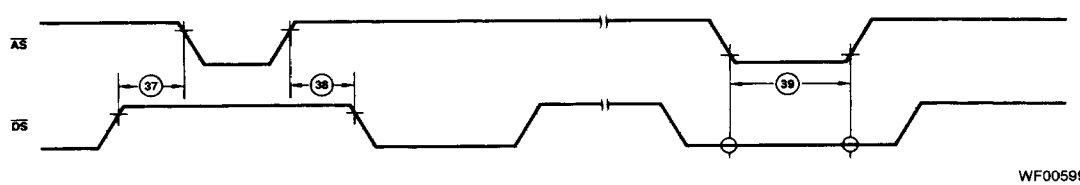



Figure 21. Reset Timing (Z8030)

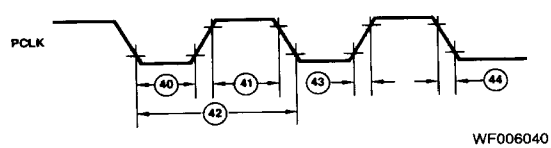



Figure 22. Cycle Timing (Z8030)

## SWITCHING CHARACTERISTICS over operating range
### INTERRUPT ACKNOWLEDGE TIMING, RESET TIMING, CYCLE TIMING (Z8530, Z8530H)

| Number | Parameters | Description | | 4 MHz Min | 4 MHz Max | 6 MHz Min | 6 MHz Max | 8 MHz Z8530H Only Min | 8 MHz Z8530H Only Max | Units |
|---|---|---|---|---|---|---|---|---|---|---|
| 27 | TdA(DR) | Address Required Valid to Read Data Valid Delay | Z8530 | | 400 | | 350 | NA | NA | ns |
| | | | Z8530H | | 300 | | 280 | | 220 | |
| 28 | TwWRI | $\overline{WR}$ Low Width | | 240 | | 200 | | 150 | | ns |
| 29 | TsDW(WR) | Write Data to $\overline{WR}$ ↓ Set-up Time | | 10 | | 10 | | 10 | | ns |
| 30 | ThDW(WR) | Write Data to $\overline{WR}$ ↑ Hold Time | | 0 | | 0 | | 0 | 170 | ns |
| 31 | TdWR(W) | $\overline{WR}$ ↓ to Wait Valid Delay (Note 4) | | | 240 | | 200 | | 170 | ns |
| 32 | TdRD(W) | $\overline{RD}$ ↓ to Wait Valid Delay (Note 4) | | | 240 | | 200 | | 170 | ns |
| 33 | TdWRf(REQ) | $\overline{WR}$ ↓ to $\overline{W/REQ}$ Not Valid Delay | | | 240 | | 200 | | 170 | ns |
| 34 | TdRDf(REQ) | $\overline{RD}$ ↓ to $\overline{W/REQ}$ Not Valid Delay | | | 240 | | 200 | | 170 | ns |
| 35 | TdWRr(REQ) | $\overline{WR}$ ↑ to $\overline{DTR/REQ}$ Not Valid Delay | | | 4TcPC | | 4TcPC | | 4TcPC | ns |
| 36 | TdRDr(REQ) | $\overline{RD}$ ↑ to $\overline{DTR/REQ}$ Not Valid Delay | | | 4TcPC | | 4TcPC | | 4TcPC | ns |
| 37 | TdPC(INT) | PCLK ↓ to $\overline{INT}$ Valid Delay (Note 4) | | | 500 | | 500 | | 500 | ns |
| 38 | TdIAi(RD) | $\overline{INTACK}$ to $\overline{RD}$ ↓ (Acknowledge) Delay (Note 5) | | 250 | | 200 | | 150 | | ns |
| 39 | TwRDA | $\overline{RD}$ (Acknowledge) Width | | 250 | | 200 | | 150 | | ns |
| 40 | TdRDA(DR) | $\overline{RD}$ ↓ (Acknowledge) to Read Data Valid Delay | | | 250 | | 180 | | 140 | ns |
| 41 | TsIEI(RDA) | IEI to $\overline{RD}$ ↓ (Acknowledge) Set-up Time | | 120 | | 100 | | 95 | | ns |
| 42 | ThIEI(RDA) | IEI to $\overline{RD}$ ↑ (Acknowledge) Hold Time | | 0 | | 0 | | 0 | | ns |
| 43 | TdIEI(IEO) | IEI to IEO Delay Time | | | 120 | | 100 | | 95 | ns |
| 44 | TdPC(IEO) | PCLK ↑ to IEO Delay | | | 250 | | 250 | | 200 | ns |
| 45 | TdRDA(INT) | $\overline{RD}$ ↓ to $\overline{INT}$ Inactive Delay (Note 4) | | | 500 | | 500 | | 450 | ns |
| 46 | TdRD(WRQ) | $\overline{RD}$ ↑ to $\overline{WR}$ ↓ Delay for No Reset | | 30 | | 15 | | 15 | | ns |
| 47 | TdWRQ(RD) | $\overline{WR}$ ↑ to $\overline{RD}$ ↓ Delay for No Reset | | 30 | | 30 | | 20 | | ns |
| 48 | TwRES | $\overline{WR}$ and $\overline{RD}$ Coincident Low for Reset | | 250 | | 200 | | 150 | | ns |
| 49 | Trc | Valid Access Recovery Time (Note 3) | Z8530 | 6TcPC + 200 | | 6TcPC + 130 | | NA | NA | ns |
| | | | Z8530H | 4TcPC | | 4TcPC | | 4TcPC | | |

Notes:
3. Parameter applies only between transactions involving the SCC.
4. Open-drain output, measured with open-drain test load.
5. Parameter is system dependent. For any SCC in the daisy chain, TdIAI(RD) must be greater than the sum of TdPC(IEO) for the highest priority device in the daisy chain, TsIEI(RDA) for the SCC, and TdIEI(IEO) for each device separating them in the daisy chain.

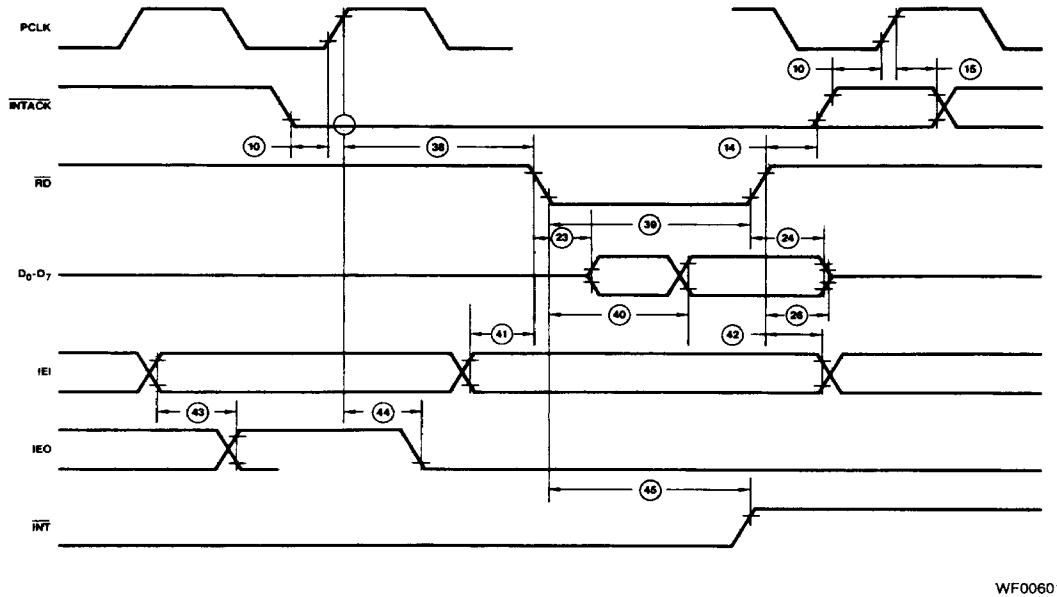



**Figure 23. Interrupt Acknowledge Timing (Z8530)**

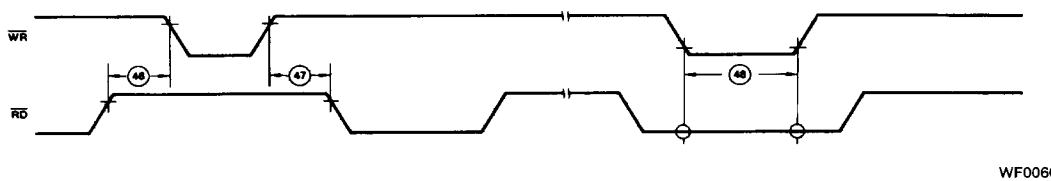



**Figure 24. Reset Timing (Z8530)**

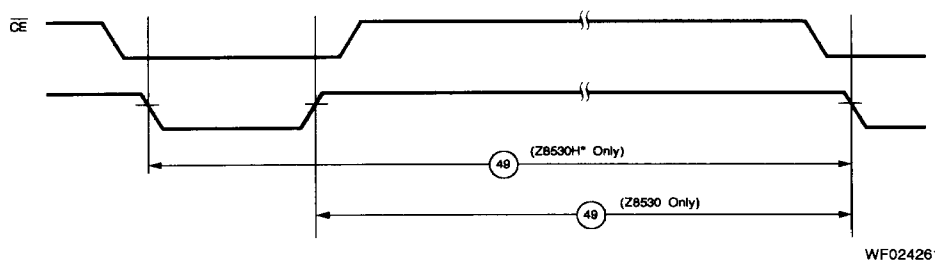



**Figure 25. Cycle Timing (Z8530, Z8530H)**

*Timings are preliminary and subject to change.