ADVANCE INFORMATION

Am29PDL128G

128 Megabit (8 M x 16-Bit/4 M x 32-Bit) CMOS 3.0 Volt-only, Simultaneous Operation Flash Memory with VersatileIO™ Control

DISTINCTIVE CHARACTERISTICS

ARCHITECTURAL ADVANTAGES

- **128Mbit Page Mode device**
  - Word (16-bit) or double word (32-bit) mode selectable via WORD# input
  - Page size of 8 words/4 double words: Fast page read access from random locations within the page
- **Single power supply operation**
  - Full Voltage range: 2.7 to 3.6 volt read, erase, and program operations for battery-powered applications
- **Simultaneous Read/Write Operation**
  - Data can be continuously read from one bank while executing erase/program functions in another bank
  - Zero latency switching from write to read operations
- **FlexBank Architecture**
  - 4 separate banks, with up to two simultaneous operations per device
  - Organized as two 16 Mbit banks (Bank 1 & 4) and two 48 Mbit banks (Bank 2 & 3)
- **VersatileI/O™ (V_{IO}) Control**
  - Output voltage generated and input voltages tolerated on the device is determined by the voltage on the V_{IO} pin
- **SecSi (Secured Silicon) Sector region**
  - 128 words (64 double words) accessible through a command sequence
- **Both top and bottom boot blocks in one device**
- **Manufactured on 0.17 µm process technology**
- **20-year data retention at 125°C**
- **Minimum 1 million write cycle guarantee per sector**

PERFORMANCE CHARACTERISTICS

- **High Performance**
  - Page access times as fast as 25 ns
  - Random access times as fast as 70 ns
- **Power consumption (typical values at 10 MHz)**
  - 38 mA active read current
  - 17 mA program/erase current
  - 1.5 µA typical standby mode current

SOFTWARE FEATURES

- **Software command-set compatible with JEDEC 42.4 standard**
  - Backward compatible with Am29F and Am29LV families
- **CFI (Common Flash Interface) complaint**
  - Provides device-specific information to the system, allowing host software to easily reconfigure for different Flash devices
- **Erase Suspend / Erase Resume**
  - Suspends an erase operation to allow read or program operations in other sectors of same bank
- **Unlock Bypass Program command**
  - Reduces overall programming time when issuing multiple program command sequences

HARDWARE FEATURES

- **Ready/Busy# pin (RY/BY#)**
  - Provides a hardware method of detecting program or erase cycle completion
- **Hardware reset pin (RESET#)**
  - Hardware method to reset the device to reading array data
- **WP# (Write Protect) input**
  - At V_{IL}, protects the two top and two bottom sectors, regardless of sector protect/unprotect status
  - At V_{IH}, allows removal of sector protection
  - An internal pull up to Vcc is provided
- **Persistent Sector Protection**
  - A command sector protection method to lock combinations of individual sectors and sector groups to prevent program or erase operations within that sector
  - Sectors can be locked and unlocked in-system at V_{CC} level
- **Password Sector Protection**
  - A sophisticated sector protection method to lock combinations of individual sectors and sector groups to prevent program or erase operations within that sector using a user-defined 64-bit password
- **ACC (Acceleration) input provides faster programming times in a factory setting**
- **Package options**
  - 80-ball Fortified BGA

This document contains information on a product under development at Advanced Micro Devices. The information is intended to help you evaluate this product. AMD reserves the right to change or discontinue work on this proposed product without notice.

Publication# **25685** Rev: **B** Amendment/**0**
Issue Date: **April 26, 2002**

GENERAL DESCRIPTION

The Am29PDL128G is a 128 Mbit, 3.0 volt-only Page Mode and Simultaneous Read/Write Flash memory device organized as 8 Mwords or 4 M double words (One word is equal to two bytes). The device is offered in an 80-ball Fortified BGA package. The word-wide data (x16) appears on DQ15-DQ0; the double word mode data (x32) appears on DQ31-DQ0. This device can be programmed in-system or in standard EPROM programmers. A 12.0 V V_{PP} is not required for write or erase operations.

The device offers fast page access times of 25 and 30 ns, with corresponding random access times of 70 and 80 ns, respectively, allowing high speed microprocessors to operate without wait states. To eliminate bus contention the device has separate chip enable (CE#), write enable (WE#) and output enable (OE#) controls.

Simultaneous Read/Write Operation with Zero Latency

The Simultaneous Read/Write architecture provides **simultaneous operation** by dividing the memory space into 4 banks, which can be considered to be four separate memory arrays as far as certain operations are concerned. The device can improve overall system performance by allowing a host system to program or erase in one bank, then immediately and simultaneously read from another bank with zero latency (with 2 simultaneous operations operating at any one time). This releases the system from waiting for the completion of a program or erase operation, greatly improving system performance.

The device can be organized in both top and bottom sector configurations (see Table 1).

Table 1. Bank/Sector Sizes

Bank	Number of Sectors	Sector Size (Word/Dbl. Word)	Bank Size
1	8	4/2	16 Mbit
	31	32/16	
2	96	32/16	48 Mbit
3	96	32/16	48 Mbit
4	8	4/2	16 Mbit
	31	32/16	

Page Mode Features

The device is AC timing, input/output, and package **compatible with 8 Mbit x16 page mode mask ROM**. The page size is 8 words or 4 double words.

After initial page access is accomplished, the page mode operation provides fast read access speed of random locations within that page.

Standard Flash Memory Features

The device requires a **single 3.0 volt power supply** (2.7 V to 3.6 V) for both read and write functions. Internally generated and regulated voltages are provided for the program and erase operations.

The device is entirely command set compatible with the **JEDEC 42.4 single-power-supply Flash standard**. Commands are written to the command register using standard microprocessor write timing. Register contents serve as inputs to an internal state-machine that controls the erase and programming circuitry. Write cycles also internally latch addresses and data needed for the programming and erase operations. Reading data out of the device is similar to reading from other Flash or EPROM devices.

Device programming occurs by executing the program command sequence. The Unlock Bypass mode facilitates faster programming times by requiring only two write cycles to program data instead of four. Device erasure occurs by executing the erase command sequence.

The host system can detect whether a program or erase operation is complete by reading the DQ7 (Data# Polling) and DQ6 (toggle) **status bits**. After a program or erase cycle has been completed, the device is ready to read array data or accept another command.

The sector erase architecture allows memory sectors to be erased and reprogrammed without affecting the data contents of other sectors. The device is fully erased when shipped from the factory.

Hardware data protection measures include a low V_{CC} detector that automatically inhibits write operations during power transitions. The hardware sector protection feature disables both program and erase operations in any combination of sectors of memory. This can be achieved in-system or via programming equipment.

The Erase Suspend/Erase Resume feature enables the user to put erase on hold for any period of time to read data from, or program data to, any sector that is not selected for erasure. True background erase can thus be achieved. If a read is needed from the SecSi Sector area (One Time Program area) after an erase suspend, then the user must use the proper command sequence to enter and exit this region.

The device offers two power-saving features. When addresses have been stable for a specified amount of time, the device enters the **automatic sleep mode**. The system can also place the device into the standby mode. Power consumption is greatly reduced in both these modes.

AMD's Flash technology combined years of Flash memory manufacturing experience to produce the highest levels of quality, reliability and cost effectiveness. The device electrically erases all bits within a sector simultaneously via Fowler-Nordheim tunneling. The data is programmed using hot electron injection.

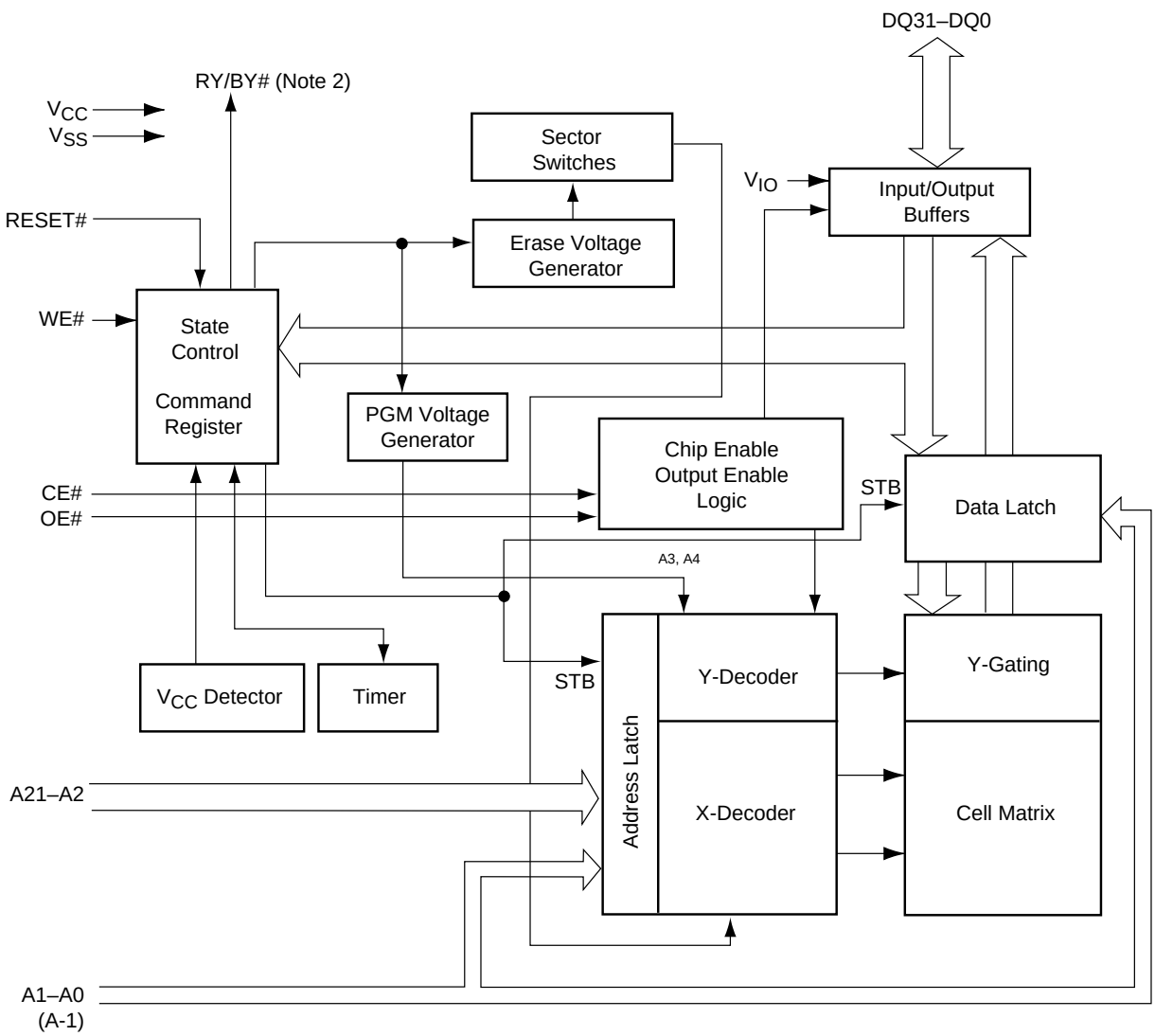
TABLE OF CONTENTS

PRODUCT SELECTOR GUIDE

Part Number		Am29PDL128G		
Speed Option	Voltage Range: V_{CC} = 3.0–3.6 V	**70R**		
	Voltage Range: V_{CC} = 2.7–3.6 V	**70**	**80**	**90**
Max Access Time, ns (t_{ACC})		70	80	90
Max CE# Access, ns (t_{CE})		70	80	90
Max Page Access, ns (t_{PACC})		25	30	35
Max OE# Access, ns (t_{OE})		25	30	40

Note: *See AC Characteristics section for full specifications.*

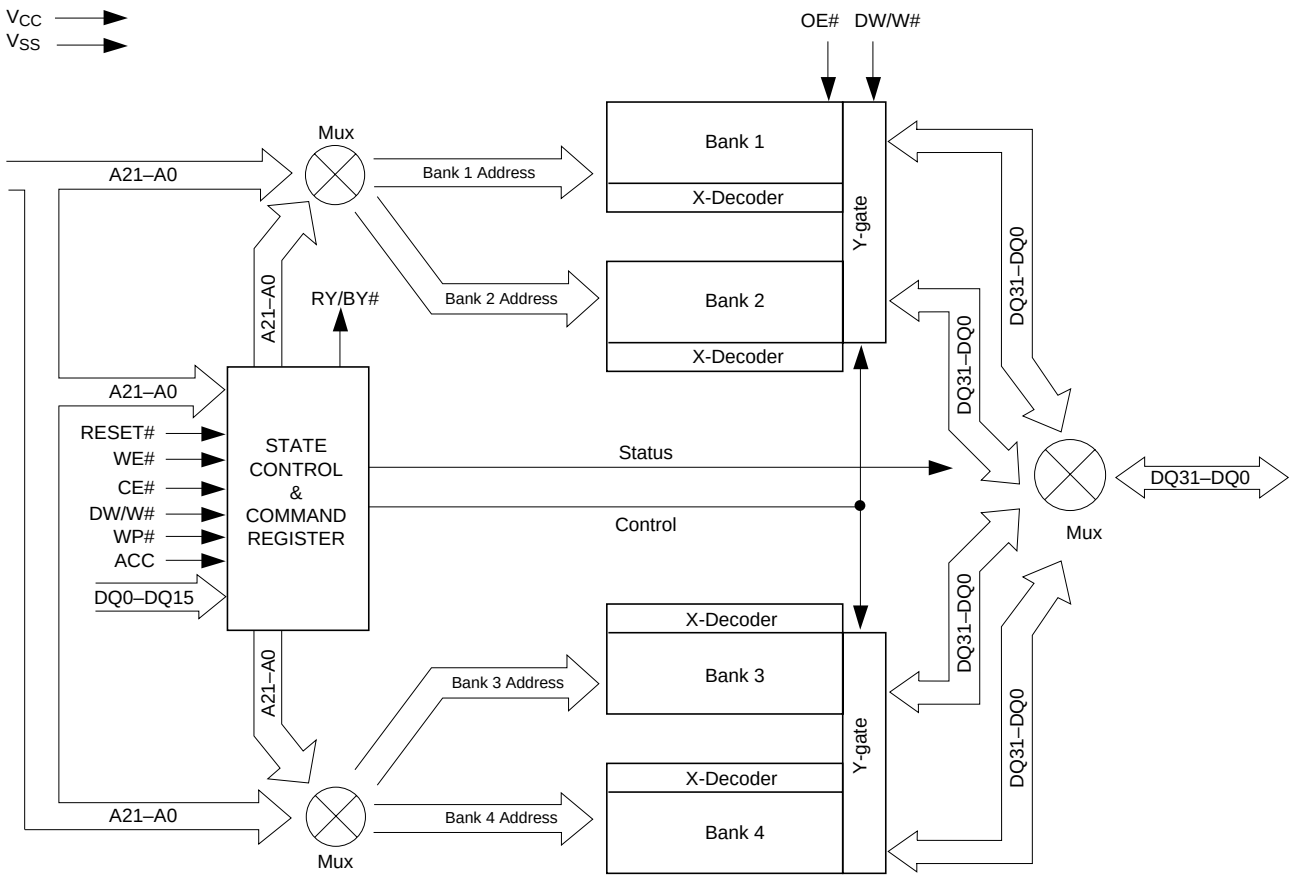
BLOCK DIAGRAM



Notes:

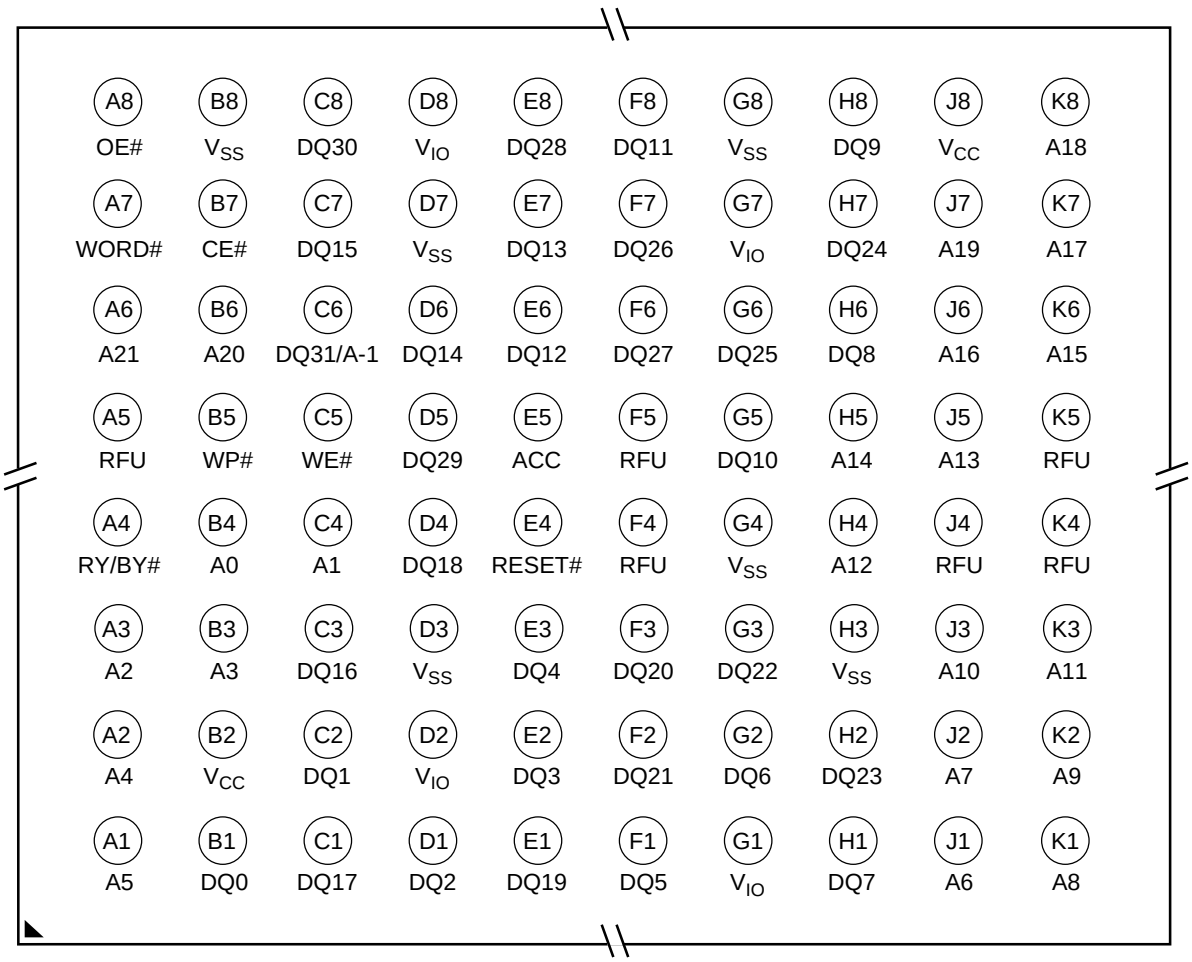
1. *In double word mode, input/outputs are DQ31-DQ0, address range is A21-A0. In word mode, input/outputs are DQ15-DQ0, address range is A21-A-1.*
2. *RY/BY# is an open drain output.*

SIMULTANEOUS OPERATION BLOCK DIAGRAM



CONNECTION DIAGRAMS

80-Ball Fortified BGA
Top View, Balls Facing Down



Special Handling Instructions for BGA Packages

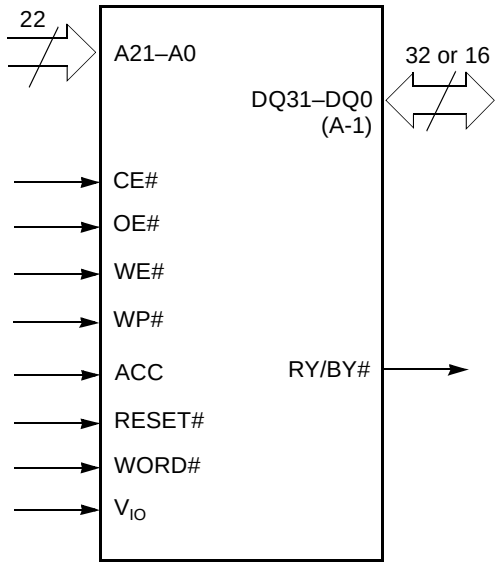
Special handling is required for Flash Memory products in BGA packages.

Flash memory devices in BGA packages may be damaged if exposed to ultrasonic cleaning methods. The package and/or data integrity may be compromised if the package body is exposed to temperatures above 150°C for prolonged periods of time.

PIN DESCRIPTION

A21–A0	=	22 Addresses
DQ30–DQ0	=	31 Data Inputs/Outputs
DQ31/A-1	=	DQ31 (Data Input/Output, double word mode), A-1 (LSB Address Input, word mode)
CE#	=	Chip Enable
OE#	=	Output Enable
WE#	=	Write Enable
WP#	=	Hardware Write Protect Input
ACC	=	Acceleration Input
RESET#	=	Hardware Reset Pin, Active Low
WORD#	=	Word Enable Input At V_{IL}, selects 16-bit mode, At $V_{IH,}$ selects 32-bit mode
RY/BY#	=	Ready/Busy Output
V_{CC}	=	3.0 Volt-only Single Power Supply (see Product Selector Guide for speed options and voltage supply tolerances)
V_{IO}	=	Output Buffer Power Supply
V_{SS}	=	Device Ground
NC	=	Pin Not Connected Internally
RFU	=	Reserved for Future Use

LOGIC SYMBOL



ORDERING INFORMATION

Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of the following:

Am29PDL128G **70** **PE** **I**

OPTIONAL PROCESSING
Blank = Standard Processing
N = 16-byte ESN devices
(Contact an AMD representative for more information)

TEMPERATURE RANGE
I = Industrial (–40°C to +85°C)
E = Extended (–55°C to +125°C)

PACKAGE TYPE
PE = 80-Ball Fortified Ball Grid Array (**F**BGA)
1 mm pitch, 10 x 15 mm package (LAB080)

SPEED OPTION
See Product Selector Guide and Valid Combinations

DEVICE NUMBER/DESCRIPTION
Am29PDL128G
128 Megabit (8 M x 16-Bit/4 M x 32-Bit) CMOS Flash Memory
3.0 Volt-only Read, Program, and Erase

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.

Valid Combinations for BGA Packages			
Order Number		**Package Marking**	
Am29PDL128G70R	PEI	PDL128G70R	I
Am29PDL128G70		PDL128G70V	
Am29PDL128G80	PEI, PEE	PDL128G80V	I, E
Am29PDL128G90		PDL128G90V	

DEVICE BUS OPERATIONS

This section describes the requirements and use of the device bus operations, which are initiated through the internal command register. The command register itself does not occupy any addressable memory location. The register is a latch used to store the commands, along with the address and data information needed to execute the command. The contents of the register serve as inputs to the internal state machine. The state machine outputs dictate the function of the device. Table 1 lists the device bus operations, the inputs and control levels they require, and the resulting output. The following subsections describe each of these operations in further detail.

Table 1. Am29PDL128G Device Bus Operations

Operation	CE#	OE#	WE#	RESET#	WP#	Addresses (Note 1)	DQ31–DQ16		DQ15–DQ0
							WORD# = V_{IH}	WORD# = V_{IL}	
Read	L	L	H	H	X	A_{IN}	D_{OUT}	DQ30–DQ16 = High-Z, DQ31 = A-1	D_{OUT}
Write	L	H	L	H	X	A_{IN}	D_{IN}		D_{IN}
Standby	V_{CC} ± 0.3 V	X	X	V_{CC} ± 0.3 V	X	X	High-Z	High-Z	High-Z
Output Disable	L	H	H	H	X	X	High-Z	High-Z	High-Z
Reset	X	X	X	L	X	X	High-Z	High-Z	High-Z
Temporary Sector Unprotect (High Voltage)	X	X	X	V_{ID}	X	A_{IN}	D_{IN}	X	D_{IN}

Legend: *L = Logic Low = V_{IL}, H = Logic High = V_{IH}, V_{ID} = 11.5–12.5 V, V_{HH} = 9.0 ± 0.5 V, X = Don't Care, SA = Sector Address, A_{IN} = Address In, D_{IN} = Data In, D_{OUT} = Data Out*

Notes:

1. *Addresses are A21–A0 in double word mode (WORD# = V_{IH}), A21–A-1 in word mode (WORD# = V_{IL}).*
2. *The sector protect and sector unprotect functions may also be implemented via programming equipment. See the "Sector Protection" section.*

Word/Double Word Configuration

The WORD# pin controls whether the device data I/O pins operate in the word or double word configuration. If the WORD# pin is set at V_{IH}, the device is in double word configuration, DQ31–DQ0 are active and controlled by CE# and OE#.

If the WORD# pin is set at V_{IL}, the device is in word configuration, and only data I/O pins DQ15–DQ0 are active and controlled by CE# and OE#. The data I/O pins DQ30–DQ16 are tri-stated, and the DQ31 pin is used as an input for the least significant address bit (LSB) function, which is named A-1.

Requirements for Reading Array Data

To read array data from the outputs, the system must drive the CE# and OE# pins to V_{IL}. CE# is the power control and selects the device. OE# is the output control and gates array data to the output pins. WE# should remain at V_{IH}. The WORD# pin determines whether the device outputs array data in words or double words.

The internal state machine is set for reading array data upon device power-up, or after a hardware reset. This ensures that no spurious alteration of the memory content occurs during the power transition. No command is necessary in this mode to obtain array data. Standard microprocessor read cycles that assert valid addresses on the device address inputs produce valid data on the device data outputs. Each bank remains enabled for read access until the command register contents are altered.

Refer to the AC Read-Only Operations table for timing specifications and to Figure 11 for the timing diagram. I_{CC1} in the DC Characteristics table represents the active current specification for reading array data.

Random Read (Non-Page Read)

Address access time (t_{ACC}) is equal to the delay from stable addresses to valid output data. The chip enable access time (t_{CE}) is the delay from the stable addresses and stable CE# to valid data at the output inputs. The output enable access time is the delay from the falling edge of the OE# to valid data at the output

inputs (assuming the addresses have been stable for at least t_{ACC}–t_{OE} time).

Page Mode Read

The device is capable of fast page mode read and is compatible with the page mode Mask ROM read operation. This mode provides faster read access speed for random locations within a page. The page size of the device is 8 words, or 4 double words, with the appropriate page being selected by the higher address bits A21–A2 and the LSB bits A1–A0 (in the double word mode) and A1 to A-1 (in the word mode) determining the specific word/double word within that page. This is an asynchronous operation with the microprocessor supplying the specific word or double word location.

The random or initial page access is equal to t_{ACC} or t_{CE} and subsequent page read accesses (as long as the locations specified by the microprocessor falls within that page) is equivalent to t_{PACC}. When CE# is deasserted and reasserted for a subsequent access, the access time is t_{ACC} or t_{CE}. Here again, CE# selects the device and OE# is the output control and should be used to gate data to the output inputs if the device is selected. Fast page mode accesses are obtained by keeping A21–A2 constant and changing A1 to A0 to select the specific double word, or changing A1 to A-1 to select the specific word, within that page.

Table 2. Page Select, Double Word Mode

Word	A1	A0
Double Word 0	0	0
Double Word 1	0	1
Double Word 2	1	0
Double Word 3	1	1

Table 3. Page Select, Word Mode

Word	A1	A0	A-1
Word 0	0	0	0
Word 1	0	0	1
Word 2	0	1	0
Word 3	0	1	1
Word 4	1	0	0
Word 5	1	0	1
Word 6	1	1	0
Word 7	1	1	1

Simultaneous Operation

The device is capable of reading data from one bank of memory while a program or erase operation is in progress in another bank of memory (simultaneous operation), in addition to the conventional features (read, program, erase-suspend read, and erase-suspend program). The bank selected can be selected by bank addresses (A21–A19) with zero latency.

The simultaneous operation can execute multi-function mode in the same bank.

Table 4. Bank Select

Bank	A21–A19
Bank 1	000
Bank 2	001, 010, 011
Bank 3	100, 101, 110
Bank 4	111

Writing Commands/Command Sequences

To write a command or command sequence (which includes programming data to the device and erasing sectors of memory), the system must drive WE# and CE# to V_{IL}, and OE# to V_{IH}.

For program operations, the WORD# pin determines whether the device accepts program data in double words or words. Refer to “Word/Double Word Configuration” for more information.

The device features an **Unlock Bypass** mode to facilitate faster programming. Once a bank enters the Unlock Bypass mode, only two write cycles are required to program a double word or word, instead of four. The “Double Word/Word Program Command Sequence” section has details on programming data to the device using both standard and Unlock Bypass command sequences.

An erase operation can erase one sector, multiple sectors, or the entire device. Table 5 indicates the address space that each sector occupies. A “bank address” is the address bits required to uniquely select a bank. Similarly, a “sector address” refers to the address bits required to uniquely select a sector. The “Command Definitions” section has details on erasing a sector or the entire chip, or suspending/resuming the erase operation.

I_{CC2} in the DC Characteristics table represents the active current specification for the write mode. The AC Characteristics section contains timing specification tables and timing diagrams for write operations.

Accelerated Program Operation

The device offers accelerated program operations through the ACC function. This function is primarily intended to allow faster manufacturing throughput at the factory.

If the system asserts V_{HH} on this pin, the device automatically enters the aforementioned Unlock Bypass mode, temporarily unprotects any protected sectors, and uses the higher voltage on the pin to reduce the time required for program operations. The system would use a two-cycle program command sequence as required by the Unlock Bypass mode. Removing V_{HH} from the ACC pin returns the device to normal operation. *Note that V_{HH} must not be asserted on ACC for operations other than accelerated programming, or device damage may result*.

Autoselect Functions

If the system writes the autoselect command sequence, the device enters the autoselect mode. The system can then read autoselect codes from the internal register (which is separate from the memory array) on DQ15–DQ0. Standard read cycle timings apply in this mode. Refer to the Autoselect Mode and Autoselect Command Sequence sections for more information.

Standby Mode

When the system is not reading or writing to the device, it can place the device in the standby mode. In this mode, current consumption is greatly reduced, and the outputs are placed in the high impedance state, independent of the OE# input.

The device enters the CMOS standby mode when the CE# and RESET# pins are both held at V_{CC} ± 0.3 V. (Note that this is a more restricted voltage range than V_{IH}.) If CE# and RESET# are held at V_{IH}, but not within V_{CC} ± 0.3 V, the device will be in the standby mode, but the standby current will be greater. The device requires standard access time (t_{CE}) for read access when the device is in either of these standby modes, before it is ready to read data.

If the device is deselected during erasure or programming, the device draws active current until the operation is completed.

I_{CC3} in the DC Characteristics table represents the CMOS standby current specification.

Automatic Sleep Mode

The automatic sleep mode minimizes Flash device energy consumption. The device automatically enables this mode when addresses remain stable for t_{ACC} + 30 ns. The automatic sleep mode is independent of the CE#, WE#, and OE# control signals. Standard address access timings provide new data when addresses are changed. While in sleep mode, output data is latched and always available to the system. Note that during automatic sleep mode, OE# must be at V_{IH} before the device reduces current to the stated sleep mode specification. I_{CC5} in the DC Characteristics table represents the automatic sleep mode current specification.

RESET#: Hardware Reset Pin

The RESET# pin provides a hardware method of resetting the device to reading array data. When the RESET# pin is driven low for at least a period of t_{RP}, the device immediately terminates any operation in progress, tristates all output pins, and ignores all read/write commands for the duration of the RESET# pulse. The device also resets the internal state machine to reading array data. The operation that was interrupted should be reinitiated once the device is ready to accept another command sequence, to ensure data integrity.

Current is reduced for the duration of the RESET# pulse. When RESET# is held at V_{SS}±0.3 V, the device draws CMOS standby current (I_{CC4}). If RESET# is held at V_{IL} but not within V_{SS}±0.3 V, the standby current will be greater.

The RESET# pin may be tied to the system reset circuitry. A system reset would thus also reset the Flash memory, enabling the system to read the boot-up firmware from the Flash memory.

If RESET# is asserted during a program or erase operation, the RY/BY# pin remains a “0” (busy) until the internal reset operation is complete, which requires a time of t_{READY} (during Embedded Algorithms). The system can thus monitor RY/BY# to determine whether the reset operation is complete. If RESET# is asserted when a program or erase operation is not executing (RY/BY# pin is “1”), the reset operation is completed within a time of t_{READY} (not during Embedded Algorithms). The system can read data t_{RH} after the RESET# pin returns to V_{IH}.

Refer to the AC Characteristics tables for RESET# parameters and to Figure 13 for the timing diagram.

Output Disable Mode

When the OE# input is at V_{IH}, output from the device is disabled. The output pins (except for RY/BY#) are placed in the high impedance state.

Table 5. Sector Address Table

Bank	Sector	Sector Address (A21-A11)	Sector Size (Kwords/ Kdoublewords)	Address Range (x16)	Address Range (x32)
Bank 1	SA0	00000000000	4/2	00000h–00FFFh	000000h–0007FFh
	SA1	00000000001	4/2	01000h–01FFFh	000800h–000FFFh
	SA2	00000000010	4/2	02000h–02FFFh	001000h–0017FFh
	SA3	00000000011	4/2	03000h–03FFFh	001800h–001FFFh
	SA4	00000000100	4/2	04000h–04FFFh	002000h–0027FFh
	SA5	00000000101	4/2	05000h–05FFFh	002800h–002FFFh
	SA6	00000000110	4/2	06000h–06FFFh	003000h–0037FFh
	SA7	00000000111	4/2	07000h–07FFFh	003800h–003FFFh
	SA8	00000001XXX	32/16	08000h–0FFFFh	004000h–007FFFh
	SA9	00000010XXX	32/16	10000h–17FFFh	008000h–00BFFFh
	SA10	00000011XXX	32/16	18000h–1FFFFh	00C000h–00FFFFh
	SA11	00000100XXX	32/16	20000h–27FFFh	010000h–013FFFh
	SA12	00000101XXX	32/16	28000h–2FFFFh	014000h–017FFFh
	SA13	00000110XXX	32/16	30000h–37FFFh	018000h–01BFFFh
	SA14	00000111XXX	32/16	38000h–3FFFFh	01C000h–01FFFFh
	SA15	00001000XXX	32/16	40000h–47FFFh	020000h–023FFFh
	SA16	00001001XXX	32/16	48000h–4FFFFh	024000h–027FFFh
	SA17	00001010XXX	32/16	50000h–57FFFh	028000h–02BFFFh
	SA18	00001011XXX	32/16	58000h–5FFFFh	02C000h–02FFFFh
	SA19	00001100XXX	32/16	60000h–67FFFh	030000h–033FFFh
	SA20	00001101XXX	32/16	68000h–6FFFFh	034000h–037FFFh
	SA21	00001110XXX	32/16	70000h–77FFFh	038000h–03BFFFh
	SA22	00001111XXX	32/16	78000h–7FFFFh	03C000h–03FFFFh
	SA23	00010000XXX	32/16	80000h–87FFFh	040000h–043FFFh
	SA24	00010001XXX	32/16	88000h–8FFFFh	044000h–047FFFh
	SA25	00010010XXX	32/16	90000h–97FFFh	048000h–04BFFFh
	SA26	00010011XXX	32/16	98000h–9FFFFh	04C000h–04FFFFh
	SA27	00010100XXX	32/16	A0000h–A7FFFh	050000h–053FFFh
	SA28	00010101XXX	32/16	A8000h–AFFFFh	054000h–057FFFh
	SA29	00010110XXX	32/16	B0000h–B7FFFh	058000h–05BFFFh
	SA30	00010111XXX	32/16	B8000h–BFFFFh	05C000h–05FFFFh
	SA31	00011000XXX	32/16	C0000h–C7FFFh	060000h–063FFFh
	SA32	00011001XXX	32/16	C8000h–CFFFFh	064000h–067FFFh
	SA33	00011010XXX	32/16	D0000h–D7FFFh	068000h–06BFFFh
	SA34	00011011XXX	32/16	D8000h–DFFFFh	06C000h–06FFFFh
	SA35	00011100XXX	32/16	E0000h–E7FFFh	070000h–073FFFh
	SA36	00011101XXX	32/16	E8000h–EFFFFh	074000h–077FFFh
	SA37	00011110XXX	32/16	F0000h–F7FFFh	078000h–07BFFFh
	SA38	00011111XXX	32/16	F8000h–FFFFFh	07C000–07FFFFh

Table 5. Sector Address Table (Continued)

Bank	Sector	Sector Address (A21-A11)	Sector Size (Kwords/ Kdoublewords)	Address Range (x16)	Address Range (x32)
Bank 2	SA39	00100000XXX	32/16	100000h–107FFFh	080000h–083FFFh
	SA40	00100001XXX	32/16	108000h–10FFFFh	084000h–087FFFh
	SA41	00100010XXX	32/16	110000h–117FFFh	088000h–08BFFFh
	SA42	00100011XXX	32/16	118000h–11FFFFh	08C000h–08FFFFh
	SA43	00100100XXX	32/16	120000h–127FFFh	090000h–093FFFh
	SA44	00100101XXX	32/16	128000h–12FFFFh	094000h–097FFFh
	SA45	00100110XXX	32/16	130000h–137FFFh	098000h–09BFFFh
	SA46	00100111XXX	32/16	138000h–13FFFFh	09C000h–09FFFFh
	SA47	00101000XXX	32/16	140000h–147FFFh	0A0000h–0A3FFFh
	SA48	00101001XXX	32/16	148000h–14FFFFh	0A4000h–0A7FFFh
	SA49	00101010XXX	32/16	150000h–157FFFh	0A8000h–0ABFFFh
	SA50	00101011XXX	32/16	158000h–15FFFFh	0AC000h–0AFFFFh
	SA51	00101100XXX	32/16	160000h–167FFFh	0B0000h–0B3FFFh
	SA52	00101101XXX	32/16	168000h–16FFFFh	0B4000h–0B7FFFh
	SA53	00101110XXX	32/16	170000h–177FFFh	0B8000h–0BBFFFh
	SA54	00101111XXX	32/16	178000h–17FFFFh	0BC000h–0BFFFFh
	SA55	00110000XXX	32/16	180000h–187FFFh	0C0000h–0C3FFFh
	SA56	00110001XXX	32/16	188000h–18FFFFh	0C4000h–0C7FFFh
	SA57	00110010XXX	32/16	190000h–197FFFh	0C8000h–0CBFFFh
	SA58	00110011XXX	32/16	198000h–19FFFFh	0CC000h–0CFFFFh
	SA59	00110100XXX	32/16	1A0000h–1A7FFFh	0D0000h–0D3FFFh
	SA60	00110101XXX	32/16	1A8000h–1AFFFFh	0D4000h–0D7FFFh
	SA61	00110110XXX	32/16	1B0000h–1B7FFFh	0D8000h–0DBFFFh
	SA62	00110111XXX	32/16	1B8000h–1BFFFFh	0DC000h–0DFFFFh
	SA63	00111000XXX	32/16	1C0000h–1C7FFFh	0E0000h–0E3FFFh
	SA64	00111001XXX	32/16	1C8000h–1CFFFFh	0E4000h–0E7FFFh
	SA65	00111010XXX	32/16	1D0000h–1D7FFFh	0E8000h–0EBFFFh
	SA66	00111011XXX	32/16	1D8000h–1DFFFFh	0EC000h–0EFFFFh
	SA67	00111100XXX	32/16	1E0000h–1E7FFFh	0F0000h–0F3FFFh
	SA68	00111101XXX	32/16	1E8000h–1EFFFFh	0F4000h–0F7FFFh
	SA69	00111110XXX	32/16	1F0000h–1F7FFFh	0F8000h–0FBFFFh
	SA70	00111111XXX	32/16	1F8000h–1FFFFFh	0FC000h–0FFFFFh
	SA71	01000000XXX	32/16	200000h–207FFFh	100000h–103FFFh
	SA72	01000001XXX	32/16	208000h–20FFFFh	104000h–107FFFh
	SA73	01000010XXX	32/16	210000h–217FFFh	108000h–10BFFFh
	SA74	01000011XXX	32/16	218000h–21FFFFh	10C000h–10FFFFh
	SA75	01000100XXX	32/16	220000h–227FFFh	110000h–113FFFh
	SA76	01000101XXX	32/16	228000h–22FFFFh	114000h–117FFFh
	SA77	01000110XXX	32/16	230000h–237FFFh	118000h–11BFFFh
	SA78	01000111XXX	32/16	238000h–23FFFFh	11C000h–11FFFFh
	SA79	01001000XXX	32/16	240000h–247FFFh	120000h–123FFFh
	SA80	01001001XXX	32/16	248000h–24FFFFh	124000h–127FFFh

Table 5. Sector Address Table (Continued)

Bank	Sector	Sector Address (A21-A11)	Sector Size (Kwords/ Kdoublewords)	Address Range (x16)	Address Range (x32)
Bank 2 (continued)	SA81	01001010XXX	32/16	250000h–257FFFh	128000h–12BFFFh
	SA82	01001011XXX	32/16	258000h–25FFFFh	12C000h–12FFFFh
	SA83	01001100XXX	32/16	260000h–267FFFh	130000h–133FFFh
	SA84	01001101XXX	32/16	268000h–26FFFFh	134000h–137FFFh
	SA85	01001110XXX	32/16	270000h–277FFFh	138000h–13BFFFh
	SA86	01001111XXX	32/16	278000h–27FFFFh	13C000h–13FFFFh
	SA87	01010000XXX	32/16	280000h–287FFFh	140000h–143FFFh
	SA88	01010001XXX	32/16	288000h–28FFFFh	144000h–147FFFh
	SA89	01010010XXX	32/16	290000h–297FFFh	148000h–14BFFFh
	SA90	01010011XXX	32/16	298000h–29FFFFh	14C000h–14FFFFh
	SA91	01010100XXX	32/16	2A0000h–2A7FFFh	150000h–153FFFh
	SA92	01010101XXX	32/16	2A8000h–2AFFFFh	154000h–157FFFh
	SA93	01010110XXX	32/16	2B0000h–2B7FFFh	158000h–15BFFFh
	SA94	01010111XXX	32/16	2B8000h–2BFFFFh	15C000h–15FFFFh
	SA95	01011000XXX	32/16	2C0000h–2C7FFFh	160000h–163FFFh
	SA96	01011001XXX	32/16	2C8000h–2CFFFFh	164000h–167FFFh
	SA97	01011010XXX	32/16	2D0000h–2D7FFFh	168000h–16BFFFh
	SA98	01011011XXX	32/16	2D8000h–2DFFFFh	16C000h–16FFFFh
	SA99	01011100XXX	32/16	2E0000h–2E7FFFh	170000h–173FFFh
	SA100	01011101XXX	32/16	2E8000h–2EFFFFh	174000h–177FFFh
	SA101	01011110XXX	32/16	2F0000h–2F7FFFh	178000h–17BFFFh
	SA102	01011111XXX	32/16	2F8000h–2FFFFFh	17C000h–17FFFFh
	SA103	01100000XXX	32/16	300000h–307FFFh	180000h–183FFFh
	SA104	01100001XXX	32/16	308000h–30FFFFh	184000h–187FFFh
	SA105	01100010XXX	32/16	310000h–317FFFh	188000h–18BFFFh
	SA106	01100011XXX	32/16	318000h–31FFFFh	18C000h–18FFFFh
	SA107	01100100XXX	32/16	320000h–327FFFh	190000h–193FFFh
	SA108	01100101XXX	32/16	328000h–32FFFFh	194000h–197FFFh
	SA109	01100110XXX	32/16	330000h–337FFFh	198000h–19BFFFh
	SA110	01100111XXX	32/16	338000h–33FFFFh	19C000h–19FFFFh
	SA111	01101000XXX	32/16	340000h–347FFFh	1A0000h–1A3FFFh
	SA112	01101001XXX	32/16	348000h–34FFFFh	1A4000h–1A7FFFh
	SA113	01101010XXX	32/16	350000h–357FFFh	1A8000h–1ABFFFh
	SA114	01101011XXX	32/16	358000h–35FFFFh	1AC000h–1AFFFFh
	SA115	01101100XXX	32/16	360000h–367FFFh	1B0000h–1B3FFFh
	SA116	01101101XXX	32/16	368000h–36FFFFh	1B4000h–1B7FFFh
	SA117	01101110XXX	32/16	370000h–377FFFh	1B8000h–1BBFFFh
	SA118	01101111XXX	32/16	378000h–37FFFFh	1BC000h–1BFFFFh
	SA119	01110000XXX	32/16	380000h–387FFFh	1C0000h–1C3FFFh

Table 5. Sector Address Table (Continued)

Bank	Sector	Sector Address (A21-A11)	Sector Size (Kwords/ Kdoublewords)	Address Range (x16)	Address Range (x32)
Bank 2 (continued)	SA120	01110001XXX	32/16	388000h–38FFFFh	1C4000h–1C7FFFh
	SA121	01110010XXX	32/16	390000h–397FFFh	1C8000h–1CBFFFh
	SA122	01110011XXX	32/16	398000h–39FFFFh	1CC000h–1CFFFFh
	SA123	01110100XXX	32/16	3A0000h–3A7FFFh	1D0000h–1D3FFFh
	SA124	01110101XXX	32/16	3A8000h–3AFFFFh	1D4000h–1D7FFFh
	SA125	01110110XXX	32/16	3B0000h–3B7FFFh	1D8000h–1DBFFFh
	SA126	01110111XXX	32/16	3B8000h–3BFFFFh	1DC000h–1DFFFFh
	SA127	01111000XXX	32/16	3C0000h–3C7FFFh	1E0000h–1E3FFFh
	SA128	01111001XXX	32/16	3C8000h–3CFFFFh	1E4000h–1E7FFFh
	SA129	01111010XXX	32/16	3D0000h–3D7FFFh	1E8000h–1EBFFFh
	SA130	01111011XXX	32/16	3D8000h–3DFFFFh	1EC000h–1EFFFFh
	SA131	01111100XXX	32/16	3E0000h–3E7FFFh	1F0000h–1F3FFFh
	SA132	01111101XXX	32/16	3E8000h–3EFFFFh	1F4000h–1F7FFFh
	SA133	01111110XXX	32/16	3F0000h–3F7FFFh	1F8000h–1FBFFFh
	SA134	01111111XXX	32/16	3F8000h–3FFFFFh	1FC000h–1FFFFFh
Bank 3	SA135	10000000XXX	32/16	400000h–407FFFh	200000h–203FFFh
	SA136	10000001XXX	32/16	408000h–40FFFFh	204000h–207FFFh
	SA137	10000010XXX	32/16	410000h–417FFFh	208000h–20BFFFh
	SA138	10000011XXX	32/16	418000h–41FFFFh	20C000h–20FFFFh
	SA139	10000100XXX	32/16	420000h–427FFFh	210000h–213FFFh
	SA140	10000101XXX	32/16	428000h–42FFFFh	214000h–217FFFh
	SA141	10000110XXX	32/16	430000h–437FFFh	218000h–21BFFFh
	SA142	10000111XXX	32/16	438000h–43FFFFh	21C000h–21FFFFh
	SA143	10001000XXX	32/16	440000h–447FFFh	220000h–223FFFh
	SA144	10001001XXX	32/16	448000h–44FFFFh	224000h–227FFFh
	SA145	10001010XXX	32/16	450000h–457FFFh	228000h–22BFFFh
	SA146	10001011XXX	32/16	458000h–45FFFFh	22C000h–22FFFFh
	SA147	10001100XXX	32/16	460000h–467FFFh	230000h–233FFFh
	SA148	10001101XXX	32/16	468000h–46FFFFh	234000h–237FFFh
	SA149	10001110XXX	32/16	470000h–477FFFh	238000h–23BFFFh
	SA150	10001111XXX	32/16	478000h–47FFFFh	23C000h–23FFFFh
	SA151	10010000XXX	32/16	480000h–487FFFh	240000h–243FFFh
	SA152	10010001XXX	32/16	488000h–48FFFFh	244000h–247FFFh
	SA153	10010010XXX	32/16	490000h–497FFFh	248000h–24BFFFh
	SA154	10010011XXX	32/16	498000h–49FFFFh	24C000h–24FFFFh
	SA155	10010100XXX	32/16	4A0000h–4A7FFFh	250000h–253FFFh
	SA156	10010101XXX	32/16	4A8000h–4AFFFFh	254000h–257FFFh
	SA157	10010110XXX	32/16	4B0000h–4B7FFFh	258000h–25BFFFh
	SA158	10010111XXX	32/16	A48000h–4BFFFFh	25C000h–25FFFFh

Table 5. Sector Address Table (Continued)

Bank	Sector	Sector Address (A21-A11)	Sector Size (Kwords/ Kdoublewords)	Address Range (x16)	Address Range (x32)
Bank 3 (continued)	SA159	10011000XXX	32/16	4C0000h–4C7FFFh	260000h–263FFFh
	SA160	10011001XXX	32/16	4C8000h–4CFFFFh	264000h–267FFFh
	SA161	10011010XXX	32/16	4D0000h–4D7FFFh	268000h–26BFFFh
	SA162	10011011XXX	32/16	4D8000h–4DFFFFh	26C000h–26FFFFh
	SA163	10011100XXX	32/16	4E0000h–4E7FFFh	270000h–273FFFh
	SA164	10011101XXX	32/16	4E8000h–4EFFFFh	274000h–277FFFh
	SA165	10011110XXX	32/16	4F0000h–4F7FFFh	278000h–27BFFFh
	SA166	10011111XXX	32/16	4F8000h–4FFFFFh	27C000h–27FFFFh
	SA167	10100000XXX	32/16	500000h–507FFFh	280000h–283FFFh
	SA168	10100001XXX	32/16	508000h–50FFFFh	284000h–287FFFh
	SA169	10100010XXX	32/16	510000h–517FFFh	288000h–28BFFFh
	SA170	10100011XXX	32/16	518000h–51FFFFh	28C000h–28FFFFh
	SA171	10100100XXX	32/16	520000h–527FFFh	290000h–293FFFh
	SA172	10100101XXX	32/16	528000h–52FFFFh	294000h–297FFFh
	SA173	10100110XXX	32/16	530000h–537FFFh	298000h–29BFFFh
	SA174	10100111XXX	32/16	538000h–53FFFFh	29C000h–29FFFFh
	SA175	10101000XXX	32/16	540000h–547FFFh	2A0000h–2A3FFFh
	SA176	10101001XXX	32/16	548000h–54FFFFh	2A4000h–2A7FFFh
	SA177	10101010XXX	32/16	550000h–557FFFh	2A8000h–2ABFFFh
	SA178	10101011XXX	32/16	558000h–55FFFFh	2AC000h–2AFFFFh
	SA179	10101100XXX	32/16	560000h–567FFFh	2B0000h–2B3FFFh
	SA180	10101101XXX	32/16	568000h–56FFFFh	2B4000h–2B7FFFh
	SA181	10101110XXX	32/16	570000h–577FFFh	2B8000h–2BBFFFh
	SA182	10101111XXX	32/16	578000h–57FFFFh	2BC000h–2BFFFFh
	SA183	10110000XXX	32/16	580000h–587FFFh	2C0000h–2C3FFFh
	SA184	10110001XXX	32/16	588000h–58FFFFh	2C4000h–2C7FFFh
	SA185	10110010XXX	32/16	590000h–597FFFh	2C8000h–2CBFFFh
	SA186	10110011XXX	32/16	598000h–59FFFFh	2CC000h–2CFFFFh
	SA187	10110100XXX	32/16	5A0000h–5A7FFFh	2D0000h–2D3FFFh
	SA188	10110101XXX	32/16	5A8000h–5AFFFFh	2D4000h–2D7FFFh
	SA189	10110110XXX	32/16	5B0000h–5B7FFFh	2D8000h–2DBFFFh
	SA190	10110111XXX	32/16	5B8000h–5BFFFFh	2DC000h–2DFFFFh
	SA191	10111000XXX	32/16	5C0000h–5C7FFFh	2E0000h–2E3FFFh
	SA192	10111001XXX	32/16	5C8000h–5CFFFFh	2E4000h–2E7FFFh
	SA193	10111010XXX	32/16	5D0000h–5D7FFFh	2E8000h–2EBFFFh
	SA194	10111011XXX	32/16	5D8000h–5DFFFFh	2EC000h–2EFFFFh
	SA195	10111100XXX	32/16	5E0000h–5E7FFFh	2F0000h–2F3FFFh
	SA196	10111101XXX	32/16	5E8000h–5EFFFFh	2F4000h–2F7FFFh
	SA197	10111110XXX	32/16	5F0000h–5F7FFFh	2F8000h–2FBFFFh

Table 5. Sector Address Table (Continued)

Bank	Sector	Sector Address (A21-A11)	Sector Size (Kwords/ Kdoublewords)	Address Range (x16)	Address Range (x32)
Bank 3 (continued)	SA198	10111111XXX	32/16	5F8000h–5FFFFFh	2FC000h–2FFFFFh
	SA199	11000000XXX	32/16	600000h–607FFFh	300000h–303FFFh
	SA200	11000001XXX	32/16	608000h–60FFFFh	304000h–307FFFh
	SA201	11000010XXX	32/16	610000h–617FFFh	308000h–30BFFFh
	SA202	11000011XXX	32/16	618000h–61FFFFh	30C000h–30FFFFh
	SA203	11000100XXX	32/16	620000h–627FFFh	310000h–313FFFh
	SA204	11000101XXX	32/16	628000h–62FFFFh	314000h–317FFFh
	SA205	11000110XXX	32/16	630000h–637FFFh	318000h–31BFFFh
	SA206	11000111XXX	32/16	638000h–63FFFFh	31C000h–31FFFFh
	SA207	11001000XXX	32/16	640000h–647FFFh	320000h–323FFFh
	SA208	11001001XXX	32/16	648000h–64FFFFh	324000h–327FFFh
	SA209	11001010XXX	32/16	650000h–657FFFh	328000h–32BFFFh
	SA210	11001011XXX	32/16	658000h–65FFFFh	32C000h–32FFFFh
	SA211	11001100XXX	32/16	660000h–667FFFh	330000h–333FFFh
	SA212	11001101XXX	32/16	668000h–66FFFFh	334000h–337FFFh
	SA213	11001110XXX	32/16	670000h–677FFFh	338000h–33BFFFh
	SA214	11001111XXX	32/16	678000h–67FFFFh	33C000h–33FFFFh
	SA215	11010000XXX	32/16	680000h–687FFFh	340000h–343FFFh
	SA216	11010001XXX	32/16	688000h–68FFFFh	344000h–347FFFh
	SA217	11010010XXX	32/16	690000h–697FFFh	348000h–34BFFFh
	SA218	11010011XXX	32/16	698000h–69FFFFh	34C000h–34FFFFh
	SA219	11010100XXX	32/16	6A0000h–6A7FFFh	350000h–353FFFh
	SA220	11010101XXX	32/16	6A8000h–6AFFFFh	354000h–357FFFh
	SA221	11010110XXX	32/16	6B0000h–6B7FFFh	358000h–35BFFFh
	SA222	11010111XXX	32/16	6B8000h–6BFFFFh	35C000h–35FFFFh
	SA223	11011000XXX	32/16	6C0000h–6C7FFFh	360000h–363FFFh
	SA224	11011001XXX	32/16	6C8000h–6CFFFFh	364000h–367FFFh
	SA225	11011010XXX	32/16	6D0000h–6D7FFFh	368000h–36BFFFh
	SA226	11011011XXX	32/16	6D8000h–6DFFFFh	36C000h–36FFFFh
	SA227	11011100XXX	32/16	6E0000h–6E7FFFh	370000h–373FFFh
	SA228	11011101XXX	32/16	6E8000h–6EFFFFh	374000h–377FFFh
	SA229	11011110XXX	32/16	6F0000h–6F7FFFh	378000h–37BFFFh
	SA230	11011111XXX	32/16	6F8000h–6FFFFFh	37C000h–37FFFFh

Table 5. Sector Address Table (Continued)

Bank	Sector	Sector Address (A21-A11)	Sector Size (Kwords/ Kdoublewords)	Address Range (x16)	Address Range (x32)
Bank 4	SA231	11100000XXX	32/16	700000h–707FFFh	380000h–383FFFh
	SA232	11100001XXX	32/16	708000h–70FFFFh	384000h–387FFFh
	SA233	11100010XXX	32/16	710000h–717FFFh	388000h–38BFFFh
	SA234	11100011XXX	32/16	718000h–71FFFFh	38C000h–38FFFFh
	SA235	11100100XXX	32/16	720000h–727FFFh	390000h–393FFFh
	SA236	11100101XXX	32/16	728000h–72FFFFh	394000h–397FFFh
	SA237	11100110XXX	32/16	730000h–737FFFh	398000h–39BFFFh
	SA238	11100111XXX	32/16	738000h–73FFFFh	39C000h–39FFFFh
	SA239	11101000XXX	32/16	740000h–747FFFh	3A0000h–3A3FFFh
	SA240	11101001XXX	32/16	748000h–74FFFFh	3A4000h–3A7FFFh
	SA241	11101010XXX	32/16	750000h–757FFFh	3A8000h–3ABFFFh
	SA242	11101011XXX	32/16	758000h–75FFFFh	3AC000h–3AFFFFh
	SA243	11101100XXX	32/16	760000h–767FFFh	3B0000h–3B3FFFh
	SA244	11101101XXX	32/16	768000h–76FFFFh	3B4000h–3B7FFFh
	SA245	11101110XXX	32/16	770000h–777FFFh	3B8000h–3BBFFFh
	SA246	11101111XXX	32/16	778000h–77FFFFh	3BC000h–3BFFFFh
	SA247	11110000XXX	32/16	780000h–787FFFh	3C0000h–3C3FFFh
	SA248	11110001XXX	32/16	788000h–78FFFFh	3C4000h–3C7FFFh
	SA249	11110010XXX	32/16	790000h–797FFFh	3C8000h–3CBFFFh
	SA250	11110011XXX	32/16	798000h–79FFFFh	3CC000h–3CFFFFh
	SA251	11110100XXX	32/16	7A0000h–7A7FFFh	3D0000h–3D3FFFh
	SA252	11110101XXX	32/16	7A8000h–7AFFFFh	3D4000h–3D7FFFh
	SA253	11110110XXX	32/16	7B0000h–7B7FFFh	3D8000h–3DBFFFh
	SA254	11110111XXX	32/16	7B8000h–7BFFFFh	3DC000h–3DFFFFh
	SA255	11111000XXX	32/16	7C0000h–7C7FFFh	3E0000h–3E3FFFh
	SA256	11111001XXX	32/16	7C8000h–7CFFFFh	3E4000h–3E7FFFh
	SA257	11111010XXX	32/16	7D0000h–7D7FFFh	3E8000h–3EBFFFh
	SA258	11111011XXX	32/16	7D8000h–7DFFFFh	3EC000h–3EFFFFh
	SA259	11111100XXX	32/16	7E0000h–7E7FFFh	3F0000h–3F3FFFh
	SA260	11111101XXX	32/16	7E8000h–7EFFFFh	3F4000h–3F7FFFh
	SA261	11111110XXX	32/16	7F0000h–7F7FFFh	3F8000h–3FBFFFh
	SA262	11111111000	4/2	7F8000h–7F8FFFh	3FC000h–3FC7FFh
	SA263	11111111001	4/2	7F9000h–7F9FFFh	3FC800h–3FCFFFh
	SA264	11111111010	4/2	7FA000h–7FAFFFh	3FD000h–3FD7FFh
	SA265	11111111011	4/2	7FB000h–7FBFFFh	3FD800h–3FDFFFh
	SA266	11111111100	4/2	7FC000h–7FCFFFh	3FE000h–3FE7FFh
	SA267	11111111101	4/2	7FD000h–7FDFFFh	3FE800h–3FEFFFh
	SA268	11111111110	4/2	7FE000h–7FEFFFh	3FF000h–3FF7FFh
	SA269	11111111111	4/2	7FF000h–7FFFFFh	3FF800h–3FFFFFh

Note: *The address range is A21:A-1 in word mode (WORD#=V_{IL}) or A21:A0 in double word mode (WORD#=V_{IH}). Address bits A21:A11 uniquely select a sector; address bits A21:A19 uniquely select a bank.*

Table 6. SecSi™ Sector Addresses

Device	Sector Size	(x32) Address Range	(x16) Address Range
Am29PDL128G	128 words/64 double words	000000h–00003Fh	000000h–00007Fh

Autoselect Mode

The autoselect mode provides manufacturer and device identification, and sector protection verification, through identifier codes output on DQ7–DQ0. This mode is primarily intended for programming equipment to automatically match a device to be programmed with its corresponding programming algorithm. However, the autoselect codes can also be accessed in-system through the command register.

When using programming equipment, the autoselect mode requires V_{ID} on address pin A9. Address pins must be as shown in Table 7. In addition, when verifying sector protection, the sector address must appear on the appropriate highest order address bits (see Table 5). Table 7 shows the remaining address bits that are don't care. When all necessary bits have been set as required, the programming equipment may then read the corresponding identifier code on DQ7–DQ0. However, the autoselect codes can also be accessed in-system through the command register, for instances when the device is erased or programmed in a system without access to high voltage on the A9 pin. The command sequence is illustrated in Tables 14 and 16. *Note that if a Bank Address (BA) on address bits A21, A20, and A19 is asserted during the third write cycle of the autoselect command, the host system can read autoselect data that bank and then immediately read array data from the other bank, without exiting the autoselect mode.*

To access the autoselect codes in-system, the host system can issue the autoselect command via the command register, as shown in Tables 14 and 16. This method does not require V_{ID}. Refer to the Autoselect Command Sequence section for more information.

Table 7. Autoselect Codes (High Voltage Method)

Description		CE#	OE#	WE#	A21 to A11	A10	A9	A8	A7	A6	A5 to A4	A3	A2	A1	A0	DQ31 to DQ8 (Word/Double Word)	DQ7 to DQ0
Manufacturer ID: AMD		L	L	H	X	X	V_{ID}	X	X	L	X	L	L	L	L	000000h	01h
Device ID	Read Cycle 1	L	L	H	X	X	V_{ID}	X	L	L	L	L	L	L	H	22h/ 222222h	7Eh
	Read Cycle 2									L		H	H	H	L	22h/ 222222h	0Dh
	Read Cycle 3									L		H	H	H	H	22h/ 222222h	00h
Sector Protection Verification		L	L	H	SA	X	V_{ID}	X	L	L	L	L	L	H	L	00h/ 000000h	01h (protected), 00h (unprotected)
SecSi Indicator Bit (DQ7)		L	L	H	X	X	V_{ID}	X	X	L	X	L	L	H	H	00h/ 000000h	80h (factory locked), 00h (not factory locked)

Legend: *L = Logic Low = V_{IL}, H = Logic High = V_{IH}, BA = Bank Address, SA = Sector Address, X = Don't care.*

Note: *The autoselect codes may also be accessed in-system via command sequences.*

Table 8. Sector Block Addresses for Protection/Unprotection

Sector Group	A21	A20	A19	A18	A17	A16	A15	A14	A13	A12	A11	Sectors
SGA0	0	0	0	0	0	0	0	0	0	0	0	SA0
SGA1	0	0	0	0	0	0	0	0	0	0	1	SA1
SGA2	0	0	0	0	0	0	0	0	0	1	0	SA2
SGA3	0	0	0	0	0	0	0	0	0	1	1	SA3
SGA4	0	0	0	0	0	0	0	0	1	0	0	SA4
SGA5	0	0	0	0	0	0	0	0	1	0	1	SA5
SGA6	0	0	0	0	0	0	0	0	1	1	0	SA6
SGA7	0	0	0	0	0	0	0	0	1	1	1	SA7
SGA8	0	0	0	0	0	0	0	1	X	X	X	SA8 to SA10
							1	0				
							1	1				
SGA9	0	0	0	0	0	1	X	X	X	X	X	SA11 to SA14
SGA10	0	0	0	0	1	0	X	X	X	X	X	SA15 to SA18
SGA11	0	0	0	0	1	1	X	X	X	X	X	SA19 to SA22
SGA12	0	0	0	1	0	0	X	X	X	X	X	SA23 to SA26
SGA13	0	0	0	1	0	1	X	X	X	X	X	SA27 to SA30
SGA14	0	0	0	1	1	0	X	X	X	X	X	SA31 to SA34
SGA15	0	0	0	1	1	1	X	X	X	X	X	SA35 to SA38
SGA16	0	0	1	0	0	0	X	X	X	X	X	SA39 to SA42
SGA17	0	0	1	0	0	1	X	X	X	X	X	SA43 to SA46
SGA18	0	0	1	0	1	0	X	X	X	X	X	SA47 to SA50
SGA19	0	0	1	0	1	1	X	X	X	X	X	SA51 to SA54
SGA20	0	0	1	1	0	0	X	X	X	X	X	SA55 to SA58
SGA21	0	0	1	1	0	1	X	X	X	X	X	SA59 to SA62
SGA22	0	0	1	1	1	0	X	X	X	X	X	SA63 to SA66
SGA23	0	0	1	1	1	1	X	X	X	X	X	SA67 to SA70
SGA24	0	1	0	0	0	0	X	X	X	X	X	SA71 to SA74
SGA25	0	1	0	0	0	1	X	X	X	X	X	SA75 to SA78
SGA26	0	1	0	0	1	0	X	X	X	X	X	SA79 to SA82
SGA27	0	1	0	0	1	1	X	X	X	X	X	SA83 to SA86
SGA28	0	1	0	1	0	0	X	X	X	X	X	SA87 to SA90
SGA29	0	1	0	1	0	1	X	X	X	X	X	SA91 to SA94
SGA30	0	1	0	1	1	0	X	X	X	X	X	SA95 to SA98
SGA31	0	1	0	1	1	1	X	X	X	X	X	SA99 to SA102

Table 8. Sector Block Addresses for Protection/Unprotection (Continued)

Sector Group	A21	A20	A19	A18	A17	A16	A15	A14	A13	A12	A11	Sectors
SGA32	0	1	1	0	0	0	X	X	X	X	X	SA103 to SA106
SGA33	0	1	1	0	0	1	X	X	X	X	X	SA107 to SA110
SGA34	0	1	1	0	1	0	X	X	X	X	X	SA111 to SA114
SGA35	0	1	1	0	1	1	X	X	X	X	X	SA115 to SA118
SGA36	0	1	1	1	0	0	X	X	X	X	X	SA119 to SA122
SGA37	0	1	1	1	0	1	X	X	X	X	X	SA123 to SA126
SGA38	0	1	1	1	1	0	X	X	X	X	X	SA127 to SA130
SGA39	0	1	1	1	1	1	X	X	X	X	X	SA131 to SA134
SGA40	1	0	0	0	0	0	X	X	X	X	X	SA135 to SA138
SGA41	1	0	0	0	0	1	X	X	X	X	X	SA139 to SA142
SGA42	1	0	0	0	1	0	X	X	X	X	X	SA143 to SA146
SGA43	1	0	0	0	1	1	X	X	X	X	X	SA147 to SA150
SGA44	1	0	0	1	0	0	X	X	X	X	X	SA151 to SA154
SGA45	1	0	0	1	0	1	X	X	X	X	X	SA155 to SA158
SGA46	1	0	0	1	1	0	X	X	X	X	X	SA159 to SA162
SGA47	1	0	0	1	1	1	X	X	X	X	X	SA163 to SA166
SGA48	1	0	1	0	0	0	X	X	X	X	X	SA167 to SA170
SGA49	1	0	1	0	0	1	X	X	X	X	X	SA171 to SA174
SGA50	1	0	1	0	1	0	X	X	X	X	X	SA175 to SA178
SGA51	1	0	1	0	1	1	X	X	X	X	X	SA179 to SA182
SGA52	1	0	1	1	0	0	X	X	X	X	X	SA183 to SA186
SGA53	1	0	1	1	0	1	X	X	X	X	X	SA187 to SA190
SGA54	1	0	1	1	1	0	X	X	X	X	X	SA191 to SA194
SGA55	1	0	1	1	1	1	X	X	X	X	X	SA195 to SA198
SGA56	1	1	0	0	0	0	X	X	X	X	X	SA199 to SA202
SGA57	1	1	0	0	0	1	X	X	X	X	X	SA203 to SA206
SGA58	1	1	0	0	1	0	X	X	X	X	X	SA207 to SA210
SGA59	1	1	0	0	1	1	X	X	X	X	X	SA211 to SA214
SGA60	1	1	0	1	0	0	X	X	X	X	X	SA215 to SA218
SGA61	1	1	0	1	0	1	X	X	X	X	X	SA219 to SA222
SGA62	1	1	0	1	1	0	X	X	X	X	X	SA223 to SA226
SGA63	1	1	0	1	1	1	X	X	X	X	X	SA227 to SA230
SGA64	1	1	1	0	0	0	X	X	X	X	X	SA231 to SA234
SGA65	1	1	1	0	0	1	X	X	X	X	X	SA235 to SA238

Table 8. Sector Block Addresses for Protection/Unprotection (Continued)

Sector Group	A21	A20	A19	A18	A17	A16	A15	A14	A13	A12	A11	Sectors
SGA66	1	1	1	0	1	0	X	X	X	X	X	SA239 to SA242
SGA67	1	1	1	0	1	1	X	X	X	X	X	SA243 to SA246
SGA68	1	1	1	1	0	0	X	X	X	X	X	SA247 to SA250
SGA69	1	1	1	1	0	1	X	X	X	X	X	SA251 to SA254
SGA70	1	1	1	1	1	0	X	X	X	X	X	SA255 to SA258
SGA71	1	1	1	1	1	1	0	0	X	X	X	SA259 to SA261
							0	1				
							1	0				
SGA72	1	1	1	1	1	1	1	1	0	0	0	SA262
SGA73	1	1	1	1	1	1	1	1	0	0	1	SA263
SGA74	1	1	1	1	1	1	1	1	0	1	0	SA264
SGA75	1	1	1	1	1	1	1	1	0	1	1	SA265
SGA76	1	1	1	1	1	1	1	1	1	0	0	SA266
SGA77	1	1	1	1	1	1	1	1	1	0	1	SA267
SGA78	1	1	1	1	1	1	1	1	1	1	0	SA268
SGA79	1	1	1	1	1	1	1	1	1	1	1	SA269

SECTOR PROTECTION

The Am29PDL128G features several levels of sector protection, which can disable both the program and erase operations in certain sectors or sector groups:

Persistent Sector Protection

A command sector protection method that replaces the old 12 V controlled protection method.

Password Sector Protection

A highly sophisticated protection method that requires a password before changes to certain sectors or sector groups are permitted

WP# Hardware Protection

A write protect pin that can prevent program or erase operations in sectors 0, 1, 268, and 269.

All parts default to operate in the Persistent Sector Protection mode. The customer must then choose if the Persistent or Password Protection method is most desirable. There are two one-time programmable non-volatile bits that define which sector protection method will be used. If the customer decides to continue using the Persistent Sector Protection method, they must set the **Persistent Sector Protection Mode Locking Bit**. This will permanently set the part to operate only using Persistent Sector Protection. If the customer decides to use the password method, they must set the **Password Mode Locking Bit**. This will permanently set the part to operate only using password sector protection.

It is important to remember that setting either the **Persistent Sector Protection Mode Locking Bit** or the **Password Mode Locking Bit** permanently selects the protection mode. It is not possible to switch between the two methods once a locking bit has been set. **It is important that one mode is explicitly selected when the device is first programmed, rather than relying on the default mode alone.** This is so that it is not possible for a system program or virus to later set the Password Mode Locking Bit, which would cause an unexpected shift from the default Persistent Sector Protection Mode into the Password Protection Mode.

The WP# Hardware Protection feature is always available, independent of the software managed protection method chosen.

The device is shipped with all sectors unprotected. AMD offers the option of programming and protecting sectors at the factory prior to shipping the device through AMD's ExpressFlash™ Service. Contact an AMD representative for details.

It is possible to determine whether a sector is protected or unprotected. See Autoselect Mode for details.

Persistent Sector Protection

The Persistent Sector Protection method replaces the old 12 V controlled protection method while at the same time enhancing flexibility by providing three different sector protection states:

- **Persistently Locked**—A sector is protected and cannot be changed.
- **Dynamically Locked**—The sector is protected and can be changed by a simple command
- **Unlocked**—The sector is unprotected and can be changed by a simple command

In order to achieve these states, three types of “bits” are going to be used:

Persistent Protection Bit (PPB)

A single Persistent (non-volatile) Protection Bit is assigned to a maximum four sectors (see the sector address tables for specific sector protection groupings). All 8 Kbyte boot-block sectors have individual sector Persistent Protection Bits (PPBs) for greater flexibility. Each PPB is individually modifiable through the **PPB Write Command**.

Note: If a PPB requires erasure, all of the sector PPBs must first be preprogrammed prior to PPB erasing. All PPBs erase in parallel, unlike programming where individual PPBs are programmable. It is the responsibility of the user to perform the preprogramming operation. Otherwise, an already erased sector PPBs has the potential of being over-erased. There is no hardware mechanism to prevent sector PPBs over-erasure.

Persistent Protection Bit Lock (PPB Lock)

A global volatile bit. When set to “1”, the PPBs cannot be changed. When cleared (“0”), the PPBs are changeable. There is only one PPB Lock bit per device. The PPB Lock is cleared after power-up or hardware reset. There is no command sequence to unlock the PPB Lock.

Dynamic Protection Bit (DPB)

A volatile protection bit is assigned for each sector. After power-up or hardware reset, the contents of all DPBs is “0”. Each DPB is individually modifiable through the DPB Write Command.

When the parts are first shipped, the PPBs are cleared, the DPBs are cleared, and PPB Lock is defaulted to power up in the cleared state – meaning the PPBs are changeable.

When the device is first powered on the DPBs power up cleared (sectors not protected). The Protection State for each sector is determined by the logical OR of the PPB and the DPB related to that sector. For the sectors that have the PPBs cleared, the DPBs control whether or not the sector is protected or unprotected. By issuing the DPB Write command sequences, the DPBs will be set or cleared, thus placing each sector in the protected or unprotected state. These are the so-called **Dynamic Locked or Unlocked** states. They are called dynamic states because it is very easy to switch back and forth between the protected and unprotected conditions. This allows software to easily protect sectors against inadvertent changes yet does not prevent the easy removal of protection when changes are needed. The DPBs maybe set or cleared as often as needed.

The PPBs allow for a more static, and difficult to change, level of protection. The PPBs retain their state across power cycles because they are Non-Volatile. Individual PPBs are set with a command but must all be cleared as a group through a complex sequence of program and erasing commands. The PPBs are also limited to 100 erase cycles.

The PPB Lock bit adds an additional level of protection. Once all PPBs are programmed to the desired settings, the PPB Lock may be set to “1”. Setting the PPB Lock disables all program and erase commands to the Non-Volatile PPBs. In effect, the PPB Lock Bit locks the PPBs into their current state. The only way to clear the PPB Lock is to go through a power cycle. System boot code can determine if any changes to the PPB are needed e.g. to allow new system code to be downloaded. If no changes are needed then the boot code can set the PPB Lock to disable any further changes to the PBBs during system operation.

The WP# protects the top two and bottom two sectors when at V_{IL}. These sectors generally hold system boot code. The WP# pin can prevent any changes to the boot code that could override the choices made while setting up sector protection during system initialization.

It is possible to have sectors that have been persistently locked, and sectors that are left in the dynamic state. The sectors in the dynamic state are all unprotected. If there is a need to protect some of them, a simple DPB Write command sequence is all that is necessary. The DPB write command for the dynamic sectors switch the DPBs to signify protected and unprotected, respectively. If there is a need to change the status of the persistently locked sectors, a few more steps are required. First, the PPB Lock bit must be disabled by either putting the device through a power-cycle, or hardware reset. The PPBs can then be changed to reflect the desired settings. Setting the

PPB lock bit once again will lock the PPBs, and the device operates normally again.

Note: to achieve the best protection, it's recommended to execute the PPB lock bit set command early in the boot code, and protect the boot code by holding WP# = V_{IL}.

Table 9. Sector Protection Schemes

DPB	PPB	PPB Lock	Sector State
0	0	0	Unprotected—PPB and DPB are changeable
0	0	1	
0	1	0	Protected—PPB and DPB are changeable
1	0	0	
1	1	0	
0	1	1	Protected—PPB not changeable, DPB is changeable
1	0	1	
1	1	1	

Table 9 contains all possible combinations of the DPB, PPB, and PPB lock relating to the status of the sector.

In summary, if the PPB is set, and the PPB lock is set, the sector is protected and the protection can not be removed until the next power cycle clears the PPB lock. If the PPB is cleared, the sector can be dynamically locked or unlocked. The DPB then controls whether or not the sector is protected or unprotected.

If the user attempts to program or erase a protected sector, the device ignores the command and returns to read mode. A program command to a protected sector enables status polling for approximately 1 µs before the device returns to read mode without having modified the contents of the protected sector. An erase command to a protected sector enables status polling for approximately 50 µs after which the device returns to read mode without having erased the protected sector.

The programming of the DPB, PPB, and PPB lock for a given sector can be verified by writing a DPB/PPB/PPB lock verify command to the device.

Persistent Sector Protection Mode Locking Bit

Like the password mode locking bit, a Persistent Sector Protection mode locking bit exists to guarantee that the device remain in software sector protection. Once set, the Persistent Sector Protection locking bit prevents programming of the password protection mode locking bit. This guarantees that a hacker could not place the device in password protection mode.

Password Protection Mode

The Password Sector Protection Mode method allows an even higher level of security than the Persistent Sector Protection Mode. There are two main differences between the Persistent Sector Protection and the Password Sector Protection Mode:

- When the device is first powered on, or comes out of a reset cycle, the PPB Lock bit set to the **locked state**, rather than cleared to the unlocked state.
- The only means to clear the PPB Lock bit is by writing a unique **64-bit Password** to the device.

The Password Sector Protection method is otherwise identical to the Persistent Sector Protection method.

A 64-bit password is the only additional tool utilized in this method.

The password is stored in the first eight bytes of the SecSi Sector. Once the Password Mode Locking Bit is set, the password is permanently set with no means to read, program, or erase it. The password is used to clear the PPB Lock bit. The Password Unlock command must be written to the flash, along with a password. The flash device internally compares the given password with the pre-programmed password. If they match, the PPB Lock bit is cleared, and the PPBs can be altered. If they do not match, the flash device does nothing. There is a built-in 2 µs delay for each "password check." This delay is intended to thwart any efforts to run a program that tries all possible combinations in order to crack the password.

Because the password occupies the first eight bytes of the SecSi Sector, the password must be programmed before either the password protection mode is selected or the SecSi Sector protection bit is programmed (to use both the SecSi Sector and Password Protection at the same time). See Utilizing Password and SecSi Sector Concurrently for more information.

Password and Password Mode Locking Bit

In order to select the Password sector protection scheme, the customer must first program the password. AMD recommends that the password be somehow correlated to the unique Electronic Serial Number (ESN) of the particular flash device. Each ESN is different for every flash device; therefore each password should be different for every flash device. While programming in the password region, the customer may perform Password Verify operations.

Once the desired password is programmed in, the customer must then set the Password Mode Locking Bit. This operation achieves two objectives:

1. It permanently sets the device to operate using the Password Protection Mode. It is not possible to reverse this function.
2. It also disables *all further commands* to the password region. All program, and read operations are ignored.

Both of these objectives are important, and if not carefully considered, may lead to unrecoverable errors. The user must be sure that the Password Protection method is desired when setting the Password Mode Locking Bit. More importantly, the user must be sure that the password is correct when the Password Mode Locking Bit is set. Due to the fact that read operations are disabled, there is no means to verify what the password is afterwards. If the password is lost after setting the Password Mode Locking Bit, there will be no way to clear the PPB Lock bit.

The Password Mode Locking Bit, once set, prevents reading the 64-bit password on the DQ bus and further password programming. The Password Mode Locking Bit is not erasable. Once Password Mode Locking Bit is programmed, the Persistent Sector Protection Locking Bit is disabled from programming, guaranteeing that no changes to the protection scheme are allowed.

64-bit Password

The 64-bit Password is located in its own memory space and is accessible through the use of the Password Program and Verify commands (see “Password Verify Command”). The password function works in conjunction with the Password Mode Locking Bit, which when set, prevents the Password Verify command from reading the contents of the password on the pins of the device.

Write Protect (WP#)

The Write Protect feature provides a hardware method of protecting sectors 0, 1, 268, and 269 without using V_{ID}. This function is provided by the WP# pin and overrides the previously discussed Sector Protection/Unprotection method.

If the system asserts V_{IL} on the WP# pin, the device disables program and erase functions in sectors 0, 1, 268, and 269 independent of whether it was previously protected or unprotected using High Voltage Sector Protection.

If the system asserts V_{IH} on the WP# pin, the device reverts to whether sectors 0, 1, 268, and 269 were last set to be protected or unprotected. That is, sector protection or unprotection for these sectors depends on whether they were previously protected or unprotected using High Voltage Sector Protection.

Persistent Protection Bit Lock

The Persistent Protection Bit (PPB) Lock is a volatile bit that reflects the state of the Password Mode Locking Bit after power-up reset. If the Password Mode Lock Bit is also set after a hardware reset (RESET# asserted) or a power-up reset. The ONLY means for clearing the PPB Lock Bit in Password Protection Mode is to issue the Password Unlock command. Successful execution of the Password Unlock command clears the PPB Lock Bit, allowing for sector PPBs modifications. Asserting RESET#, taking the device through a power-on reset, or issuing the PPB Lock Bit Set command sets the PPB Lock Bit to a “1” when the Password Mode Lock Bit is not set.

If the Password Mode Locking Bit is not set, including Persistent Protection Mode, the PPB Lock Bit is cleared after power-up or hardware reset. The PPB Lock Bit is set by issuing the PPB Lock Bit Set command. Once set the only means for clearing the PPB Lock Bit is by issuing a hardware or power-up reset. The Password Unlock command is ignored in Persistent Protection Mode.

High Voltage Sector Protection

Sector protection and unprotection may also be implemented using programming equipment. The procedure requires high voltage (V_{ID}) to be placed on the RESET# pin. Refer to Figure 1 for details on this procedure. Note that for sector unprotect, all unprotected sectors must first be protected prior to the first sector write cycle.

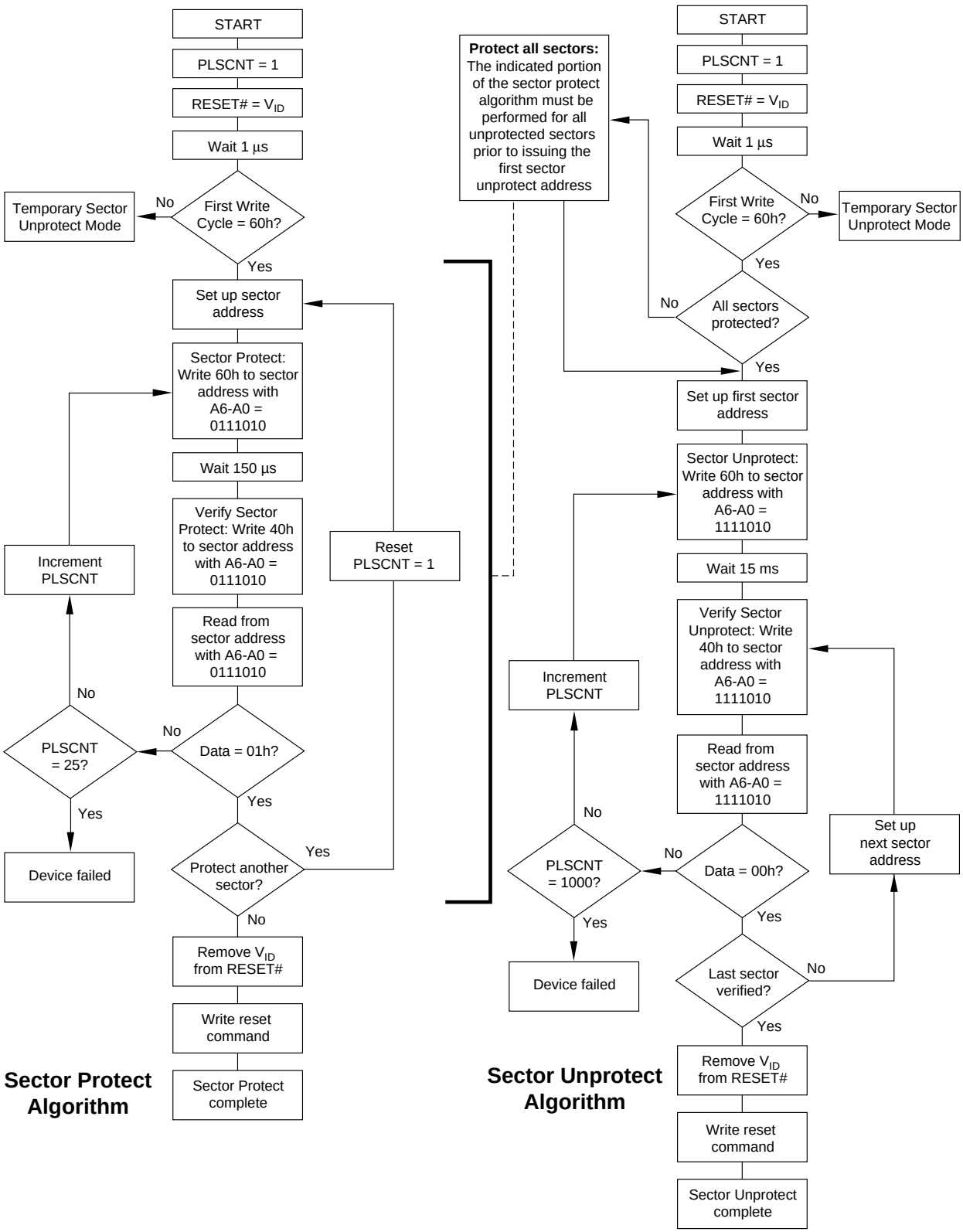
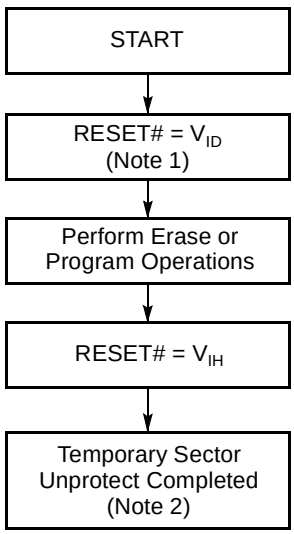


Figure 1. In-System Sector Protection/ Sector Unprotection Algorithms

Temporary Sector Unprotect

This feature allows temporary unprotection of previously protected sectors to change data in-system. The Sector Unprotect mode is activated by setting the RESET# pin to V_{ID}. During this mode, formerly protected sectors can be programmed or erased by selecting the sector addresses. Once V_{ID} is removed from the RESET# pin, all the previously protected sectors are protected again. Figure 2 shows the algorithm, and Figure 23 shows the timing diagrams, for this feature.



Notes:

1. *All protected sectors unprotected (If WP# = V_{IL}, sectors 0, 1, 268, and 269 will remain protected).*
2. *All previously protected sectors are protected once again.*

Figure 2. Temporary Sector Unprotect Operation

SecSi™ (Secured Silicon) Sector Flash Memory Region

The SecSi (Secured Silicon) Sector feature provides a Flash memory region that enables permanent part identification through an Electronic Serial Number (ESN). The SecSi Sector is 128 words (64 double words) in length, and uses a SecSi Sector Indicator Bit (DQ7) to indicate whether or not the SecSi Sector is locked when shipped from the factory. This bit is permanently set at the factory and cannot be changed, which prevents cloning of a factory locked part. This ensures the security of the ESN once the product is shipped to the field.

AMD offers the device with the SecSi Sector either factory locked or customer lockable. The factory-locked version is always protected when shipped from the factory, and has the SecSi Sector Indicator Bit permanently set to a “1.” The customer-lockable version is shipped with the SecSi Sector unprotected, allowing customers to utilize the that sector in any manner they choose. The customer-lockable version has the SecSi Sector Indicator Bit permanently set to a “0.” Thus, the SecSi Sector Indicator Bit prevents customer-lockable devices from being used to replace devices that are factory locked.

The system accesses the SecSi Sector through a command sequence (see Enter SecSi Sector/Exit SecSi Sector Command Sequence). After the system has written the Enter SecSi Sector command sequence, it may read the SecSi Sector by using the addresses normally occupied by the boot sectors. This mode of operation continues until the system issues the Exit SecSi Sector command sequence, or until power is removed from the device. On power-up, or following a hardware reset, the device reverts to sending commands to the normal address space.

Factory Locked: SecSi Sector Programmed and Protected At the Factory

In a factory locked device, the SecSi Sector is protected when the device is shipped from the factory. The SecSi Sector cannot be modified in any way. The device is preprogrammed with both a random number and a secure ESN. The SecSi Sector is located at addresses 000000h–00007Fh in word mode (or 000000h–00003Fh in double word mode). The device is available preprogrammed with one of the following:

- A random, secure ESN only
- Customer code through the ExpressFlash service
- Both a random, secure ESN and customer code through the ExpressFlash service.

Customers may opt to have their code programmed by AMD through the AMD ExpressFlash service. AMD programs the customer’s code, with or without the random ESN. The devices are then shipped from AMD’s factory with the SecSi Sector permanently locked. Contact an AMD representative for details on using AMD’s ExpressFlash service.

Customer Lockable: SecSi Sector NOT Programmed or Protected At the Factory

If the security feature is not required, the SecSi Sector can be treated as an additional Flash memory space. The SecSi Sector can be read any number of times, but can be programmed and locked only once. Note that the accelerated programming (ACC) and unlock bypass functions are not available when programming the SecSi Sector.

The SecSi Sector area can be protected using one of the following procedures:

- Write the three-cycle Enter SecSi Sector Region command sequence, and then follow the in-system sector protect algorithm as shown in Figure 1, except that *RESET# may be at either V_{IH} or V_{ID}*. This allows in-system protection of the SecSi Sector Region without raising any device pin to a high voltage. Note that this method is only applicable to the SecSi Sector.
- Write the three-cycle Enter SecSi Sector Secure Region command sequence, and then use the alternate method of sector protection described in the Sector Protection section.

Once the SecSi Sector is locked and verified, the system must write the Exit SecSi Sector Region command sequence to return to reading and writing the remainder of the array.

The SecSi Sector lock must be used with caution since, once locked, there is no procedure available for unlocking the SecSi Sector area and none of the bits in the SecSi Sector memory space can be modified in any way.

SecSi Sector Protection Bit

The SecSi Sector Protection Bit prevents programming of the SecSi Sector memory area. Once set, the SecSi Sector memory area contents are non-modifiable.

Utilizing Password and SecSi Sector Concurrently

The password must be stored in the first eight bytes of the SecSi Sector. Once the device is permanently locked into the Password Protection Mode, the erase, program, and read operation no longer work on those eight bytes of password in the SecSi Sector. Once the SecSi Sector protection bit is programmed, no location in the SecSi Sector may be programmed. To use both Password Protection and the SecSi Sector concurrently, the user must always program the password into the first eight bytes of the SecSi Sector *before* either the Password Protection Mode is selected or the SecSi Sector protection bit is programmed.

Method 1

1. Enter the SecSi Sector by issuing the SecSi Sector Entry command.
2. Program the 64-bit password by issuing the Password Program and Password Verify commands
3. Lock the password by issuing the Password Protection Mode Locking Bit Program command.
4. Program the SecSi Sector, excluding bytes 0–7.
5. Lock the SecSi Sector by issuing the SecSi Sector Protection Bit Program command.
6. Exit the SecSi Sector by issuing the SecSi Sector Exit or Reset command

Note: *Step 4 may be performed prior to step 2.*

Method 2

1. Enter the SecSi Sector by issuing the SecSi Sector Entry command.
2. Program the entire SecSi Sector, including the first eight bytes contain the 64-bit password.
3. Lock the password by issuing the Password Protection Mode Locking Bit Program command.
4. Lock the SecSi Sector by issuing the SecSi Sector Protection Bit Program command.
5. Exit the SecSi Sector by issuing the SecSi Sector Exit or Reset command

Note: *Step 4 may be performed prior to step 3.*

Hardware Data Protection

The command sequence requirement of unlock cycles for programming or erasing provides data protection against inadvertent writes. In addition, the following hardware data protection measures prevent accidental erasure or programming, which might otherwise be caused by spurious system level signals during V_{CC} power-up and power-down transitions, or from system noise.

Low V_{CC} Write Inhibit

When V_{CC} is less than V_{LKO}, the device does not accept any write cycles. This protects data during V_{CC} power-up and power-down. The command register and all internal program/erase circuits are disabled, and the device resets to the read mode. Subsequent writes are ignored until V_{CC} is greater than V_{LKO}. The system must provide the proper signals to the control pins to prevent unintentional writes when V_{CC} is greater than V_{LKO}.

Write Pulse “Glitch” Protection

Noise pulses of less than 5 ns (typical) on OE#, CE# or WE# do not initiate a write cycle.

Logical Inhibit

Write cycles are inhibited by holding any one of OE# = V_{IL}, CE# = V_{IH} or WE# = V_{IH}. To initiate a write cycle, CE# and WE# must be a logical zero while OE# is a logical one.

Power-Up Write Inhibit

If WE# = CE# = V_{IL} and OE# = V_{IH} during power up, the device does not accept commands on the rising edge of WE#. The internal state machine is automatically reset to the read mode on power-up.

COMMON FLASH MEMORY INTERFACE (CFI)

The Common Flash Interface (CFI) specification outlines device and host system software interrogation handshake, which allows specific vendor-specified software algorithms to be used for entire families of devices. Software support can then be device-independent, JEDEC ID-independent, and forward- and backward-compatible for the specified flash device families. Flash vendors can standardize their existing interfaces for long-term compatibility.

This device enters the CFI Query mode when the system writes the CFI Query command, 98h, to address 55h in word mode (or address AAh in byte mode), any time the device is ready to read array data. The system can read CFI information at the addresses given in Tables 10–13. To terminate reading CFI data, the system must write the reset command. The CFI Query mode is not accessible when the device is executing an Embedded Program or embedded Erase algorithm.

The system can also write the CFI query command when the device is in the autoselect mode. The device enters the CFI query mode, and the system can read CFI data at the addresses given in Tables 10–13. The system must write the reset command to return the device to the autoselect mode.

For further information, please refer to the CFI Specification and CFI Publication 100, available via the World Wide Web at http://www.amd.com/products/nvd/overview/cfi.html. Alternatively, contact an AMD representative for copies of these documents.

Table 10. CFI Query Identification String

Addresses (Double Word Mode)	Addresses (Word Mode)	Data	Description
10h 11h 12h	20h 22h 24h	0051h 0052h 0059h	Query Unique ASCII string “QRY”
13h 14h	26h 28h	0002h 0000h	Primary OEM Command Set
15h 16h	2Ah 2Ch	0040h 0000h	Address for Primary Extended Table
17h 18h	2Eh 30h	0000h 0000h	Alternate OEM Command Set (00h = none exists)
19h 1Ah	32h 34h	0000h 0000h	Address for Alternate OEM Extended Table (00h = none exists)

Table 11. System Interface String

Addresses (Double Word Mode)	Addresses (Word Mode)	Data	Description
1Bh	36h	0027h	V_{CC} Min. (write/erase) D7–D4: volt, D3–D0: 100 millivolt
1Ch	38h	0036h	V_{CC} Max. (write/erase) D7–D4: volt, D3–D0: 100 millivolt
1Dh	3Ah	0000h	V_{PP} Min. voltage (00h = no V_{PP} pin present)
1Eh	3Ch	0000h	V_{PP} Max. voltage (00h = no V_{PP} pin present)
1Fh	3Eh	0004h	Typical timeout per single byte/word write 2^N µs
20h	40h	0000h	Typical timeout for Min. size buffer write 2^N µs (00h = not supported)
21h	42h	000Ah	Typical timeout per individual block erase 2^N ms
22h	44h	0000h	Typical timeout for full chip erase 2^N ms (00h = not supported)
23h	46h	0005h	Max. timeout for byte/word write 2^N times typical
24h	48h	0000h	Max. timeout for buffer write 2^N times typical
25h	4Ah	0004h	Max. timeout per individual block erase 2^N times typical
26h	4Ch	0000h	Max. timeout for full chip erase 2^N times typical (00h = not supported)

Table 12. Device Geometry Definition

Addresses (Double Word Mode)	Addresses (Word Mode)	Data	Description
27h	4Eh	0018h	Device Size = 2^N byte
28h 29h	50h 52h	0005h 0000h	Flash Device Interface description (refer to CFI publication 100)
2Ah 2Bh	54h 56h	0000h 0000h	Max. number of byte in multi-byte write = 2^N (00h = not supported)
2Ch	58h	0003h	Number of Erase Block Regions within device
2Dh 2Eh 2Fh 30h	5Ah 5Ch 5Eh 60h	0007h 0000h 0020h 0000h	Erase Block Region 1 Information (refer to the CFI specification or CFI publication 100)
31h 32h 33h 34h	62h 64h 66h 68h	00FDh 0000h 0000h 0001h	Erase Block Region 2 Information (refer to the CFI specification or CFI publication 100)
35h 36h 37h 38h	6Ah 6Ch 6Eh 70h	0007h 0000h 0020h 0000h	Erase Block Region 3 Information (refer to the CFI specification or CFI publication 100)
39h 3Ah 3Bh 3Ch	72h 74h 76h 78h	0000h 0000h 0000h 0000h	Erase Block Region 4 Information (refer to the CFI specification or CFI publication 100)

Table 13. Primary Vendor-Specific Extended Query

Addresses (Double Word Mode)	Addresses (Word Mode)	Data	Description
40h 41h 42h	80h 82h 84h	0050h 0052h 0049h	Query-unique ASCII string “PRI”
43h	86h	0031h	Major version number, ASCII (reflects modifications to the silicon)
44h	88h	0033h	Minor version number, ASCII (reflects modifications to the CFI table)
45h	8Ah	0004h	Address Sensitive Unlock (Bits 1-0) 0 = Required, 1 = Not Required Silicon Revision Number (Bits 7-2)
46h	8Ch	0002h	Erase Suspend 0 = Not Supported, 1 = To Read Only, 2 = To Read & Write
47h	8Eh	0001h	Sector Protect 0 = Not Supported, X = Number of sectors in per group
48h	90h	0001h	Sector Temporary Unprotect 00 = Not Supported, 01 = Supported
49h	92h	0007h	Sector Protect/Unprotect scheme 01 =29F040 mode, 02 = 29F016 mode, 03 = 29F400, 04 = 29LV800 mode
4Ah	94h	00E7h	Simultaneous Operation 00 = Not Supported, X = Number of Sectors excluding Bank 1
4Bh	96h	0000h	Burst Mode Type 00 = Not Supported, 01 = Supported
4Ch	98h	0002h	Page Mode Type 00 = Not Supported, 01 = 4 Word Page, 02 = 8 Word Page
4Dh	9Ah	00B5h	ACC (Acceleration) Supply Minimum 00h = Not Supported, D7-D4: Volt, D3-D0: 100 mV
4Eh	9Ch	0005h	ACC (Acceleration) Supply Maximum 00h = Not Supported, D7-D4: Volt, D3-D0: 100 mV
4Fh	9Eh	0001h	Top/Bottom Boot Sector Flag 00h = Uniform device, 01h = Uniform, 8 x 8 Kbit Top and Bottom, 02h = Bottom Boot Device, 03h = Top Boot Device, 04h = Both Top and Bottom
50h	A0h	0000h	Program Suspend 0 = Not supported, 1 = Supported
57h	AEh	0004h	Bank Organization 00 = Data at 4Ah is zero, X = Number of Banks
58h	B0h	*0027h	Bank 1 Region Information X = Number of Sectors in Bank 1
59h	B2h	*0060h	Bank 2 Region Information X = Number of Sectors in Bank 2
5Ah	B4h	*0060h	Bank 3 Region Information X = Number of Sectors in Bank 3
5Bh	B6h	0027h	Bank 4 Region Information X = Number of Sectors in Bank 4

COMMAND DEFINITIONS

Writing specific address and data commands or sequences into the command register initiates device operations. Tables 14–17 define the valid register command sequences. Writing **incorrect address and data values** or writing them in the **improper sequence** resets the device to reading array data.

All addresses are latched on the falling edge of WE# or CE#, whichever happens later. All data is latched on the rising edge of WE# or CE#, whichever happens first. Refer to the AC Characteristics section for timing diagrams.

Reading Array Data

The device is automatically set to reading array data after device power-up. No commands are required to retrieve data. Each bank is ready to read array data after completing an Embedded Program or Embedded Erase algorithm.

After the device accepts an Erase Suspend command, the corresponding bank enters the erase-suspend-read mode, after which the system can read data from any non-erase-suspended sector within the same bank. The system can read array data using the standard read timing, except that if it reads at an address within erase-suspended sectors, the device outputs status data. After completing a programming operation in the Erase Suspend mode, the system may once again read array data with the same exception. See the Erase Suspend/Erase Resume Commands section for more information.

The system *must* issue the reset command to return a bank to the read (or erase-suspend-read) mode if DQ5 goes high during an active program or erase operation, or if the bank is in the autoselect mode. See the next section, Reset Command, for more information.

See also Requirements for Reading Array Data in the Device Bus Operations section for more information. The Read-Only Operations table provides the read parameters, and Figure 11 shows the timing diagram.

Reset Command

Writing the reset command resets the banks to the read or erase-suspend-read mode. Address bits are don't cares for this command.

The reset command may be written between the sequence cycles in an erase command sequence before erasing begins. This resets the bank to which the system was writing to the read mode. Once erasure begins, however, the device ignores reset commands until the operation is complete.

The reset command may be written between the sequence cycles in a program command sequence before programming begins. This resets the bank to which the system was writing to the read mode. If the program command sequence is written to a bank that is in the Erase Suspend mode, writing the reset command returns that bank to the erase-suspend-read mode. Once programming begins, however, the device ignores reset commands until the operation is complete.

The reset command may be written between the sequence cycles in an autoselect command sequence. Once in the autoselect mode, the reset command must be written to return to the read mode. If a bank entered the autoselect mode while in the Erase Suspend mode, writing the reset command returns that bank to the erase-suspend-read mode.

If DQ5 goes high during a program or erase operation, writing the reset command returns the banks to the read mode (or erase-suspend-read mode if that bank was in Erase Suspend).

Autoselect Command Sequence

The autoselect command sequence allows the host system to access the manufacturer and device codes, and determine whether or not a sector is protected. The autoselect command sequence may be written to an address within a bank that is either in the read or erase-suspend-read mode. The autoselect command may not be written while the device is actively programming or erasing in the other bank.

The autoselect command sequence is initiated by first writing two unlock cycles. This is followed by a third write cycle that contains the bank address and the autoselect command. The bank then enters the autoselect mode. The system may read any number of autoselect codes without reinitiating the command sequence.

Tables 14 and 16 show the address and data requirements. To determine sector protection information, the system must write to the appropriate bank address (BA) and sector address (SA). Table 5 shows the address range and bank number associated with each sector.

The system must write the reset command to return to the read mode (or erase-suspend-read mode if the bank was previously in Erase Suspend).

Enter SecSi Sector/Exit SecSi Sector Command Sequence

The SecSi Sector region provides a secured data area containing a random, eight word/four double word electronic serial number (ESN). The system can access the SecSi Sector region by issuing the three-cycle Enter SecSi Sector command sequence. The device continues to access the SecSi Sector region

until the system issues the four-cycle Exit SecSi Sector command sequence. The Exit SecSi Sector command sequence returns the device to normal operation. The SecSi Sector is not accessible when the device is executing an Embedded Program or embedded Erase algorithm. Tables 15 and 17 show the address and data requirements for both command sequences. See also "SecSi™ (Secured Silicon) Sector Flash Memory Region" for further information.

Double Word/Word Program Command Sequence

The system may program the device by double word or word, depending on the state of the WORD# pin. Programming is a four-bus-cycle operation. The program command sequence is initiated by writing two unlock write cycles, followed by the program set-up command. The program address and data are written next, which in turn initiate the Embedded Program algorithm. The system is *not* required to provide further controls or timings. The device automatically provides internally generated program pulses and verifies the programmed cell margin. Tables 14 and 16 show the address and data requirements for the program command sequence.

When the Embedded Program algorithm is complete, that bank then returns to the read mode and addresses are no longer latched. The system can determine the status of the program operation by using DQ7, DQ6, or RY/BY#. Refer to the Write Operation Status section for information on these status bits.

Any commands written to the device during the Embedded Program Algorithm are ignored. Note that a **hardware reset** immediately terminates the program operation. The program command sequence should be reinitiated once that bank has returned to the read mode, to ensure data integrity.

Programming is allowed in any sequence and across sector boundaries. **A bit cannot be programmed from "0" back to a "1."** Attempting to do so may cause that bank to set DQ5 = 1, or cause the DQ7 and DQ6 status bits to indicate the operation was successful. However, a succeeding read will show that the data is still "0." Only erase operations can convert a "0" to a "1."

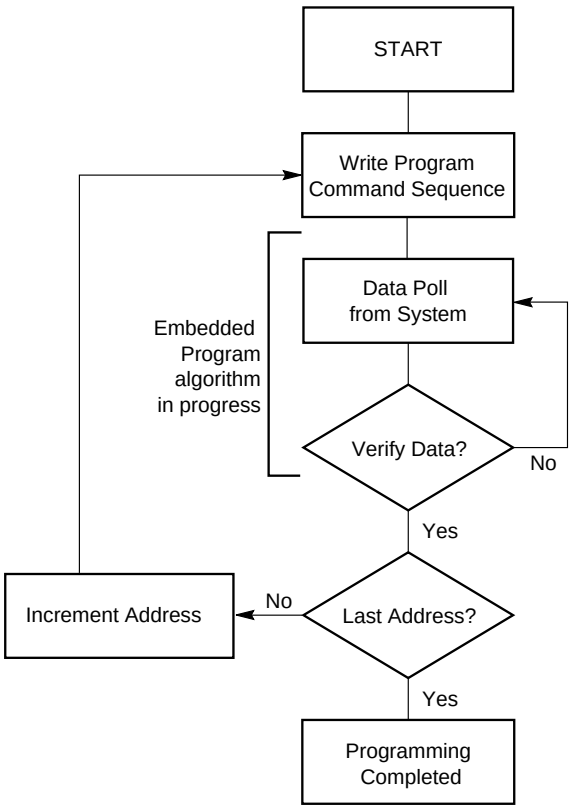
Unlock Bypass Command Sequence

The unlock bypass feature allows the system to program data to a bank faster than using the standard program command sequence. The unlock bypass command sequence is initiated by first writing two unlock cycles. This is followed by a third write cycle containing the unlock bypass command, 20h. That bank then enters the unlock bypass mode. A two-cycle unlock bypass program command sequence is all that is required to program in this mode. The first cycle in this sequence contains the unlock bypass program command, A0h; the second cycle contains the program address and data. Additional data is programmed in the same manner. This mode dispenses with the initial two unlock cycles required in the standard program command sequence, resulting in faster total programming time. Tables 14 and 16 show the requirements for the command sequence.

During the unlock bypass mode, only the Unlock Bypass Program and Unlock Bypass Reset commands are valid. To exit the unlock bypass mode, the system must issue the two-cycle unlock bypass reset command sequence. The first cycle must contain the bank address and the data 90h. The second cycle need only contain the data 00h. The bank then returns to the read mode.

The device offers accelerated program operations through the ACC pin. When the system asserts V_{HH} on the ACC pin, the device automatically enters the Unlock Bypass mode. The system may then write the two-cycle Unlock Bypass program command sequence. The device uses the higher voltage on the ACC pin to accelerate the operation. *Note that the ACC pin must not be at V_{HH} any operation other than accelerated programming, or device damage may result. In addition, the ACC pin must not be left floating or unconnected; inconsistent behavior of the device may resul*t.

Figure 3 illustrates the algorithm for the program operation. Refer to the Erase and Program Operations table in the AC Characteristics section for parameters, and Figure 16 for timing diagrams.



Note: *See Tables 14 and 16 for program command sequence.*

Figure 3. Program Operation

Chip Erase Command Sequence

Chip erase is a six bus cycle operation. The chip erase command sequence is initiated by writing two unlock cycles, followed by a set-up command. Two additional unlock write cycles are then followed by the chip erase command, which in turn invokes the Embedded Erase algorithm. The device does *not* require the system to preprogram prior to erase. The Embedded Erase algorithm automatically preprograms and verifies the entire memory for an all zero data pattern prior to electrical erase. The system is not required to provide any controls or timings during these operations. Tables 14 and 16 show the address and data requirements for the chip erase command sequence.

When the Embedded Erase algorithm is complete, that bank returns to the read mode and addresses are no longer latched. The system can determine the status of the erase operation by using DQ7, DQ6, DQ2, or RY/BY#. Refer to the Write Operation Status section for information on these status bits.

Any commands written during the chip erase operation are ignored. However, note that a **hardware reset** immediately terminates the erase operation. If that occurs, the chip erase command sequence should be reinitiated once that bank has returned to reading array data, to ensure data integrity.

Figure 4 illustrates the algorithm for the erase operation. Refer to the Erase and Program Operations tables in the AC Characteristics section for parameters, and Figure 18 section for timing diagrams.

Sector Erase Command Sequence

Sector erase is a six bus cycle operation. The sector erase command sequence is initiated by writing two unlock cycles, followed by a set-up command. Two additional unlock cycles are written, and are then followed by the address of the sector to be erased, and the sector erase command. Tables 14 and 16 show the address and data requirements for the sector erase command sequence.

The device does *not* require the system to preprogram prior to erase. The Embedded Erase algorithm automatically programs and verifies the entire memory for an all zero data pattern prior to electrical erase. The system is not required to provide any controls or timings during these operations.

After the command sequence is written, a sector erase time-out of 80 µs occurs. During the time-out period, additional sector addresses and sector erase commands may be written. Loading the sector erase buffer may be done in any sequence, and the number of sectors may be from one sector to all sectors. The time between these additional cycles must be less than 80 µs, otherwise erasure may begin. Any sector erase address and command following the exceeded time-out may or may not be accepted. It is recommended that processor interrupts be disabled during this time to ensure all commands are accepted. The interrupts can be re-enabled after the last Sector Erase command is written. **Any command other than Sector Erase or Erase Suspend during the time-out period resets that bank to the read mode.** The system must rewrite the command sequence and any additional addresses and commands.

The system can monitor DQ3 to determine if the sector erase timer has timed out (See the section on DQ3: Sector Erase Timer.). The time-out begins from the rising edge of the final WE# pulse in the command sequence.

When the Embedded Erase algorithm is complete, the bank returns to reading array data and addresses are no longer latched. Note that while the Embedded Erase operation is in progress, the system can read data from the non-erasing bank. The system can determine the status of the erase operation by reading

DQ7, DQ6, DQ2, or RY/BY# in the erasing bank. Refer to the Write Operation Status section for information on these status bits.

Once the sector erase operation has begun, only the Erase Suspend command is valid. All other commands are ignored. However, note that a **hardware reset** immediately terminates the erase operation. If that occurs, the sector erase command sequence should be reinitiated once that bank has returned to reading array data, to ensure data integrity.

Figure 4 illustrates the algorithm for the erase operation. Refer to the Erase and Program Operations tables in the AC Characteristics section for parameters, and Figure 18 section for timing diagrams.

Erase Suspend/Erase Resume Commands

The Erase Suspend command, B0h, allows the system to interrupt a sector erase operation and then read data from, or program data to, any sector not selected for erasure. The bank address is required when writing this command. This command is valid only during the sector erase operation, including the 80 µs time-out period during the sector erase command sequence. The Erase Suspend command is ignored if written during the chip erase operation or Embedded Program algorithm.

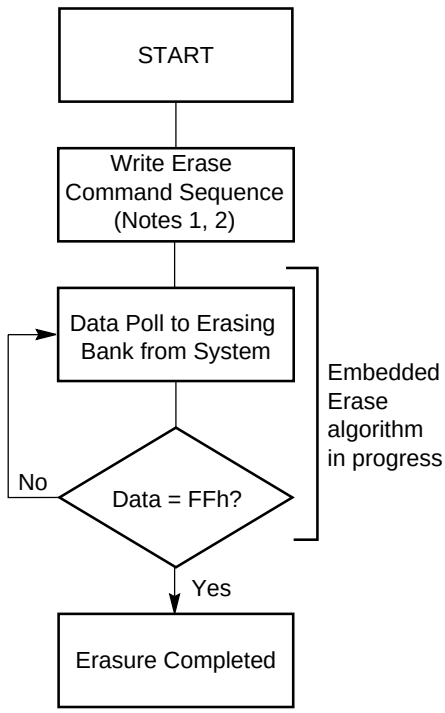
When the Erase Suspend command is written during the sector erase operation, the device requires a maximum of 20 µs to suspend the erase operation. However, when the Erase Suspend command is written during the sector erase time-out, the device immediately terminates the time-out period and suspends the erase operation. Addresses are “don’t-cares” when writing the Erase suspend command.

After the erase operation has been suspended, the bank enters the erase-suspend-read mode. The system can read data from or program data to any sector not selected for erasure. (The device “erase suspends” all sectors selected for erasure.) Reading at any address within erase-suspended sectors produces status information on DQ7–DQ0. The system can use DQ7, or DQ6 and DQ2 together, to determine if a sector is actively erasing or is erase-suspended. Refer to the Write Operation Status section for information on these status bits.

After an erase-suspended program operation is complete, the bank returns to the erase-suspend-read mode. The system can determine the status of the program operation using the DQ7 or DQ6 status bits, just as in the standard Double Word/Word Program operation. Refer to the Write Operation Status section for more information.

In the erase-suspend-read mode, the system can also issue the autoselect command sequence. The device allows reading autoselect codes even at addresses within erasing sectors, since the codes are not stored in the memory array. When the device exits the autoselect mode, the device reverts to the Erase Suspend mode, and is ready for another valid operation. Refer to the Autoselect Mode and Autoselect Command Sequence sections for details.

To resume the sector erase operation, the system must write the Erase Resume command (address bits are don’t care). The bank address of the erase-suspended bank is required when writing this command. Further writes of the Resume command are ignored. Another Erase Suspend command can be written after the chip has resumed erasing.



Notes:

1. *See Tables 14 and 16 for erase command sequence.*
2. *See the section on DQ3 for information on the sector erase timer.*

Figure 4. Erase Operation

Password Program Command

The Password Program Command permits programming the password that is used as part of the hardware protection scheme. The actual password is 64-bits long. Depending upon the state of the WORD# pin, multiple Password Program Commands are required. For a x16 bit data bus, 4 Password Program commands are required to program the password. For

a x32 bit data bus, 2 Password Program commands are required. The user must enter the unlock cycle, password program command (38h) and the program address/data for each portion of the password when programming. There is no special addressing order required for programming the password. Also, when the password is undergoing programming, Simultaneous Operation is disabled. Read operations to any memory location will return the programming status. Once programming is complete, the user must issue a Read/Reset command to return the device to normal operation. Once the Password is written and verified, the Password Mode Locking Bit must be set in order to prevent verification. The Password Program Command is only capable of programming "0"s. Programming a "1" after a cell is programmed as a "0" results in a time-out by the Embedded Program Algorithm™ with the cell remaining as a "0". The password is all F's when shipped from the factory. All 64-bit password combinations are valid as a password.

Password Programming is permitted if the SecSi sector is enabled.

Password Verify Command

The Password Verify Command is used to verify the Password. The Password is verifiable only when the Password Mode Locking Bit is not programmed. If the Password Mode Locking Bit is programmed and the user attempts to verify the Password, the device will always drive all F's onto the DQ data bus.

The Password Verify command is permitted if the SecSi sector is enabled. Also, the device will not operate in Simultaneous Operation when the Password Verify command is executed. Only the password is returned regardless of the bank address. The lower two address bits (A0:A-1) are valid during the Password Verify. Writing the Read/Reset command returns the device back to normal operation.

Password Protection Mode Locking Bit Program Command

The Password Protection Mode Locking Bit Program Command programs the Password Protection Mode Locking Bit, which prevents further verifies or updates to the Password. Once programmed, the Password Protection Mode Locking Bit cannot be erased! If the Password Protection Mode Locking Bit is verified as program without margin, the Password Protection Mode Locking Bit Program command can be executed to improve the program margin. Once the Password Protection Mode Locking Bit is programmed, the Persistent Sector Protection Locking Bit program circuitry is disabled, thereby forcing the device to remain in the Password Protection mode. Exiting the Mode Locking Bit Program command is accomplished by writing the Read/Reset command.

The Password Protection Mode Locking Bit Program command is permitted if the SecSi sector is enabled.

Persistent Sector Protection Mode Locking Bit Program Command

The Persistent Sector Protection Mode Locking Bit Program Command programs the Persistent Sector Protection Mode Locking Bit, which prevents the Password Mode Locking Bit from ever being programmed. If the Persistent Sector Protection Mode Locking Bit is verified as programmed without margin, the Persistent Sector Protection Mode Locking Bit Program Command should be reissued to improve program margin. By disabling the program circuitry of the Password Mode Locking Bit, the device is forced to remain in the Persistent Sector Protection mode of operation, once this bit is set. Exiting the Persistent Protection Mode Locking Bit Program command is accomplished by writing the Read/Reset command.

The Persistent Sector Protection Mode Locking Bit Program command is permitted if the SecSi sector is enabled.

SecSi Sector Protection Bit Program Command

The SecSi Sector Protection Bit Program Command programs the SecSi Sector Protection Bit, which prevents the SecSi sector memory from being cleared. If the SecSi Sector Protection Bit is verified as programmed without margin, the SecSi Sector Protection Bit Program Command should be reissued to improve program margin. Exiting the V_{CC}-level SecSi Sector Protection Bit Program Command is accomplished by writing the Read/Reset command.

The SecSi Sector Protection Bit Program command is permitted if the SecSi sector is enabled.

PPB Lock Bit Set Command

The PPB Lock Bit Set command is used to set the PPB Lock bit if it is cleared either at reset or if the Password Unlock command was successfully executed. There is no PPB Lock Bit Clear command. Once the PPB Lock Bit is set, it cannot be cleared unless the device is taken through a power-on clear or the Password Unlock command is executed. Upon setting the PPB Lock Bit, the PPBs are latched into the DPBs. If the Password Mode Locking Bit is set, the PPB Lock Bit status is reflected as set, even after a power-on reset cycle. In the Persistent Sector Protection mode, exiting the PPB Lock Bit Set command is accomplished by writing the Read/Reset command.

The PPB Lock Bit Set command is permitted if the SecSi sector is enabled.

DPB Write Command

The DPB Write command is used to set or clear a DPB for a given sector. The high order address bits (A21–A11) are issued at the same time as the code 01h or 00h on DQ7-DQ0. All other DQ data bus pins are ignored during the data write cycle. The DPBs are modifiable at any time, regardless of the state of the PPB or PPB Lock Bit. The DPBs are cleared at power-up or hardware reset.Exiting the DPB Write command is accomplished by writing the Read/Reset command.

The DPB Write command is permitted if the SecSi sector is enabled.

Password Unlock Command

The Password Unlock command is used to clear the PPB Lock Bit so that the PPBs can be unlocked for modification, thereby allowing the PPBs to become accessible for modification. The exact password must be entered in order for the unlocking function to occur. This command cannot be issued any faster than 2 µs at a time to prevent a hacker from running through the all 64-bit combinations in an attempt to correctly match a password. If the command is issued before the 2 µs execution window for each portion of the unlock, the command will be ignored.

The Password Unlock function is accomplished by writing Password Unlock command and data to the device to perform the clearing of the PPB Lock Bit. The password is 64 bits long, so the user must write the Password Unlock command 2 times for a x32 bit data bus and 4 times for a x16 data bus.

Once the Password Unlock command is entered, the RY/BY# pin goes LOW indicating that the device is busy. Approximately 2 µs is required for each portion of the unlock. Once the first portion of the password unlock completes (RY/BY# is not driven and DQ6 does not toggle when read), the Password Unlock command is issued again, only this time with the next part of the password. If WORD# = 1, the second Password Unlock command is the final command before the PPB Lock Bit is cleared (assuming a valid password). If WORD# = 0, this is the fourth Password Unlock command. In x16 mode, four Password Unlock commands are required to successfully clear the PPB Lock Bit. As with the first Password Unlock command, the RY/BY# signal goes LOW and reading the device results in the DQ6 pin toggling on successive read operations until complete. It is the responsibility of the microprocessor to keep track of the number of Password Unlock commands (2 for x32 bus and 4 for x16 bus), the order, and when to read the PPB Lock bit to confirm successful password unlock

The Password Unlock command is permitted if the SecSi sector is enabled.

PPB Program Command

The PPB Program command is used to program, or set, a given PPB. Each PPB is individually programmed (but is bulk erased with the other PPBs). The specific sector address (A21–A11) are written at the same time as the program command 60h with A6 = 0. If the PPB Lock Bit is set and the corresponding PPB is set for the sector, the PPB Program command will not execute and the command will time-out without programming the PPB.

After programming a PPB, two additional cycles are needed to determine whether the PPB has been programmed with margin. If the PPB has been programmed without margin, the program command should be reissued to improve the program margin.

The PPB Program command is permitted if the SecSi sector is enabled. The PPB Program command does not follow the Embedded Program algorithm.

All PPB Erase Command

The All PPB Erase command is used to erase all PPBs in bulk. There is no means for individually erasing a specific PPB. Unlike the PPB program, no specific sector address is required. However, when the PPB erase command is written (60h) and A6 = 1, all Sector PPBs are erased in parallel. If the PPB Lock Bit is set the ALL PPB Erase command will not execute and the command will time-out without erasing the PPBs. After erasing the PPBs, two additional cycles are needed to determine whether the PPB has been erased with margin. If the PPBs has been erased without margin, the erase command should be reissued to improve the program margin.

It is the responsibility of the user to preprogram all PPBs prior to issuing the All PPB Erase command. If the user attempts to erase a cleared PPB, over-erasure may occur making it difficult to program the PPB at a later time. Also note that the total number of PPB program/erase cycles is limited to 100 cycles. Cycling the PPBs beyond 100 cycles is not guaranteed.

The All PPB Erase command is permitted if the SecSi sector is enabled.

DPB Write Command

The DPB Write command is used for setting the DPB, which is a volatile bit that is cleared at hardware reset. There is one DPB per sector. If the PPB is set, the sector is protected regardless of the value of the DPB. If the PPB is cleared, setting the DPB to a 1 protects the sector from programs or erases. Since this is a volatile bit, removing power or resetting the device will clear the DPBs. The bank address is latched when the command is written.

The DPB Write command is permitted if the SecSi sector is enabled.

PPB Lock Bit Set Command

The PPB Lock Bit set command is used for setting the PPB lock bit. During Password Protection mode, only the Password Unlock command can reset the PPB Lock Bit to 0. Otherwise, a power-up or hardware reset resets the PPB Lock Bit to 0.

PPB Lock Bit Status Command

The programming of the PPB Lock Bit can be verified by writing a PPB Lock Bit status verify command to the device.

Sector Protection Status Command

The programming of either the PPB or DPB for a given sector or sector group can be verified by writing a Sector Protection Status command to the device.

Note that there is no single command to independently verify the programming of a DPB or PPB for a given sector group.

Command Definitions Tables

Table 14. Memory Array Command Definitions (x32 Mode)

Command (Notes)		Cycles	Bus Cycles (Notes 1–4)											
			Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data
Read (5)		1	RA	RD										
Reset (6)		1	XXX	F0										
Autoselect (Note 7)	Manufacturer ID	4	555	AA	2AA	55	555	90	(BA)X00	01				
	Device ID (11)	6	555	AA	2AA	55	555	90	(BA)X01	7E	(BA)X0E	08	(BA)X0F	00/01
Program		4	555	AA	2AA	55	555	A0	PA	PD				
Chip Erase		6	555	AA	2AA	55	555	80	555	AA	2AA	55	555	10
Sector Erase		6	555	AA	2AA	55	555	80	555	AA	2AA	55	SA	30
Program/Erase Suspend (12)		1	BA	B0										
Program/Erase Resume (13)		1	BA	30										
CFI Query (14, 15)		1	55	98										
Accelerated Program (16)		2	XX	A0	PA	PD								
Configuration Register Verify (15)		3	555	AA	2AA	55	(BA)555	C6	(BA)XX	RD				
Configuration Register Write (17)		4	555	AA	2AA	55	555	D0	XX	WD				
Unlock Bypass Entry (18)		3	555	AA	2AA	55	555	20						
Unlock Bypass Program (18)		2	XX	A0	PA	PD								
Unlock Bypass Erase (18)		2	XX	80	XX	10								
Unlock Bypass CFI (14, 18)		1	XX	98										
Unlock Bypass Reset (18)		2	XX	90	XX	00								

Legend:

BA = Address of bank switching to autoselect mode, bypass mode, or erase operation. Determined by A21:A19, see Tables 4 and 5 for more detail.

PA = Program Address (A21:A0). Addresses latch on falling edge of WE# or CE# pulse, whichever happens later.

PD = Program Data (DQ15:DQ0) written to location PA. Data latches on rising edge of WE# or CE# pulse, whichever happens first.

RA = Read Address (A21:A0).

RD = Read Data (DQ15:DQ0) from location RA.

SA = Sector Address (A21:A12) for verifying (in autoselect mode) or erasing.

WD = Write Data. See "Configuration Register" definition for specific write data. Data latched on rising edge of WE#.

X = Don't care

Notes:

1. *See Table 1 for description of bus operations.*
2. *All values are in hexadecimal.*
3. *Shaded cells in table denote read cycles. All other cycles are write operations.*
4. *During unlock and command cycles, when lower address bits are 555 or 2AAh as shown in table, address bits higher than A11 (except where BA is required) and data bits higher than DQ7 are don't cares.*
5. *No unlock or command cycles required when bank is reading array data.*
6. *Reset command is required to return to reading array (or to erase-suspend-read mode if previously in Erase Suspend) when bank is in autoselect mode, or if DQ5 goes high (while bank is providing status information).*
7. *Cycle 4 of autoselect command sequence is a read cycle. System must provide bank address to obtain manufacturer ID or device ID information. See Autoselect Command Sequence section for more information.*
8. *Unlock Bypass command must be executed before writing command sequence. Unlock Bypass Reset command must be executed to return to normal operation.*
9. *Command is ignored during any embedded program, erase or suspended operation.*
10. *Valid read operations include asynchronous and burst read mode operations.*
11. *Device ID must be read across cycles 4, 5, and 6. 00h in cycle 6 indicates top boot block, 01h indicates bottom boot block.*
12. *System may read and program in non-erasing sectors, or enter autoselect mode, when in Program/Erase Suspend mode. Program/Erase Suspend command is valid only during a sector erase operation, and requires bank address.*
13. *Program/Erase Resume command valid only during Erase Suspend mode, and requires bank address.*
14. *Command valid when device is ready to read array data or when device is in autoselect mode.*
15. *Asynchronous read operations.*
16. *ACC must be at V_{ID} during entire operation of command.*
17. *Command is ignored during any Embedded Program, Embedded Erase, or Suspend operation.*
18. *Unlock Bypass Entry command is required prior to any Unlock Bypass operation. Unlock Bypass Reset command is required to return to reading array.*

Table 15. Sector Protection Command Definitions (x32 Mode)

Command (Notes)	Cycles	Bus Cycles (Notes 1-4)											
		Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data
Reset	1	XXX	F0										
SecSi Sector Entry	3	555	AA	2AA	55	(BA)555	88						
SecSi Sector Exit	4	555	AA	2AA	55	(BA)555	90	XX	00				
SecSi Protection Bit Program (5, 6, 7)	6	555	AA	2AA	55	(BA)555	60	SSA	68	SSA	48	XX	RD(0)
Password Program (5, 8, 9)	5	555	AA	2AA	55	555	38	XX[0-1]	PD[0-1]				
Password Verify (6, 9, 10)	4	555	AA	2AA	55	555	C8	PWA[0-1]	PWD[0-1]				
Password Unlock (8, 11, 12)	4	555	AA	2AA	55	555	28	PWA[0-1]	PWD[0-1]				
PPB Program (5, 6, 7, 13)	6	555	AA	2AA	55	555	60	(SA)WP	68	(SA)WP	48	(SA)WP	RD(0)
All PPB Erase (5, 6, 14, 15)	6	555	AA	2AA	55	555	60	(SA)EP	60	(SA)EP	40	(SA)WP	RD(0)
PPB Lock Bit Set	3	555	AA	2AA	55	555	78						
PPB Lock Bit Status (6, 16)	4	555	AA	2AA	55	555	58	SA	RD(1)				
DPB Write (8)	4	555	AA	2AA	55	555	48	SA	X1				
DPB Erase (8)	4	555	AA	2AA	55	555	48	SA	X0				
DPB or PPB Status (6)	4	555	AA	2AA	55	555	58	SA	RD(0)				
PPMLB Program (5, 6, 7, 13)	6	555	AA	2AA	55	555	60	PL	68	PL	48	XX	RD(0)
PPMLB Status (5)	6	555	AA	2AA	55	555	60	PL	RD(0)				
SPMLB Program (5, 6, 7, 13)	6	555	AA	2AA	55	555	60	SL	68	SL	48	XX	RD(0)
SPMLB Status (5)	6	555	AA	2AA	55	555	60	SL	RD(0)				

Legend:

DPB = Dynamic Protection Bit
SSA = SecSi Sector Address (A6:A0) is (0011010).
PD[1:0] = Program Data. Password written in 2 portions.
PPB = Persistent Protection Bit
PWA = Password Address. A0 selects portion of password.
PWD = Password Data being verified.
PL = Password Protection Mode Lock Address (A5:A0) is (001010)
RD(0) = Read Data DQ0 for protection indicator bit.
RD(1) = Read Data DQ1 for PPB Lock bit status.
SA = Sector Address where security command applies. Address bits A21:A11 uniquely select any sector.
SL = Persistent Protection Mode Lock Address (A5:A0) is (010010)
WP = PPB Address (A6:A0) is (0111010)
EP = PPB Erase Address (A6:A0) is (1111010)
X = Don't care
PPMLB = Password Protection Mode Locking Bit
SPMLB = Persistent Protection Mode Locking Bit

1. *See Table 1 for description of bus operations.*
2. *All values are in hexadecimal.*
3. *Shaded cells in table denote read cycles. All other cycles are write operations.*
4. *During unlock and command cycles, when lower address bits are 555 or 2AAh as shown in table, address bits higher than A11 (except where BA is required) and data bits higher than DQ7 are don't cares.*
5. *Reset command returns device to reading array.*
6. *Asynchronous read operation.*
7. *Cycle 4 programs addressed locking bit. Cycles 5 and 6 validate bit has been fully programmed when DQ0 = 1. If DQ0 = 0 in cycle 6, entire command sequence must be issued and verified again.*
8. *Data is latched on rising edge of WE#.*
9. *Entire command sequence must be executed for each portion of password.*
10. *Command sequence returns FFh if PPMLB is set.*
11. *Password is written over four consecutive cycles at addresses 0-3.*
12. *A 2 µs timeout is required between any two portions of password.*
13. *A 100 µs timeout is required between cycles 4 and 5.*
14. *A 1.2 ms timeout is required between cycles 4 and 5.*
15. *Cycle 4 erases all PPBs. Cycles 5 and 6 validate bits have been fully erased when DQ0 = 0. If DQ0 = 1 in cycle 6, entire command sequence must be issued and verified again. Before issuing erase command, all PPBs should be programmed to prevent PPBs overerasure.*
16. *DQ1 = 1 if PPB locked, 0 if unlocked.*

Table 16. Memory Array Command Definitions (x16 Mode)

Command (Notes)		Cycles	Bus Cycles (Notes 1–4)											
			Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data
Read (5)		1	RA	RD										
Reset (6)		1	XXX	F0										
Autoselect (Note 7)	Manufacturer ID	4	AAA	AA	555	55	AAA	90	(BA)X00	01				
	Device ID (11)	6	AAA	AA	555	55	AAA	90	(BA)X01	7E	(BA)X0E	08	(BA)X0F	00/01
Program		4	AAA	AA	555	55	AAA	A0	PA	PD				
Chip Erase		6	AAA	AA	555	55	AAA	80	AAA	AA	555	55	AAA	10
Sector Erase		6	AAA	AA	555	55	AAA	80	AAA	AA	555	55	SA	30
Program/Erase Suspend (12)		1	BA	B0										
Program/Erase Resume (13)		1	BA	30										
CFI Query (14, 15)		1	55	98										
Accelerated Program (16)		2	XX	A0	PA	PD								
Configuration Register Verify (15)		3	AAA	AA	555	55	(BA)AAA	C6	(BA)XX	RD				
Configuration Register Write (17)		4	AAA	AA	555	55	AAA	D0	XX	WD				
Unlock Bypass Entry (18)		3	AAA	AA	555	55	AAA	20						
Unlock Bypass Program (18)		2	XX	A0	PA	PD								
Unlock Bypass Erase (18)		2	XX	80	XX	10								
Unlock Bypass CFI (14, 18)		1	XX	98										
Unlock Bypass Reset (18)		2	XX	90	XX	00								

Legend:

BA = Address of bank switching to autoselect mode, bypass mode, or erase. Determined by A21:A19, see Tables 4 and 5 for more detail.

PA = Program Address (A21:A-1). Addresses latch on falling edge of WE# or CE# pulse, whichever happens later.

PD = Program Data (DQ15:DQ0) written to location PA. Data latches on rising edge of WE# or CE# pulse, whichever happens first.

RA = Read Address (A21:A-1).

RD = Read Data (DQ15:DQ0) from location RA.

SA = Sector Address (A21:A12) for verifying (in autoselect mode) or erasing.

WD = Write Data. See "Configuration Register" definition for specific write data. Data latched on rising edge of WE#.

X = Don't care

Notes:

1. *See Table 1 for description of bus operations.*
2. *All values are in hexadecimal.*
3. *Shaded cells in table denote read cycles. All other cycles are write operations.*
4. *During unlock and command cycles, when lower address bits are 555 or AAAh as shown in table, address bits higher than A11 (except where BA is required) and data bits higher than DQ7 are don't cares.*
5. *No unlock or command cycles required when bank is reading array data.*
6. *Reset command is required to return to reading array (or to erase-suspend-read mode if previously in Erase Suspend) when a bank is in autoselect mode, or if DQ5 goes high (while bank is providing status information).*
7. *Cycle 4 of autoselect command sequence is a read cycle. System must provide bank address to obtain manufacturer ID or device ID information. See Autoselect Command Sequence section for more information.*
8. *Unlock Bypass command must be executed before writing command sequence. Unlock Bypass Reset command must be executed to return to normal operation.*
9. *Command is ignored during any embedded program, erase or suspended operation.*
10. *Valid read operations include asynchronous and burst read mode operations.*
11. *Device ID must be read across cycles 4, 5, and 6. 00h in cycle 6 indicates top boot block, 01h indicates bottom boot block.*
12. *System may read and program in non-erasing sectors, or enter autoselect mode, when in Program/Erase Suspend mode. Program/Erase Suspend command valid only during a sector erase operation, and requires bank address.*
13. *Program/Erase Resume command valid only during Erase Suspend mode, and requires bank address.*
14. *Command is valid when device is ready to read array data or when device is in autoselect mode.*
15. *Asynchronous read operations.*
16. *ACC must be at V_{ID} during entire operation of this command.*
17. *Command ignored during any Embedded Program, Embedded Erase, or Suspend operation.*
18. *Unlock Bypass Entry command required prior to any Unlock Bypass operation. Unlock Bypass Reset command is required to return to reading array.*

Table 17. Sector Protection Command Definitions (x16 Mode)

Command (Notes)	Cycles	Bus Cycles (Notes 1-4)											
		Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data
Reset	1	XXX	F0										
SecSi Sector Entry	3	AAA	AA	555	55	(BA)AAA	88						
SecSi Sector Exit	4	AAA	AA	555	55	(BA)AAA	90	XX	00				
SecSi Protection Bit Program (5, 6, 7)	6	AAA	AA	555	55	(BA)AAA	60	SSA	68	SSA	48	XX	RD(0)
Password Program (5, 8, 9)	5	AAA	AA	555	55	AAA	38	XX[0-3]	PD[0-3]				
Password Verify (6, 9, 10)	4	AAA	AA	555	55	AAA	C8	PWA[0-3]	PWD[0-3]				
Password Unlock (8, 11, 12)	4	AAA	AA	555	55	AAA	28	PWA[0-3]	PWD[0-3]				
PPB Program (5, 6, 7, 13)	6	AAA	AA	555	55	AAA	60	(SA)WP	68	(SA)WP	48	(SA)WP	RD(0)
All PPB Erase (5, 6, 14, 15)	6	AAA	AA	555	55	AAA	60	(SA)EP	60	(SA)EP	40	(SA)WP	RD(0)
PPB Lock Bit Set	3	AAA	AA	555	55	AAA	78						
PPB Lock Bit Status (6, 16)	4	AAA	AA	555	55	AAA	58	SA	RD(1)				
DPB Write (8)	4	AAA	AA	555	55	AAA	48	SA	X1				
DPB Erase (8)	4	AAA	AA	555	55	AAA	48	SA	X0				
DPB or PPB Status (6)	4	AAA	AA	555	55	AAA	58	SA	RD(0)				
PPMLB Program (5, 6, 7, 13)	6	AAA	AA	555	55	AAA	60	PL	68	PL	48	XX	RD(0)
PPMLB Status (5)	6	AAA	AA	555	55	AAA	60	PL	RD(0)				
SPMLB Program (5, 6, 7, 13)	6	AAA	AA	555	55	AAA	60	SL	68	SL	48	XX	RD(0)
SPMLB Status (5)	6	AAA	AA	555	55	AAA	60	SL	RD(0)				

Legend:

DPB = Dynamic Protection Bit
SSA = SecSi Sector Address (A6:A0) is (0011010).
PD[3:0] = Program Data. Password written as four 16-bit sections.
PPB = Persistent Protection Bit
PWA = Password Address. A0:A-1 selects portion of password.
PWD = Password Data being verified.
PL = Password Protection Mode Lock Address (A5:A0) is (001010)
RD(0) = Read Data DQ0 for protection indicator bit.
RD(1) = Read Data DQ1 for PPB Lock bit status.
SA = Sector Address where security command applies. Address bits A21:A11 uniquely select any sector.
SL = Persistent Protection Mode Lock Address (A5:A0) is (010010)
WP = PPB Address (A6:A0) is (0111010)
EP = PPB Erase Address (A6:A0) is (1111010)
X = Don't care
PPMLB = Password Protection Mode Locking Bit
SPMLB = Persistent Protection Mode Locking Bit

1. *See Table 1 for description of bus operations.*
2. *All values are in hexadecimal.*
3. *Shaded cells in table denote read cycles. All other cycles are write operations.*
4. *During unlock and command cycles, when lower address bits are 555 or AAAh as shown in table, address bits higher than A11 (except where BA is required) and data bits higher than DQ7 are don't cares.*
5. *Reset command returns device to reading array.*
6. *Asynchronous read operation.*
7. *Cycle 4 programs addressed locking bit. Cycles 5 and 6 validate the bit has been fully programmed when DQ0 = 1. If DQ0 = 0 in cycle 6, the program command must be issued and verified again.*
8. *Data is latched on rising edge of WE#.*
9. *Entire command sequence must be executed for each portion of password.*
10. *Command sequence returns FFh if PPMLB is set.*
11. *Password is written over four consecutive cycles, at addresses 0-3.*
12. *A 2 µs timeout is required between any two portions of password.*
13. *A 100 µs timeout is required between cycles 4 and 5.*
14. *A 1.2 ms timeout is required between cycles 4 and 5.*
15. *Cycle 4 erases all PPBs. Cycles 5 and 6 validate bits have been fully erased when DQ0 = 0. If DQ0 = 1 in cycle 6, erase command must be issued and verified again. Before issuing erase command, all PPBs should be programmed in order to prevent PPB overerasure.*
16. *DQ1 = 1 if PPB locked, 0 if unlocked.*

WRITE OPERATION STATUS

The device provides several bits to determine the status of a program or erase operation: DQ2, DQ3, DQ5, DQ6, and DQ7. Table 18 and the following subsections describe the function of these bits. DQ7 and DQ6 each offer a method for determining whether a program or erase operation is complete or in progress. The device also provides a hardware-based output signal, RY/BY#, to determine whether an Embedded Program or Erase operation is in progress or has been completed.

DQ7: Data# Polling

The Data# Polling bit, DQ7, indicates to the host system whether an Embedded Program or Erase algorithm is in progress or completed, or whether a bank is in Erase Suspend. Data# Polling is valid after the rising edge of the final WE# pulse in the command sequence.

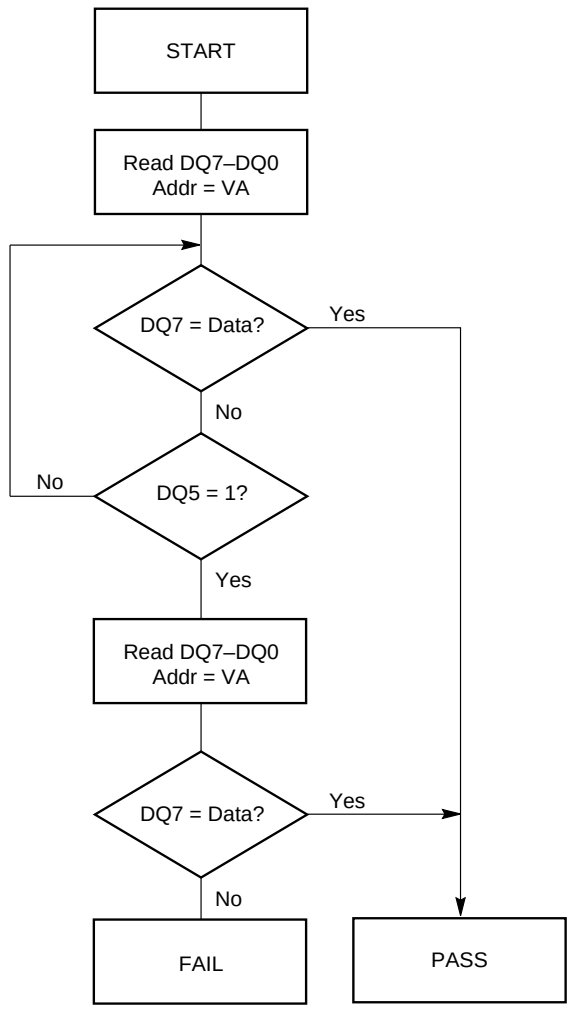
During the Embedded Program algorithm, the device outputs on DQ7 the complement of the datum programmed to DQ7. This DQ7 status also applies to programming during Erase Suspend. When the Embedded Program algorithm is complete, the device outputs the datum programmed to DQ7. The system must provide the program address to read valid status information on DQ7. If a program address falls within a protected sector, Data# Polling on DQ7 is active for approximately 1 µs, then that bank returns to the read mode.

During the Embedded Erase algorithm, Data# Polling produces a “0” on DQ7. When the Embedded Erase algorithm is complete, or if the bank enters the Erase Suspend mode, Data# Polling produces a “1” on DQ7. The system must provide an address within any of the sectors selected for erasure to read valid status information on DQ7.

After an erase command sequence is written, if all sectors selected for erasing are protected, Data# Polling on DQ7 is active for approximately 100 µs, then the bank returns to the read mode. If not all selected sectors are protected, the Embedded Erase algorithm erases the unprotected sectors, and ignores the selected sectors that are protected. However, if the system reads DQ7 at an address within a protected sector, the status may not be valid.

When the system detects DQ7 has changed from the complement to true data, it can read valid data at DQ31–DQ0 (or DQ15–DQ0 for word mode) on the *following* read cycles. Just prior to the completion of an Embedded Program or Erase operation, DQ7 may change asynchronously with DQ31–DQ16 (DQ15–DQ0 for word mode) while Output Enable (OE#) is asserted low. That is, the device may change from providing status information to valid data on DQ7. Depending on when the system samples the DQ7 output, it may read the status or valid data. Even if the device has completed the program or erase operation and DQ7 has valid data, the data outputs on DQ31–DQ0 may be still invalid. Valid data on DQ31–DQ0 (or DQ15–DQ0 for word mode) will appear on successive read cycles.

Table 18 shows the outputs for Data# Polling on DQ7. Figure 5 shows the Data# Polling algorithm. Figure 20 in the AC Characteristics section shows the Data# Polling timing diagram.



Notes:

1. *VA = Valid address for programming. During a sector erase operation, a valid address is any sector address within the sector being erased. During chip erase, a valid address is any non-protected sector address.*
2. *DQ7 should be rechecked even if DQ5 = “1” because DQ7 may change simultaneously with DQ5.*

Figure 5. Data# Polling Algorithm

RY/BY#: Ready/Busy#

The RY/BY# is a dedicated, open-drain output pin which indicates whether an Embedded Algorithm is in progress or complete. The RY/BY# status is valid after the rising edge of the final WE# pulse in the command sequence. Since RY/BY# is an open-drain output, several RY/BY# pins can be tied together in parallel with a pull-up resistor to V_{CC}.

If the output is low (Busy), the device is actively erasing or programming. (This includes programming in the Erase Suspend mode.) If the output is high (Ready), the device is in the read mode, the standby mode, or one of the banks is in the erase-suspend-read mode.

Table 18 shows the outputs for RY/BY#.

DQ6: Toggle Bit I

Toggle Bit I on DQ6 indicates whether an Embedded Program or Erase algorithm is in progress or complete, or whether the device has entered the Erase Suspend mode. Toggle Bit I may be read at any address, and is valid after the rising edge of the final WE# pulse in the command sequence (prior to the program or erase operation), and during the sector erase time-out.

During an Embedded Program or Erase algorithm operation, successive read cycles to any address cause DQ6 to toggle. The system may use either OE# or CE# to control the read cycles. When the operation is complete, DQ6 stops toggling.

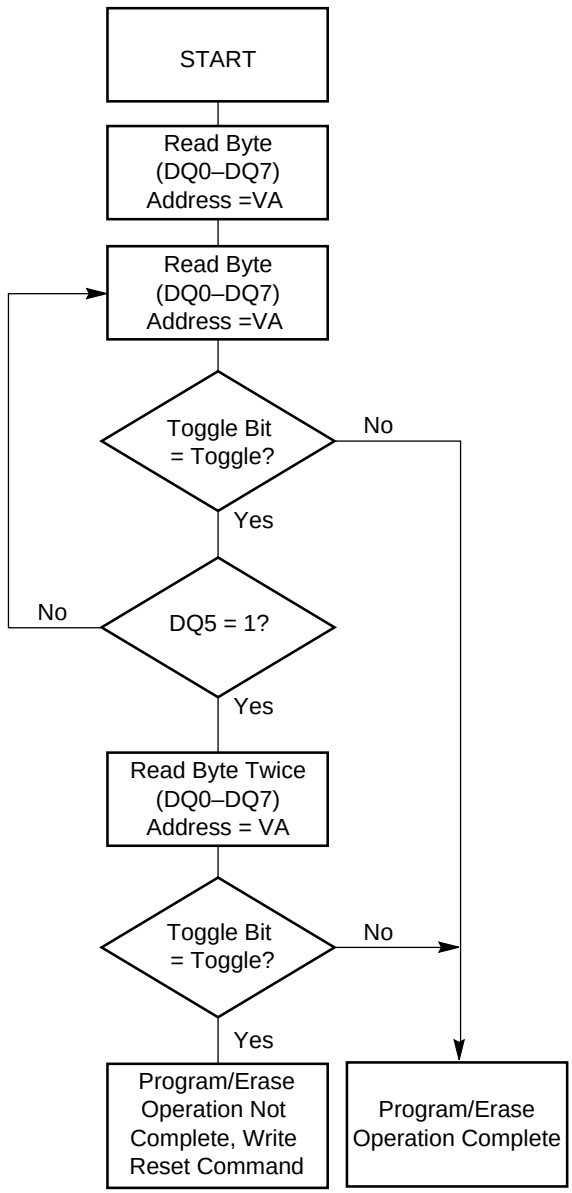
After an erase command sequence is written, if all sectors selected for erasing are protected, DQ6 toggles for approximately 100 µs, then returns to reading array data. If not all selected sectors are protected, the Embedded Erase algorithm erases the unprotected sectors, and ignores the selected sectors that are protected.

The system can use DQ6 and DQ2 together to determine whether a sector is actively erasing or is erase-suspended. When the device is actively erasing (that is, the Embedded Erase algorithm is in progress), DQ6 toggles. When the device enters the Erase Suspend mode, DQ6 stops toggling. However, the system must also use DQ2 to determine which sectors are erasing or erase-suspended. Alternatively, the system can use DQ7 (see the subsection on DQ7: Data# Polling).

If a program address falls within a protected sector, DQ6 toggles for approximately 1 µs after the program command sequence is written, then returns to reading array data.

DQ6 also toggles during the erase-suspend-program mode, and stops toggling once the Embedded Program algorithm is complete.

Table 18 shows the outputs for Toggle Bit I on DQ6. Figure 6 shows the toggle bit algorithm. Figure 21 in the “AC Characteristics” section shows the toggle bit timing diagrams. Figure 22 shows the differences between DQ2 and DQ6 in graphical form. See also the subsection on DQ2: Toggle Bit II.



Note: *The system should recheck the toggle bit even if DQ5 = “1” because the toggle bit may stop toggling as DQ5 changes to “1.” See the subsections on DQ6 and DQ2 for more information.*

Figure 6. Toggle Bit Algorithm

DQ2: Toggle Bit II

The “Toggle Bit II” on DQ2, when used with DQ6, indicates whether a particular sector is actively erasing (that is, the Embedded Erase algorithm is in progress), or whether that sector is erase-suspended. Toggle Bit II is valid after the rising edge of the final WE# pulse in the command sequence.

DQ2 toggles when the system reads at addresses within those sectors that have been selected for erasure. (The system may use either OE# or CE# to control the read cycles.) But DQ2 cannot distinguish whether the sector is actively erasing or is erase-suspended. DQ6, by comparison, indicates whether the device is actively erasing, or is in Erase Suspend, but cannot distinguish which sectors are selected for erasure. Thus, both status bits are required for sector and mode information. Refer to Table 18 to compare outputs for DQ2 and DQ6.

Figure 6 shows the toggle bit algorithm in flowchart form, and the section “DQ2: Toggle Bit II” explains the algorithm. See also the DQ6: Toggle Bit I subsection. Figure 21 shows the toggle bit timing diagram. Figure 22 shows the differences between DQ2 and DQ6 in graphical form.

Reading Toggle Bits DQ6/DQ2

Refer to Figure 6 for the following discussion. Whenever the system initially begins reading toggle bit status, it must read DQ31–DQ0 (or DQ15–DQ0 for word mode) at least twice in a row to determine whether a toggle bit is toggling. Typically, the system would note and store the value of the toggle bit after the first read. After the second read, the system would compare the new value of the toggle bit with the first. If the toggle bit is not toggling, the device has completed the program or erase operation. The system can read array data on DQ31–DQ0 (or DQ15–DQ0 for word mode) on the following read cycle.

However, if after the initial two read cycles, the system determines that the toggle bit is still toggling, the system also should note whether the value of DQ5 is high (see the section on DQ5). If it is, the system should then determine again whether the toggle bit is toggling, since the toggle bit may have stopped toggling just as DQ5 went high. If the toggle bit is no longer toggling, the device has successfully completed the program or erase operation. If it is still toggling, the device did not completed the operation successfully, and the system must write the reset command to return to reading array data.

The remaining scenario is that the system initially determines that the toggle bit is toggling and DQ5 has not gone high. The system may continue to monitor the toggle bit and DQ5 through successive read cycles, determining the status as described in the previous paragraph. Alternatively, it may choose to perform other system tasks. In this case, the system must start at the beginning of the algorithm when it returns to determine the status of the operation (top of Figure 6).

DQ5: Exceeded Timing Limits

DQ5 indicates whether the program or erase time has exceeded a specified internal pulse count limit. Under these conditions DQ5 produces a “1,” indicating that the program or erase cycle was not successfully completed.

The device may output a “1” on DQ5 if the system tries to program a “1” to a location that was previously programmed to “0.” **Only an erase operation can change a “0” back to a “1.”** Under this condition, the device halts the operation, and when the timing limit has been exceeded, DQ5 produces a “1.”

Under both these conditions, the system must write the reset command to return to the read mode (or to the erase-suspend-read mode if a bank was previously in the erase-suspend-program mode).

DQ3: Sector Erase Timer

After writing a sector erase command sequence, the system may read DQ3 to determine whether or not erasure has begun. (The sector erase timer does not apply to the chip erase command.) If additional sectors are selected for erasure, the entire time-out also applies after each additional sector erase command. When the time-out period is complete, DQ3 switches from a “0” to a “1.” If the time between additional sector erase commands from the system can be assumed to be less than 50 µs, the system need not monitor DQ3. See also the Sector Erase Command Sequence section.

After the sector erase command is written, the system should read the status of DQ7 (Data# Polling) or DQ6 (Toggle Bit I) to ensure that the device has accepted the command sequence, and then read DQ3. If DQ3 is “1,” the Embedded Erase algorithm has begun; all further commands (except Erase Suspend) are ignored until the erase operation is complete. If DQ3 is “0,” the device will accept additional sector erase commands. To ensure the command has been accepted, the system software should check the status of DQ3 prior to and following each subsequent sector erase command. If DQ3 is high on the second status check, the last command might not have been accepted.

Table 18 shows the status of DQ3 relative to the other status bits.

Table 18. Write Operation Status

Status			DQ7 (Note 2)	DQ6	DQ5 (Note 1)	DQ3	DQ2 (Note 2)	RY/BY#
Standard Mode	Embedded Program Algorithm		DQ7#	Toggle	0	N/A	No toggle	0
	Embedded Erase Algorithm		0	Toggle	0	1	Toggle	0
Erase Suspend Mode	Erase-Suspend-Read	Erase Suspended Sector	1	No toggle	0	N/A	Toggle	1
		Non-Erase Suspended Sector	Data	Data	Data	Data	Data	1
	Erase-Suspend-Program		DQ7#	Toggle	0	N/A	N/A	0

Notes:

1. *DQ5 switches to '1' when an Embedded Program or Embedded Erase operation has exceeded the maximum timing limits. Refer to the section on DQ5 for more information.*
2. *DQ7 and DQ2 require a valid address when reading status information. Refer to the appropriate subsection for further details.*
3. *When reading write operation status bits, the system must always provide the bank address where the Embedded Algorithm is in progress. The device outputs array data if the system addresses a non-busy bank.*

ABSOLUTE MAXIMUM RATINGS

Storage Temperature
Plastic Packages . . . . . –65°C to +150°C

Ambient Temperature
with Power Applied . . . . . –65°C to +125°C

Voltage with Respect to Ground

V_{CC} (Note 1) . . . . . –0.5 V to +4.0 V

A9, OE#, and RESET#
(Note 2) . . . . . –0.5 V to +12.5 V

ACC (Note 2) . . . . . –0.5 V to +10.5 V

All other pins (Note 1) . . . . . –0.5 V to V_{CC} +0.5 V

Output Short Circuit Current (Note 3) . . . . . 200 mA

Notes:

1. *Minimum DC voltage on input or I/O pins is –0.5 V. During voltage transitions, input or I/O pins may overshoot V_{SS} to –2.0 V for periods of up to 20 ns. Maximum DC voltage on input or I/O pins is V_{CC} +0.5 V. See Figure 7. During voltage transitions, input or I/O pins may overshoot to V_{CC} +2.0 V for periods up to 20 ns. See Figure 8.*
2. *Minimum DC input voltage on pins A9, OE#, RESET#, and ACC is –0.5 V. During voltage transitions, A9, OE#, ACC, and RESET# may overshoot V_{SS} to –2.0 V for periods of up to 20 ns. See Figure 7. Maximum DC input voltage on pin A9, OE#, and RESET# is +12.5 V which may overshoot to +14.0 V for periods up to 20 ns. Maximum DC input voltage on ACC is +9.5 V which may overshoot to +12.0 V for periods up to 20 ns.*
3. *No more than one output may be shorted to ground at a time. Duration of the short circuit should not be greater than one second.*

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this data sheet is not implied. Exposure of the device to absolute maximum rating conditions for extended periods may affect device reliability.

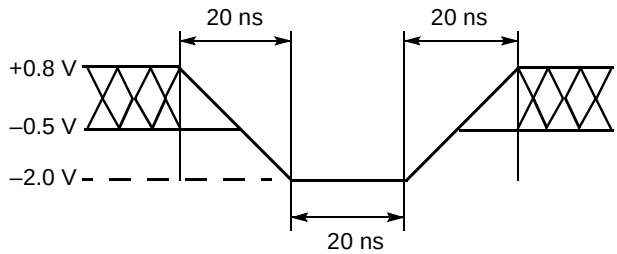


Figure 7. Maximum Negative Overshoot Waveform

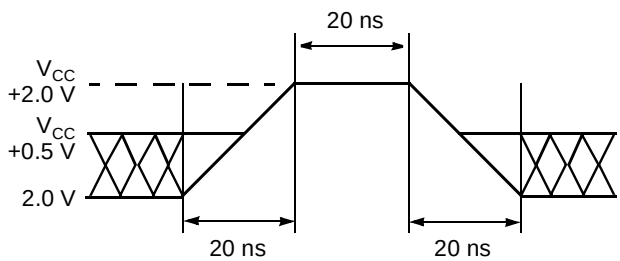


Figure 8. Maximum Positive Overshoot Waveform

OPERATING RANGES

Industrial (I) Devices

Ambient Temperature (T_A) . . . . . –40°C to +85°C

Extended (E) Devices

Ambient Temperature (T_A) . . . . . –55°C to +125°C

Supply Voltages

V_{CC} for full regulated range . . . . . 3.0 V to 3.6 V

V_{CC} for full voltage range . . . . . 2.7 V to 3.6 V

V_{IO} (see Note) . . . . . 2.7 V to 3.6 V

Note: *For all AC and DC specifications, $V_{IO} = V_{CC}$; contact AMD for other V_{IO} options.*

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS

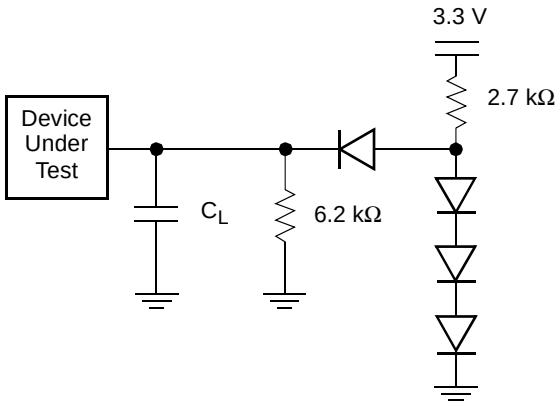
CMOS Compatible

Parameter Symbol	Parameter Description	Test Conditions		Min	Typ	Max	Unit
I_{LI}	Input Load Current	$V_{IN} = V_{SS}$ to V_{CC}, $V_{CC} = V_{CC\ max}$				±1.0	µA
I_{LIT}	A9, OE#, RESET# Input Load Current	$V_{CC} = V_{CC\ max}$; V_{ID}= 12.5 V				35	µA
I_{LO}	Output Leakage Current	$V_{OUT} = V_{SS}$ to V_{CC}, OE# = V_{IH} $V_{CC} = V_{CC\ max}$				±1.0	µA
I_{CC1}	V_{CC} Active Inter-page Read Current, Word/Double Word Modes (Notes 1, 2)	CE# = V_{IL}, OE# = V_{IH}	1 MHz		4.5	9	mA
			5 MHz		20	40	
			10 MHz		38	45	
	V_{CC} Active Intra-page Read Current, Word/Double Word Modes (Note 2)	CE# = V_{IL}, OE# = V_{IH}	1 MHz		9	18	mA
			5 MHz		37	45	
I_{CC2}	V_{CC} Active Write Current (Notes 2, 3)	CE# = V_{IL}, OE# = V_{IH}, WE# = V_{IL}			17	35	mA
I_{CC3}	V_{CC} Standby Current (Note 2)	CE#, RESET# = V_{CC} ± 0.3 V			1.5	5	µA
I_{CC4}	V_{CC} Reset Current (Note 2)	RESET# = V_{SS} ± 0.3 V			1.5	5	µA
I_{CC5}	Automatic Sleep Mode (Notes 2, 4)	$V_{IH} = V_{CC}$ ± 0.3 V; $V_{IL} = V_{SS}$ ± 0.3 V			1.5	5	µA
I_{CC6}	V_{CC} Active Read-While-Program Current (Notes 1, 2)	CE# = V_{IL}, OE# = V_{IH}	Word		30	45	mA
			Dbl. Word		30	45	
I_{CC7}	V_{CC} Active Read-While-Erase Current (Notes 1, 2)	CE# = V_{IL}, OE# = V_{IH}	Word		21	45	mA
			Dbl. Word		21	45	
I_{CC8}	V_{CC} Active Program-While-Erase-Suspended Current (Notes 2, 5)	CE# = V_{IL}, OE# = V_{IH}			17	35	mA
I_{ACC}	ACC Accelerated Program Current, Double Word or Word	CE# = V_{IL}, OE# = V_{IH}	ACC pin		5	10	mA
			V_{CC} pin		15	30	mA
V_{IL}	Input Low Voltage			–0.5		0.8	V
V_{IH}	Input High Voltage			0.7 x V_{CC}		V_{CC} + 0.3	V
V_{HH}	Voltage for ACC Program Acceleration	V_{CC} = 3.0 V ± 10%		8.5		9.5	V
V_{ID}	Voltage for Autoselect and Temporary Sector Unprotect	V_{CC} = 3.0 V ± 10%		11.5		12.5	V
V_{OL}	Output Low Voltage	I_{OL} = 4.0 mA, $V_{CC} = V_{CC\ min}$				0.45	V
V_{OH1}	Output High Voltage	I_{OH} = –2.0 mA, $V_{CC} = V_{CC\ min}$		0.85 V_{IO}			V
V_{OH2}		I_{OH} = –100 µA, $V_{CC} = V_{CC\ min}$		V_{IO}–0.4			
V_{LKO}	Low V_{CC} Lock-Out Voltage (Note 5)			2.3		2.5	V

Notes:

1. *The I_{CC} current listed is typically less than 4mA/MHz, with OE# at V_{IH}.*
2. *Maximum I_{CC} specifications are tested with $V_{CC} = V_{CCmax}$.*
3. *I_{CC} active while Embedded Erase or Embedded Program is in progress.*
4. *Automatic sleep mode enables the low power mode when addresses remain stable for t_{ACC} + 30 ns. Typical sleep mode current is 200 nA.*
5. *Not 100% tested.*

TEST CONDITIONS



Note: *Diodes are IN3064 or equivalent*

Figure 9. Test Setup

Table 19. Test Specifications

Test Condition	70R, 70, 80, 90	Unit
Output Load	1 TTL gate	
Output Load Capacitance, C_L (including jig capacitance)	30	pF
Input Rise and Fall Times	5	ns
Input Pulse Levels	0.0–3.0	V
Input timing measurement reference levels	1.5	V
Output timing measurement reference levels	1.5	V

KEY TO SWITCHING WAVEFORMS

WAVEFORM	INPUTS	OUTPUTS
	Steady	
	Changing from H to L	
	Changing from L to H	
	Don't Care, Any Change Permitted	Changing, State Unknown
	Does Not Apply	Center Line is High Impedance State (High Z)

KS000010-PAL

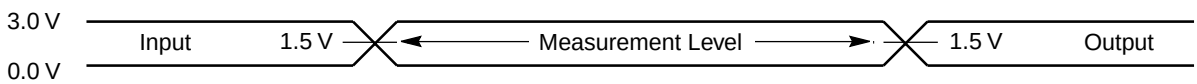


Figure 10. Input Waveforms and Measurement Levels

AC CHARACTERISTICS

Read-Only Operations

Parameter		Description		Test Setup		Speed Options			Unit
JEDEC	Std.					70R, 70	80	90	
t_{AVAV}	t_{RC}	Read Cycle Time (Note 1)			Min	70	80	90	ns
t_{AVQV}	t_{ACC}	Address to Output Delay		CE#, OE# = V_{IL}	Max	70	80	90	ns
t_{ELQV}	t_{CE}	Chip Enable to Output Delay		OE# = V_{IL}	Max	70	80	90	ns
	t_{PACC}	Page Access Time			Max	25	30	35	ns
t_{GLQV}	t_{OE}	Output Enable to Output Delay			Max	25	30	40	ns
t_{EHQZ}	t_{DF}	Chip Enable to Output High Z (Notes 1, 3)			Max	25	30	30	ns
t_{GHQZ}	t_{DF}	Output Enable to Output High Z (Notes 1, 3)			Max	25	30	30	ns
t_{AXQX}	t_{OH}	Output Hold Time From Addresses, CE# or OE#, Whichever Occurs First			Min	4	5	5	ns
	t_{OEH}	Output Enable Hold Time (Note 1)	Read		Min	0			ns
			Toggle and Data# Polling		Min	10			ns

Notes:

1. *Not 100% tested.*
2. *See Figure 9 and Table 19 for test specifications*
3. *Measurements performed by placing a 50 ohm termination on the data pin with a bias of V_{CC}/2. The time from OE# high to the data bus driven to V_{CC}/2 is taken as t_{DF}.*

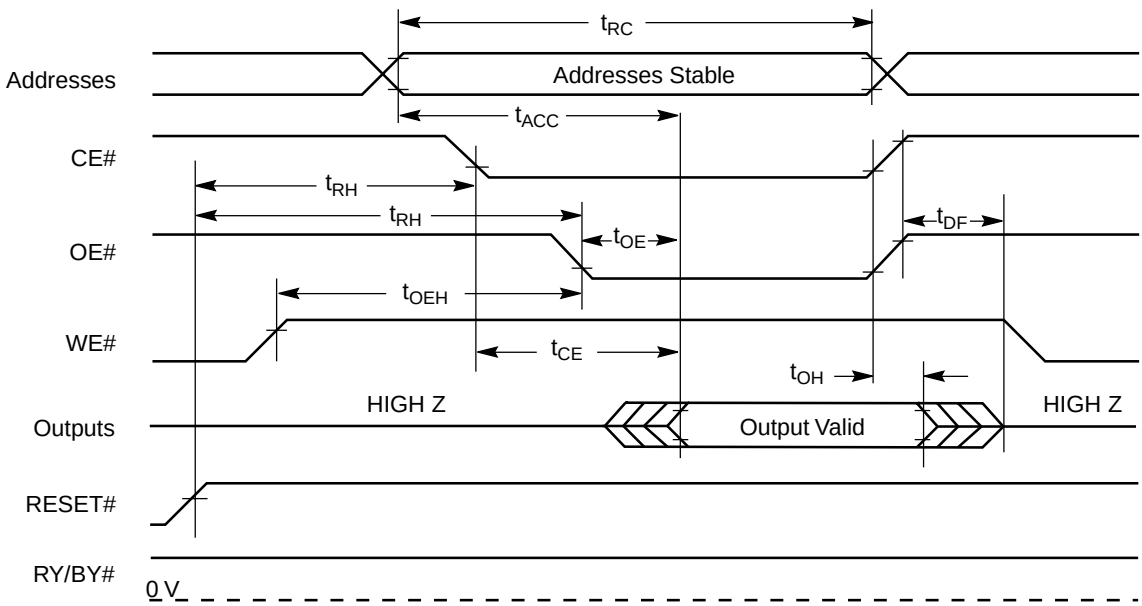


Figure 11. Read Operation Timings

AC CHARACTERISTICS

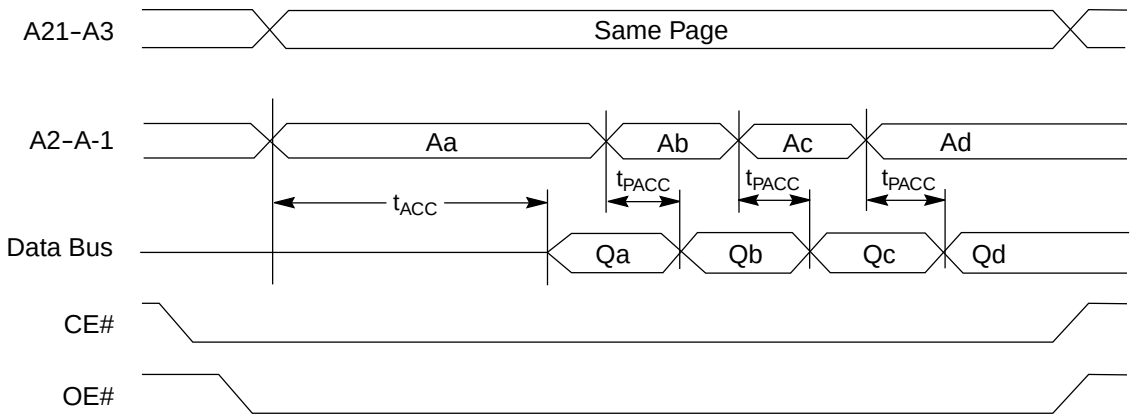


Figure 12. Page Read Operation Timings

AC CHARACTERISTICS

Hardware Reset (RESET#)

Parameter		Description		All Speed Options	Unit
JEDEC	Std				
	t_{Ready}	RESET# Pin Low (During Embedded Algorithms) to Read Mode (See Note)	Max	20	µs
	t_{Ready}	RESET# Pin Low (NOT During Embedded Algorithms) to Read Mode (See Note)	Max	500	ns
	t_{RP}	RESET# Pulse Width	Min	500	ns
	t_{RH}	Reset High Time Before Read (See Note)	Min	50	ns
	t_{RPD}	RESET# Low to Standby Mode	Min	20	µs
	t_{RB}	RY/BY# Recovery Time	Min	0	ns

Note: *Not 100% tested.*

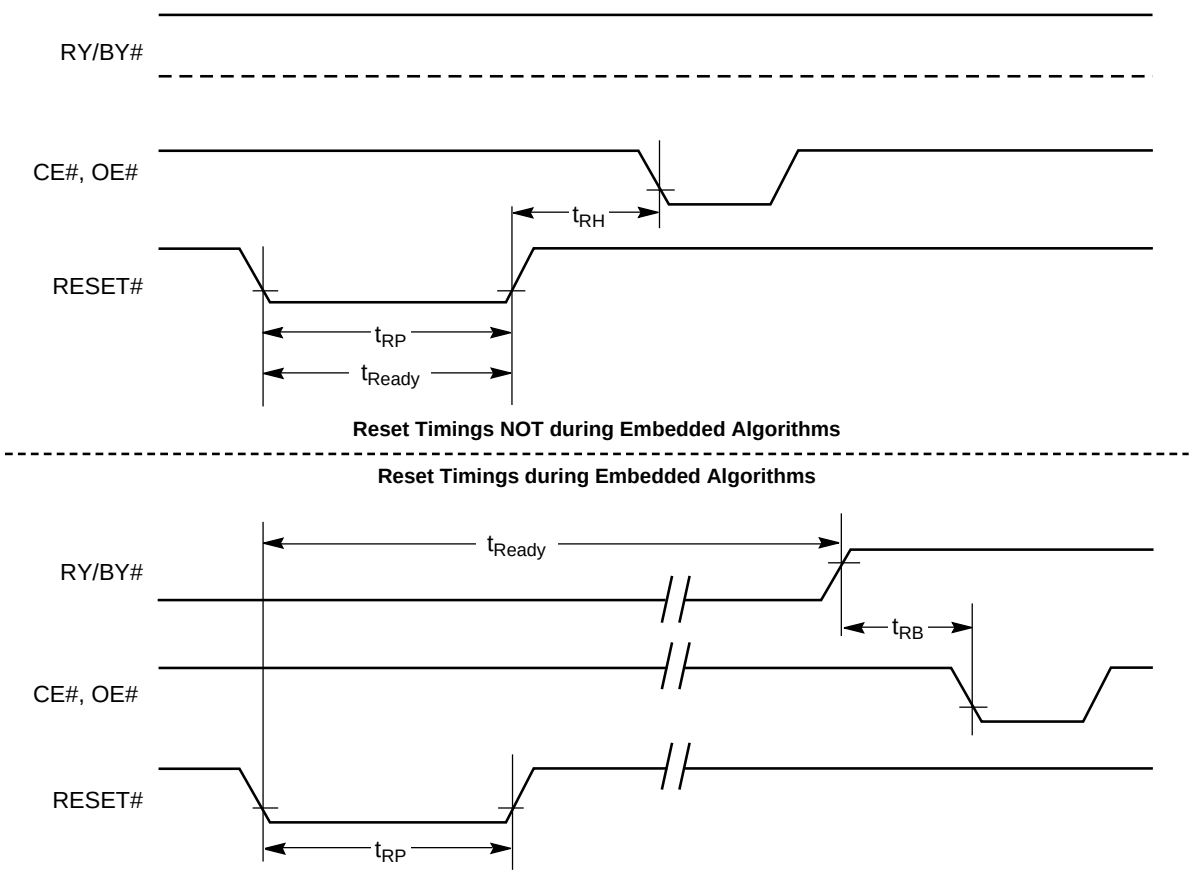


Figure 13. Reset Timings

AC CHARACTERISTICS

Word/Double Word Configuration (WORD#)

Parameter		Description		Speed Options			Unit
JEDEC	Std			70R, 70	80	90	
	t_{ELFL}/t_{ELFH}	CE# to WORD# Switching Low or High	Max	5			ns
	t_{FLQZ}	WORD# Switching Low to Output HIGH Z	Max	30	30	30	ns
	t_{FHQV}	WORD# Switching High to Output Active	Min	70	80	90	ns

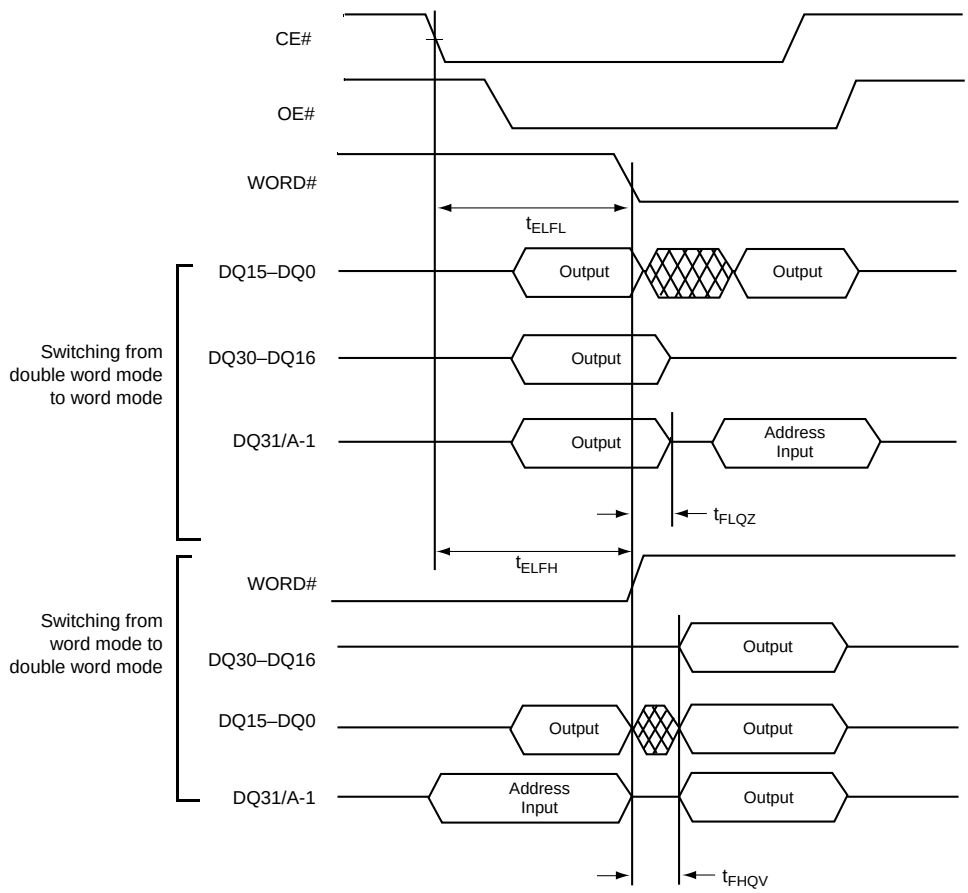
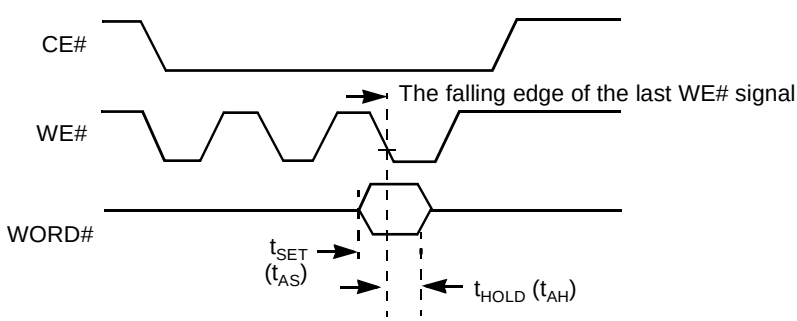


Figure 14. WORD# Timings for Read Operations



Note: *Refer to the Erase/Program Operations table for t_{AS} and t_{AH} specifications.*

Figure 15. WORD# Timings for Write Operations

AC CHARACTERISTICS

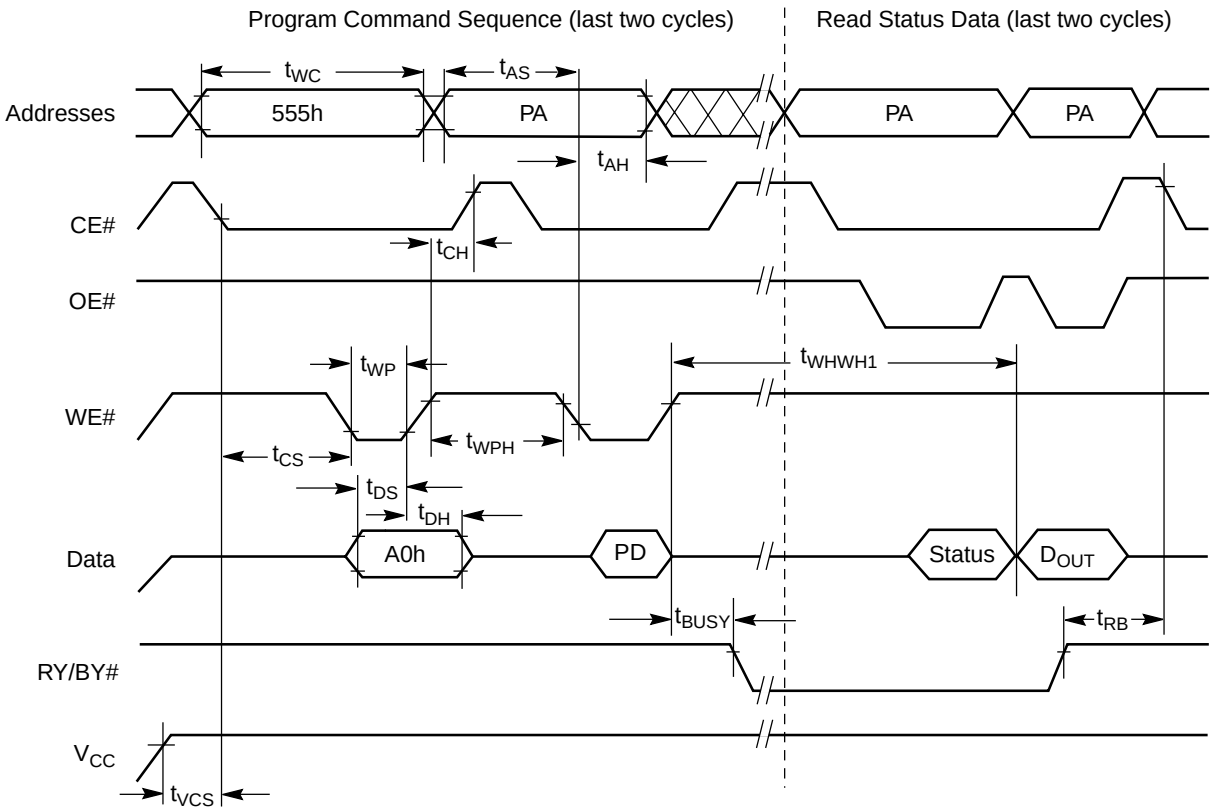
Erase and Program Operations

Parameter		Description			Speed Options			Unit
JEDEC	Std.				70R, 70	80	90	
t_{AVAV}	t_{WC}	Write Cycle Time (Note 1)		Min	70	80	90	ns
t_{AVWL}	t_{AS}	Address Setup Time		Min	0			ns
	t_{ASO}	Address Setup Time to OE# low during toggle bit polling		Min	15			ns
t_{WLAX}	t_{AH}	Address Hold Time		Min	45			ns
	t_{AHT}	Address Hold Time From CE# or OE# high during toggle bit polling		Min	0			ns
t_{DVWH}	t_{DS}	Data Setup Time		Min	35	45	45	ns
t_{WHDX}	t_{DH}	Data Hold Time		Min	0			ns
	t_{OEPH}	Output Enable High during toggle bit polling		Min	20			ns
t_{GHWL}	t_{GHWL}	Read Recovery Time Before Write (OE# High to WE# Low)		Min	0			ns
t_{ELWL}	t_{CS}	CE# Setup Time		Min	0			ns
t_{WHEH}	t_{CH}	CE# Hold Time		Min	0			ns
t_{WLWH}	t_{WP}	Write Pulse Width		Min	35			ns
t_{WHDL}	t_{WPH}	Write Pulse Width High		Min	30			ns
	$t_{SR/W}$	Latency Between Read and Write Operations		Min	0			ns
t_{WHWH1}	t_{WHWH1}	Programming Operation (Note 2)	Word	Typ	8.6			µs
			Double Word	Typ	12.6			
t_{WHWH1}	t_{WHWH1}	Accelerated Programming Operation, Double Word or Word (Note 2)		Typ	4			µs
t_{WHWH2}	t_{WHWH2}	Sector Erase Operation (Note 2)		Typ	0.2			sec
	t_{VCS}	V_{CC} Setup Time (Note 1)		Min	50			µs
	t_{RB}	Write Recovery Time from RY/BY#		Min	0			ns
	t_{BUSY}	Program/Erase Valid to RY/BY# Delay		Max	90			ns

Notes:

1. *Not 100% tested.*
2. *See the "Erase And Programming Performance" section for more information.*

AC CHARACTERISTICS



Notes:

1. *PA = program address, PD = program data, D_{OUT} is the true data at the program address.*
2. *Illustration shows device in word mode.*

Figure 16. Program Operation Timings

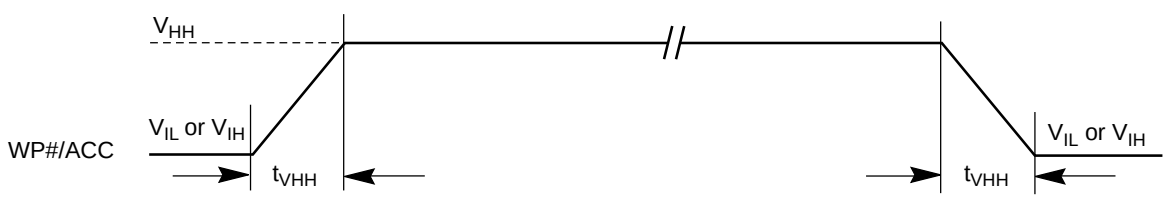
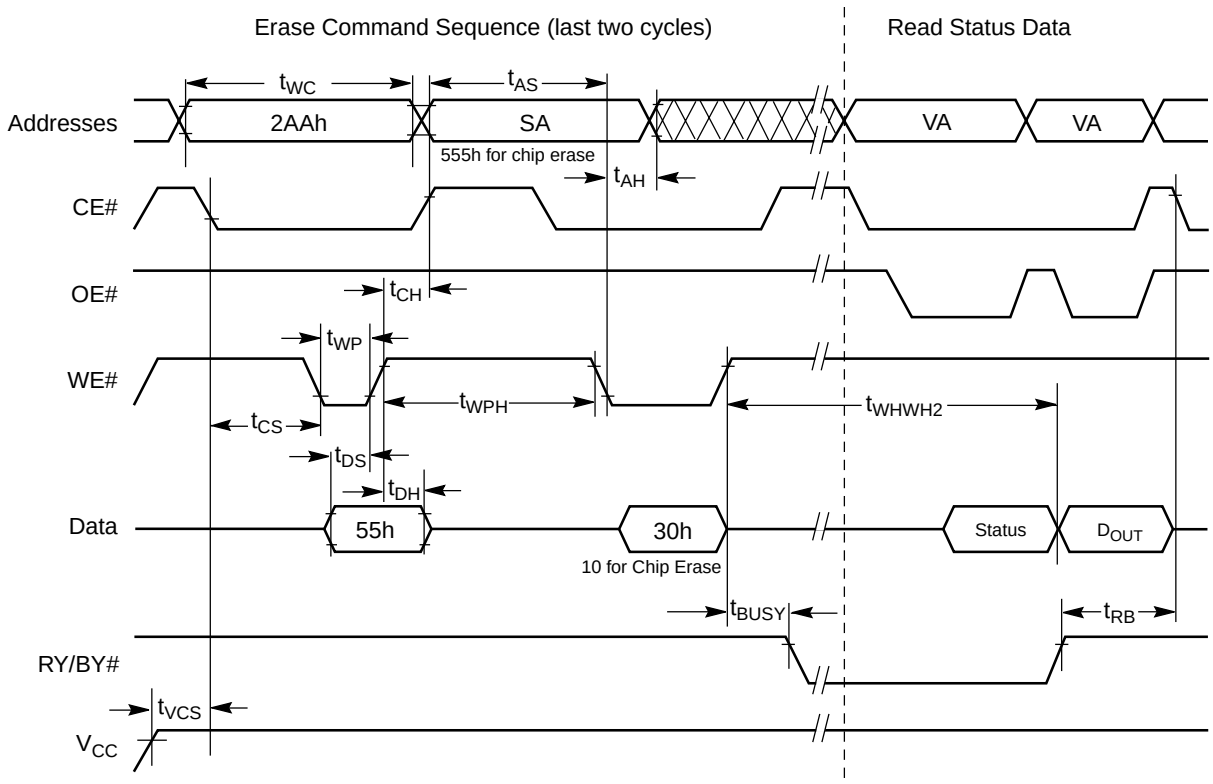


Figure 17. Accelerated Program Timing Diagram

AC CHARACTERISTICS



Notes:

1. *SA = sector address (for Sector Erase), VA = Valid Address for reading status data (see "Write Operation Status".*
2. *These waveforms are for the word mode.*

Figure 18. Chip/Sector Erase Operation Timings

AC CHARACTERISTICS

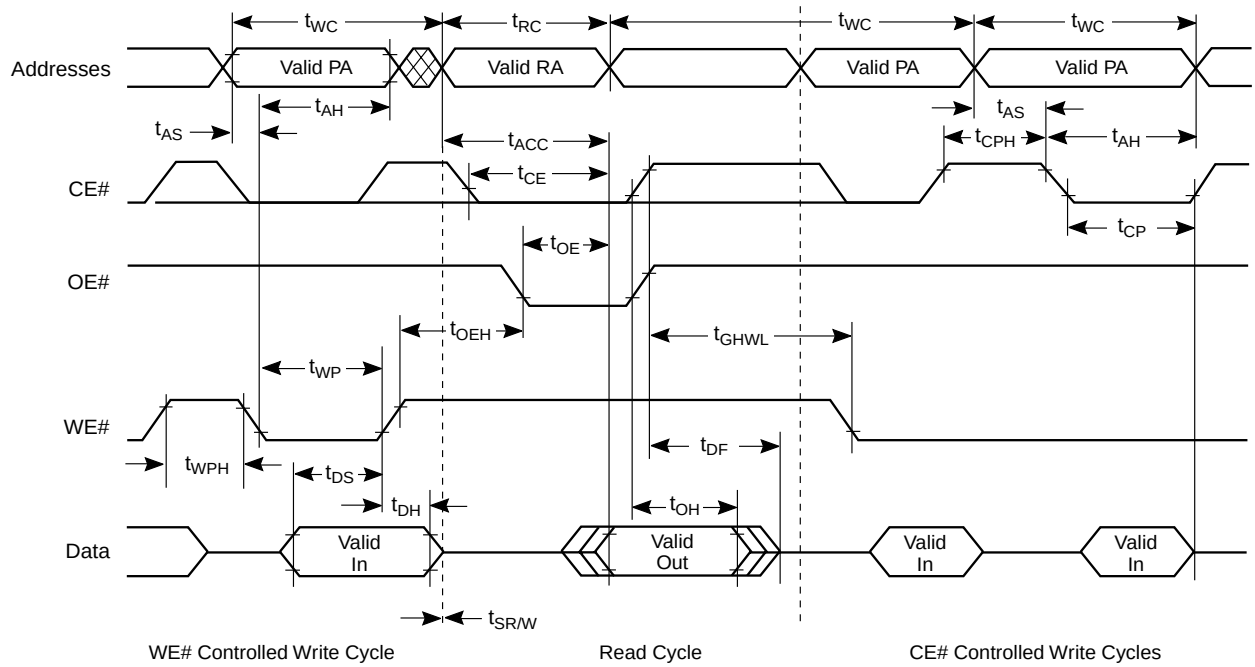
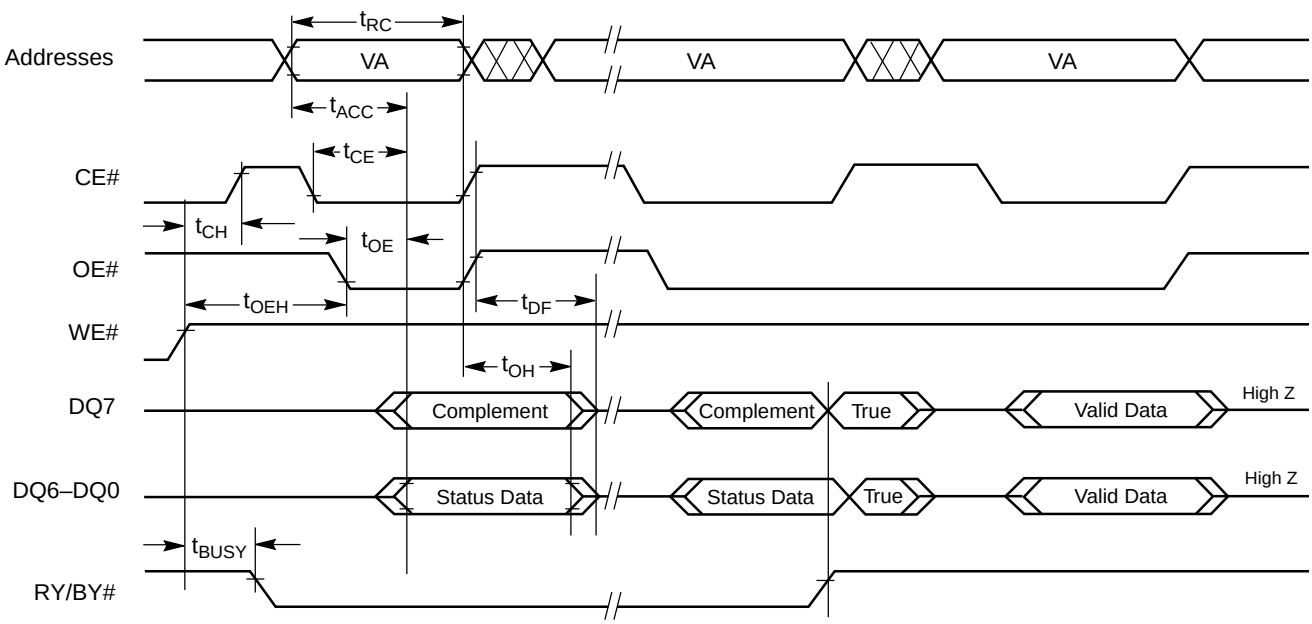


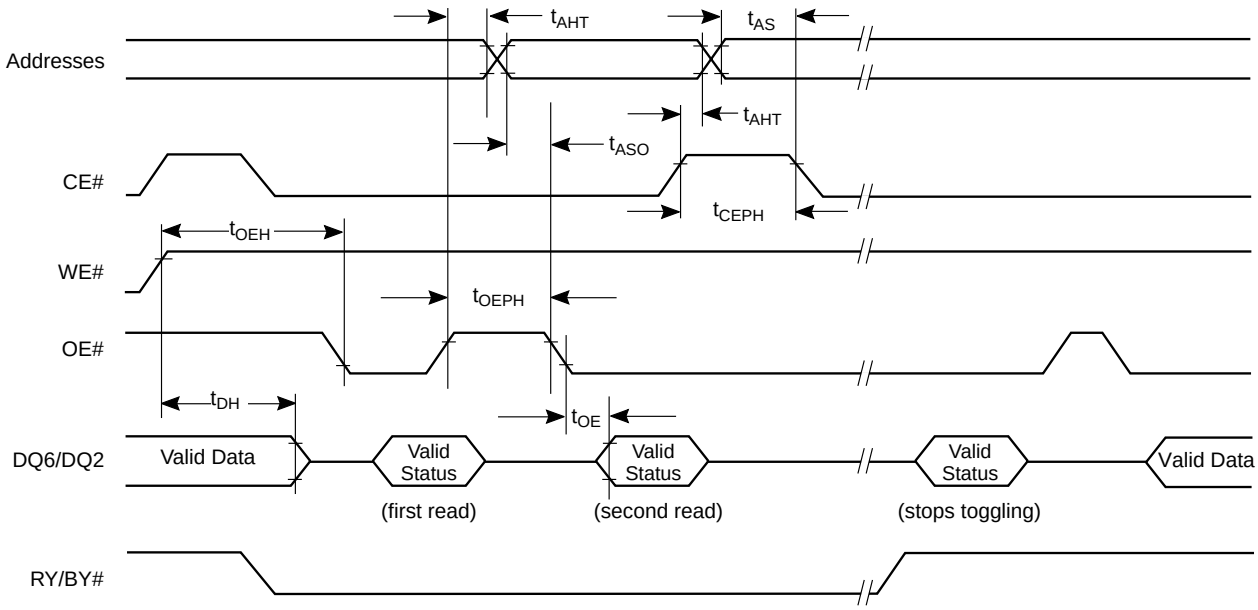
Figure 19. Back-to-back Read/Write Cycle Timings



Note: *VA = Valid address. Illustration shows first status cycle after command sequence, last status read cycle, and array data read cycle.*

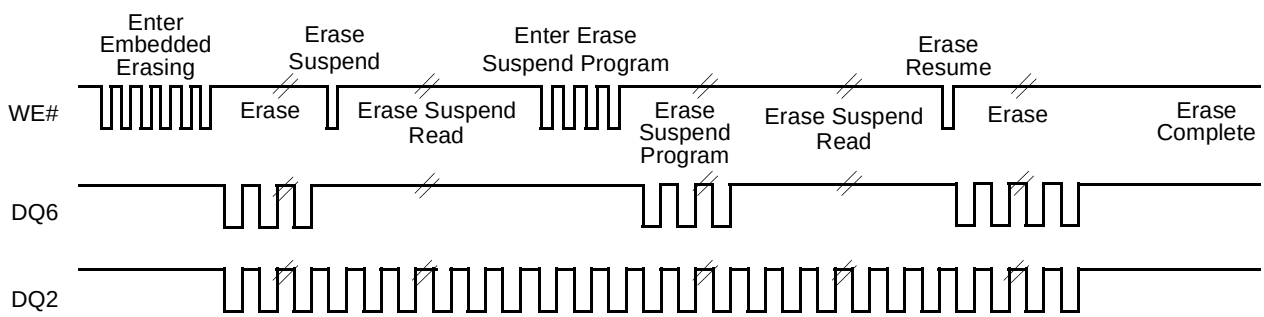
Figure 20. Data# Polling Timings (During Embedded Algorithms)

AC CHARACTERISTICS



Note: *VA = Valid address; not required for DQ6. Illustration shows first two status cycle after command sequence, last status read cycle, and array data read cycle*

Figure 21. Toggle Bit Timings (During Embedded Algorithms)



Note: *DQ2 toggles only when read at an address within an erase-suspended sector. The system may use OE# or CE# to toggle DQ2 and DQ6.*

Figure 22. DQ2 vs. DQ6

AC CHARACTERISTICS

Temporary Sector Unprotect

Parameter					
JEDEC	Std	Description		All Speed Options	Unit
	t_{VIDR}	V_{ID} Rise and Fall Time (See Note)	Min	500	ns
	t_{VHH}	V_{HH} Rise and Fall Time (See Note)	Min	250	ns
	t_{RSP}	RESET# Setup Time for Temporary Sector Unprotect	Min	4	µs
	t_{RRB}	RESET# Hold Time from RY/BY# High for Temporary Sector Unprotect	Min	4	µs

Note: *Not 100% tested.*

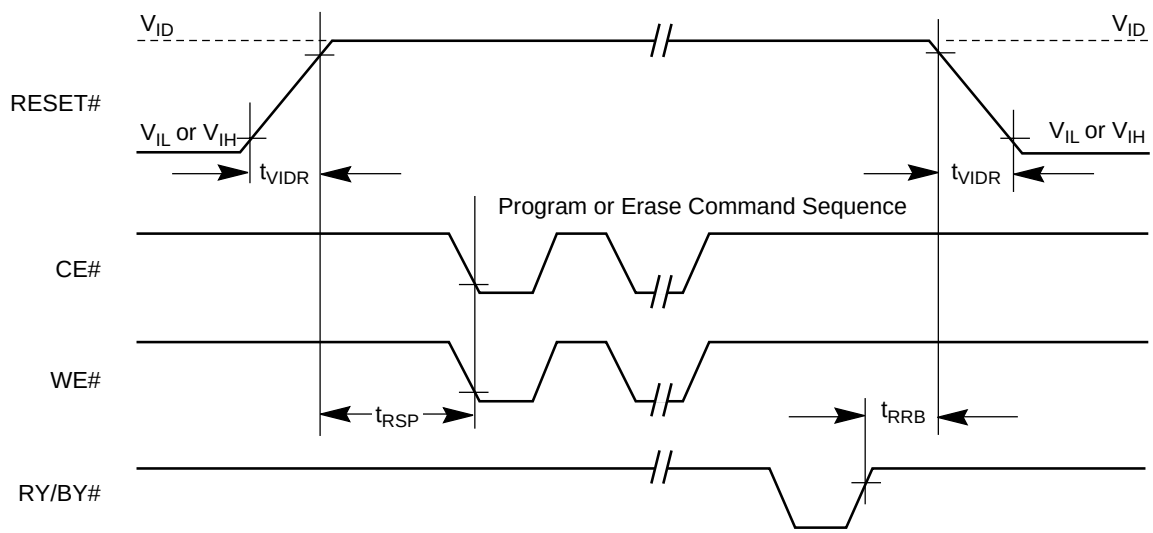
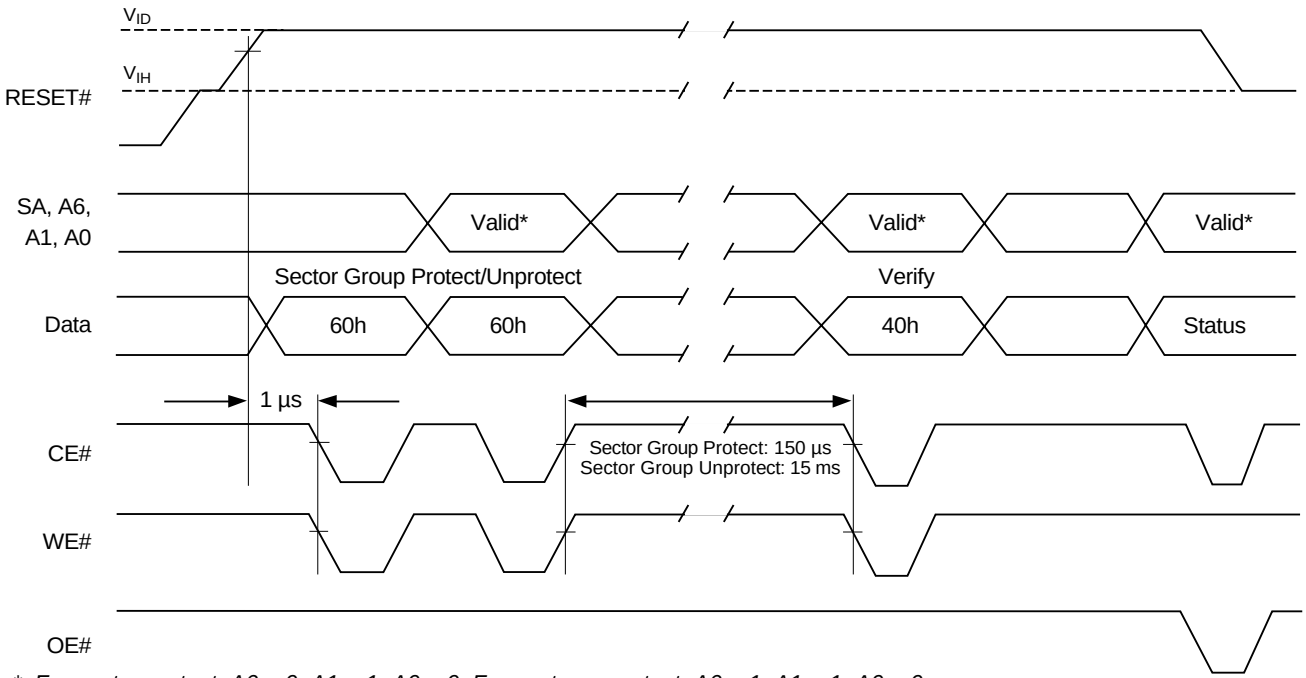


Figure 23. Temporary Sector Unprotect Timing Diagram

AC CHARACTERISTICS



* *For sector protect, A6 = 0, A1 = 1, A0 = 0. For sector unprotect, A6 = 1, A1 = 1, A0 = 0.*

Figure 24. Sector/Sector Block Protect and Unprotect Timing Diagram

AC CHARACTERISTICS

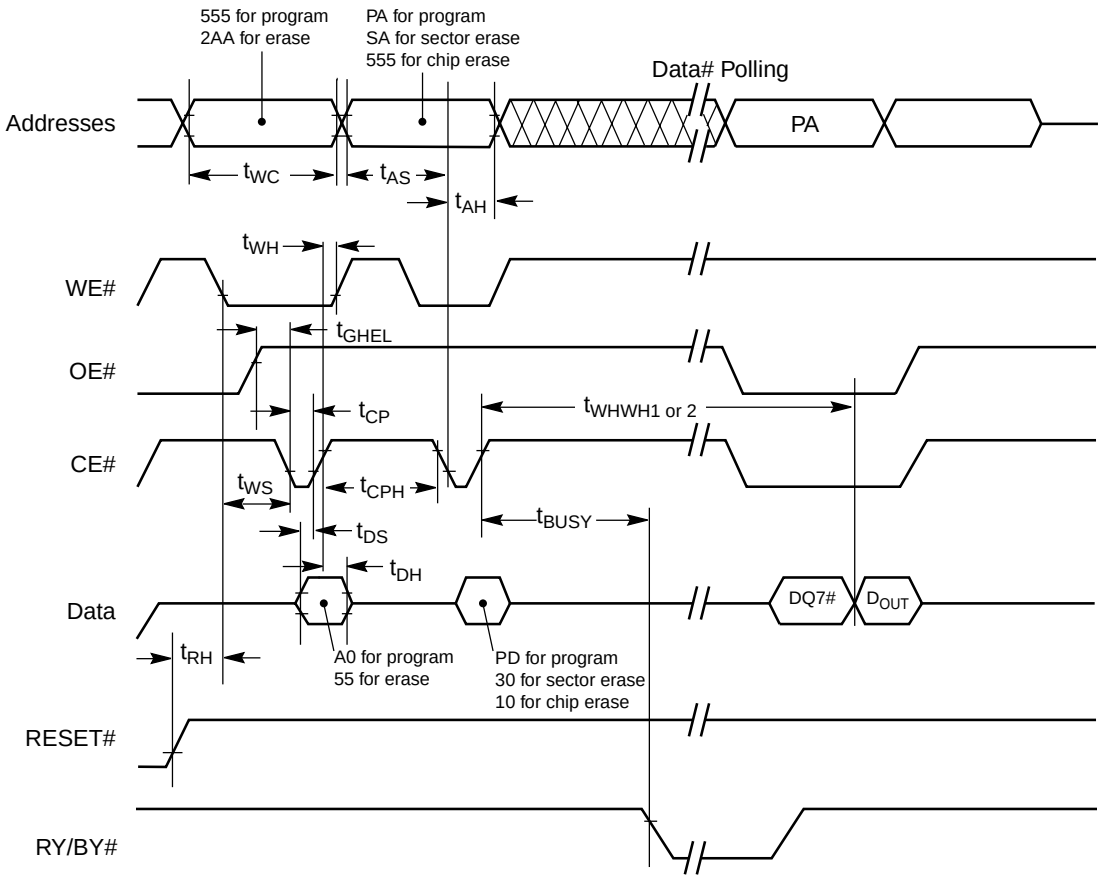
Alternate CE# Controlled Erase and Program Operations

Parameter		Description			Speed Options			Unit
JEDEC	Std.				70R, 70	80	90	
t_{AVAV}	t_{WC}	Write Cycle Time (Note 1)		Min	70	80	90	ns
t_{AVWL}	t_{AS}	Address Setup Time		Min	0			ns
t_{ELAX}	t_{AH}	Address Hold Time		Min	45	45	45	ns
t_{DVEH}	t_{DS}	Data Setup Time		Min	35	45	45	ns
t_{EHDX}	t_{DH}	Data Hold Time		Min	0			ns
t_{GHEL}	t_{GHEL}	Read Recovery Time Before Write (OE# High to WE# Low)		Min	0			ns
t_{WLEL}	t_{WS}	WE# Setup Time		Min	0			ns
t_{EHWH}	t_{WH}	WE# Hold Time		Min	0			ns
t_{ELEH}	t_{CP}	CE# Pulse Width		Min	35			ns
t_{EHEL}	t_{CPH}	CE# Pulse Width High		Min	30			ns
t_{WHWH1}	t_{WHWH1}	Programming Operation (Note 2)	Word	Typ	8.6			µs
			Double Word	Typ	12.6			
t_{WHWH1}	t_{WHWH1}	Accelerated Programming Operation, Double Word or Word (Note 2)		Typ	4			µs
t_{WHWH2}	t_{WHWH2}	Sector Erase Operation (Note 2)		Typ	0.2			sec

Notes:

1. *Not 100% tested.*
2. *See the “Erase And Programming Performance” section for more information.*

AC CHARACTERISTICS



Notes:

1. *Figure indicates last two bus cycles of a program or erase operation.*
2. *PA = program address, SA = sector address, PD = program data.*
3. *DQ7# is the complement of the data written to the device. D_{OUT} is the data written to the device.*
4. *Waveforms are for the word mode.*

Figure 25. Alternate CE# Controlled Write (Erase/Program) Operation Timings

ERASE AND PROGRAMMING PERFORMANCE

Parameter		Typ (Note 1)	Max (Note 2)	Unit	Comments
Sector Erase Time		0.2	TBD	sec	Excludes 00h programming prior to erasure (Note 4)
Chip Erase Time		54		sec	
Double Word Program Time		12.6	TBD	µs	Excludes system level overhead (Note 5)
Word Program Time		8.6	TBD	µs	
Accelerated Double Word Program Time		4	TBD		
Accelerated Word Program Time		4	TBD	µs	
Chip Program Time (Note 3)	Double Word Mode	50.4	200	sec	
	Word Mode	TBD	TBD		

Notes:

1. *Typical program and erase times assume the following conditions: 25°C, 3.0 V V_{CC}, 1,000,000 cycles. Additionally, programming typicals assume checkerboard pattern.*
2. *Under worst case conditions of 90°C, V_{CC} = 2.7 V, 1,000,000 cycles.*
3. *The typical chip programming time is considerably less than the maximum chip programming time listed, since most bytes program faster than the maximum program times listed.*
4. *In the pre-programming step of the Embedded Erase algorithm, all bytes are programmed to 00h before erasure.*
5. *System-level overhead is the time required to execute the two- or four-bus-cycle sequence for the program command. See Tables 14–17 for further information on command definitions.*
6. *The device has a minimum erase and program cycle endurance of 1,000,000 cycles.*

LATCHUP CHARACTERISTICS

Description	Min	Max
Input voltage with respect to V_{SS} on all pins except I/O pins (including A9, OE#, and RESET#)	–1.0 V	13 V
Input voltage with respect to V_{SS} on all I/O pins	–1.0 V	V_{CC} + 1.0 V
V_{CC} Current	–100 mA	+100 mA

Note: *Includes all pins except V_{CC}. Test conditions: V_{CC} = 3.0 V, one pin at a time.*

TSOP PIN CAPACITANCE

Parameter Symbol	Parameter Description	Test Setup	Typ	Max	Unit
C_{IN}	Input Capacitance	V_{IN} = 0	6	7.5	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0	8.5	12	pF
C_{IN2}	Control Pin Capacitance	V_{IN} = 0	8	10	pF

Notes:

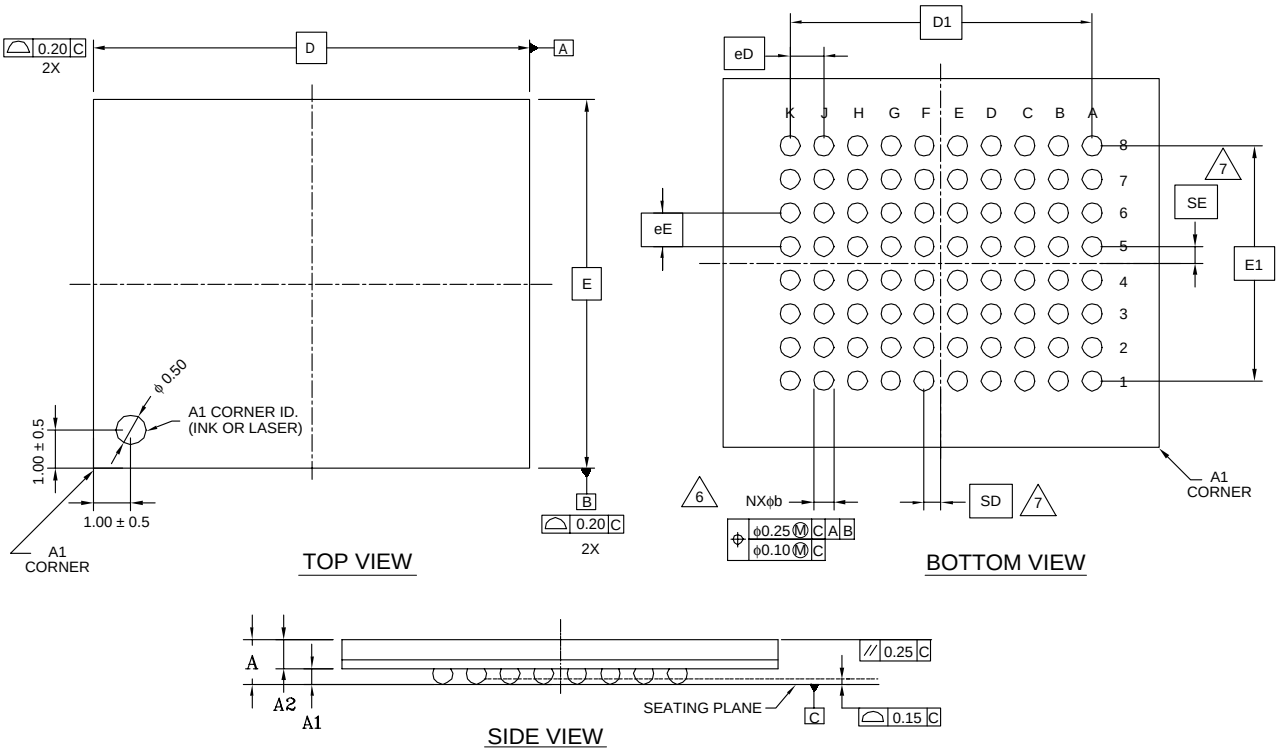
1. *Sampled, not 100% tested.*
2. *Test conditions T_A = 25°C, f = 1.0 MHz.*

DATA RETENTION

Parameter Description	Test Conditions	Min	Unit
Minimum Pattern Data Retention Time	150°C	10	Years
	125°C	20	Years

PHYSICAL DIMENSIONS

LAB080—80-Ball Fortified Ball Grid Array
10 x 15 mm package



PACKAGE	LAB 080			NOTE
JEDEC	N/A			
	15.00 mm x 10.00 mm PACKAGE			
SYMBOL	MIN.	NOM.	MAX.	
A	---	---	1.40	PROFILE HEIGHT
A1	0.40	---	---	STANDOFF
A2	0.60	---	---	BODY THICKNESS
D	15.00 BSC.			BODY SIZE
E	10.00 BSC.			BODY SIZE
D1	9.00 BSC.			MATRIX FOOTPRINT
E1	7.00 BSC.			MATRIX FOOTPRINT
MD	10			MATRIX SIZE D DIRECTION
ME	8			MATRIX SIZE E DIRECTION
N	80			BALL COUNT
φb	0.50	0.60	0.70	BALL DIAMETER
eD	1.00 BSC.			BALL PITCH - D DIRECTION
eE	1.00 BSC.			BALL PITCH - E DIRECTION
SD/SE	0.50 BSC.			SOLDER BALL PLACEMENT
				DEPOPULATED SOLDER BALLS
	A			PACKAGE OUTLINE TYPE

NOTES UNLESS OTHERWISE SPECIFIED:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994 .
2. ALL DIMENSIONS ARE IN MILLIMETERS .
3. BALL POSITION DESIGNATION PER JESD 95-1, SPP-010 (EXCEPT AS NOTED).
4. e REPRESENTS THE SOLDER BALL GRID PITCH .
5. SYMBOL "MD" IS THE BALL ROW MATRIX SIZE IN THE "D" DIRECTION. SYMBOL "ME" IS THE BALL COLUMN MATRIX SIZE IN THE "E" DIRECTION. N IS THE TOTAL NUMBER OF SOLDER BALLS.
6. DIMENSION "b" IS MEASURED AT THE MAXIMUM BALL DIAMETER IN A PLANE PARALLEL TO DATUM C .
7. SD AND SE ARE MEASURED WITH RESPECT TO DATUMS A AND B AND DEFINE THE POSITION OF THE CENTER SOLDER BALL IN THE OUTER ROW. WHEN THERE IS AN ODD NUMBER OF SOLDER BALLS IN THE OUTER ROW PARALLEL TO THE D OR E DIMENSION, RESPECTIVELY, SD OR SE = 0.000.

   WHEN THERE IS AN EVEN NUMBER OF SOLDER BALLS IN THE OUTER ROW, SD OR SE = e/2
8. "+" INDICATES THE THEORETICAL CENTER OF DEPOPULATED BALLS.

REVISION SUMMARY

Revision A (October 29, 2001)

Initial release.

Revision A+1 (November 13, 2001)

Simultaneous Operation Block Diagram

Added drawing.

Table 13, Primary Vendor-Specific Extended Query

Corrected data for 4Dh and 4Eh addresses (double-word mode).

Physical Dimensions

Added LAB080 package drawing.

Revision A+2 (February 8, 2002)

Global

Added 90 ns speed option. At this speed, t_{DF} is 30 ns and t_{OH} is 5 ns. For all speeds, changed typical word programming time to 8.6 µs, and typical double word programming time to 12.6 µs.

Simultaneous Operation Block Diagram

Deleted BYTE# input.

Revision B (April 26, 2002)

Global

Added 70R (regulated voltage range) to speed options.

Ordering Information

Added “V” to package marking.

Device Bus Operations

Corrected sector size references in sector address table.

Password Protection Mode section: Clarified that first 8 bytes of SecSi Sector should be reserved for the password. Added description of using password and SecSi Sector concurrently.

SecSi Sector Flash Memory Region

Added section on using password and SecSi Sector concurrently.

Table 13, Primary Vendor-Specific Extended Query

Corrected data for addresses 4D and 4Eh.

Command Definitions

Deleted PPB Status Command section.

Password Program Command section: Modified first paragraph.

Password Unlock Command section: Modified second paragraph.

PPB Lock Bit Set Command section: Modified entire section.

Substantial modifications were made to the command definitions tables and notes, including the following: deleted the PPB Status command sequence; added bank address requirements to SecSi Sector command; separated memory array and sector protection command sequences for easier reference.

DC Characteristics

In Note 1 of the CMOS Compatible table, changed typical I_{CC} current from 2 to 4mA/MHz. Changed I_{CC1} typical and maximum read currents, added currents for 10 MHz operation. Added specifications for intra-page read current. Changed I_{CC6} typical current to 30 mA.

Trademarks

Copyright © 2002 Advanced Micro Devices, Inc. All rights reserved.

AMD, the AMD logo, and combinations thereof are registered trademarks of Advanced Micro Devices, Inc.

ExpressFlash is a trademark of Advanced Micro Devices, Inc.

Product names used in this publication are for identification purposes only and may be trademarks of their respective companies.