

# 8751H/8753H

Single-Chip 8-Bit Microcontroller

## MILITARY INFORMATION

### DISTINCTIVE CHARACTERISTICS

- Military Temperature Range  
– –55 to +125°C (Tc)
- 4K x 8 EPROM (8751); 8K x 8 EPROM (8753)
- 128 x 8 RAM
- 64K bytes Program Memory space
- 64K bytes Data Memory space
- Pin-compatible with entire 8051 Family
- Full-duplex programmable serial ports
- 32 I/O lines (four 8-bit ports)
- Supports Adaptive EPROM Programming
- EPROM Security Feature
- Two 16-bit Timer/Event counters

### GENERAL DESCRIPTION

The 8751H and 8753H are members of a family of advanced single-chip microcontrollers. Both the 8751H, which has 4K bytes of EPROM, and the 8753H, which has 8K bytes of EPROM, are pin-compatible EPROM versions of the 8051AH and 8053AH, respectively. Thus, the 8751H/8753H are full-speed prototyping tools which provide effective single-chip solutions for controller applications that require code modification flexibility. Refer to the block diagram of the 8051 family.

The 8751H/8753H devices feature: thirty-two I/O lines; two 16-bit timer/event counters; a Boolean processor, a 5-source, bi-level interrupt structure; a full-duplex serial channel; and on-chip oscillator and clock circuitry.

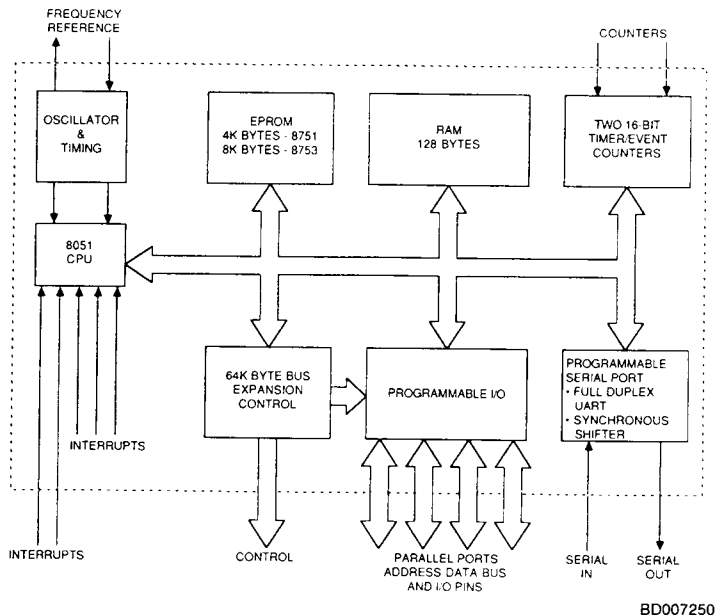
Program and Data Memory are located in independent addresses. The AMD family of microcontrollers can access up to 64K bytes of external Program Memory and up to 64K

bytes of external Data Memory. The 8751H and the 8753H contain the lower 4K and 8K bytes of Program Memory, respectively, on-chip. Both parts have 128 bytes of on-chip read/write data memory.

The AMD 8051 Microcontroller Family is specifically suited for control applications. A variety of fast addressing modes, which access the internal RAM, facilitates byte processing and numerical operations on small data structures. Included in the instruction set is a menu of 8-bit arithmetic instructions, including 4-cycle multiply and divide instructions.

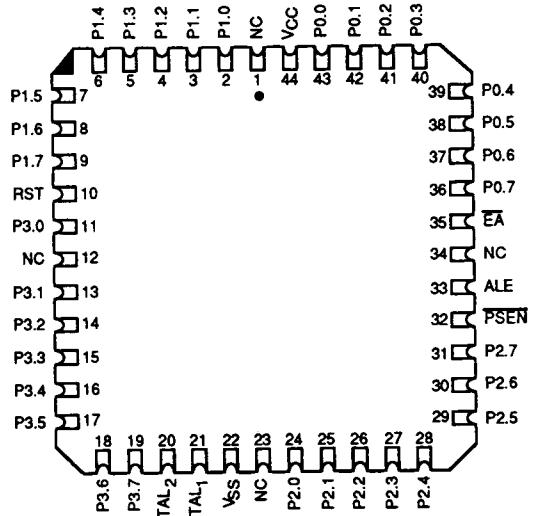
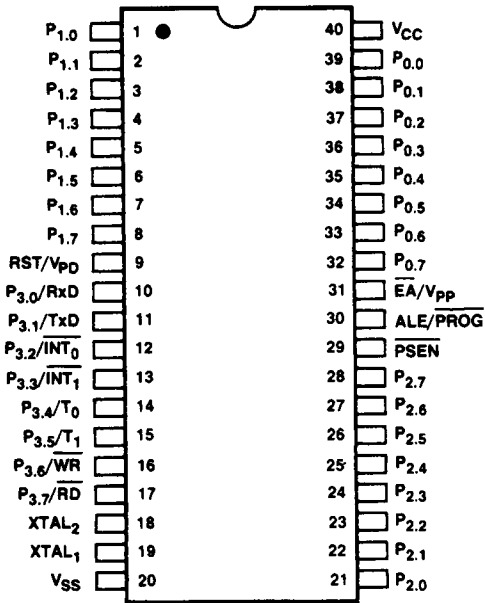
Extensive on-chip support enables direct bit manipulation and testing of 1-bit variables as separate data types. Thus, the device is also suited for control and logic systems that require Boolean processing.

### BLOCK DIAGRAM



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### CONNECTION DIAGRAMS Top View

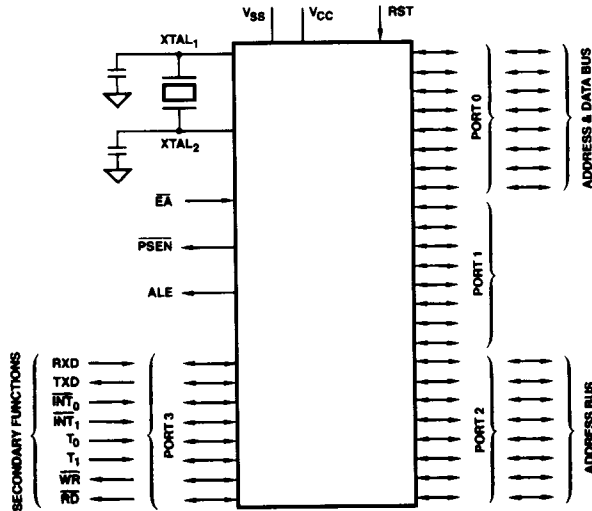


CD010870

CD005651

Note: Pin 1 is marked for orientation.

### LOGIC SYMBOL



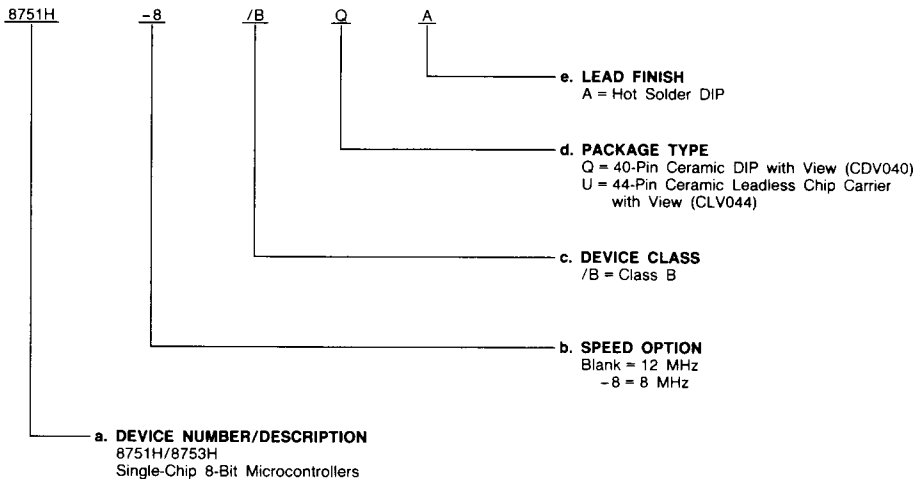
LS001325

# MILITARY ORDERING INFORMATION

## APL Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. APL (Approved Products List) products are fully compliant with MIL-STD-883C requirements. The order number (Valid Combination) is formed by a combination of:

- a. **Device Number**
- b. **Speed Option** (if applicable)
- c. **Device Class**
- d. **Package Type**
- e. **Lead Finish**



Valid Combinations	
8751H	/BQA, /BUA
8751H-8	
8753H	
8753H-8	

### Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations or to check for newly released valid combinations.

### Group A Tests

Group A tests consist of Subgroups 1, 2, 3, 7, 8, 9, 10, 11.

**ABSOLUTE MAXIMUM RATINGS**

Storage Temperature .....	-65 to +150°C
Voltage on Any Other Pin to V <sub>SS</sub> (Except V <sub>pp</sub> ) .....	-0.5 to +7.0 V
Voltage from V <sub>pp</sub> to V <sub>SS</sub> .....	-0.5 to +21.5 V
Power Dissipation .....	2 W

Stresses above those listed under **ABSOLUTE MAXIMUM RATINGS** may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

**OPERATING RANGES**

Military (M) Devices	
Temperature (T <sub>C</sub> ) .....	-55 to +125°C
Supply Voltage (V <sub>CC</sub> ) .....	+4.5 to +5.5 V
Ground (V <sub>SS</sub> ) .....	0 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

**DC CHARACTERISTICS** over operating range (for APL Products, Group A, Subgroups 1, 2, 3 are tested unless otherwise noted)

Parameter Symbol	Parameter Description	Test Conditions	Min.	Max.	Unit
V <sub>IL</sub> †	Input LOW Voltage		-0.5	0.7	V
V <sub>IL1</sub> †	Input LOW Voltage to $\bar{E}A$		0	0.7	V
V <sub>IH</sub> †	Input HIGH Voltage (Except XTAL <sub>2</sub> , RST)		2.2	V <sub>CC</sub> + 0.5	V
V <sub>IH1</sub> †	Input HIGH Voltage to XTAL <sub>2</sub> , RST	XTAL <sub>1</sub> = V <sub>SS</sub>	2.5	V <sub>CC</sub> + 0.5	V
V <sub>OL</sub>	Output LOW Voltage (Ports 1, 2, 3) (Note 1)	I <sub>OL</sub> = 1 mA		0.45	V
V <sub>OL1</sub>	Output LOW Voltage (Port 0, ALE, $\bar{P}SEN$ ) (Note 1)	I <sub>OL</sub> = 8 mA		0.60	V
		I <sub>OL</sub> = 2.4 mA		0.45	V
V <sub>OH</sub>	Output HIGH Voltage (Ports 1, 2, 3)	I <sub>OH</sub> = -60 μA	2.4		V
V <sub>OH1</sub>	Output HIGH Voltage (Port 0 in External Bus Mode, ALE, $\bar{P}SEN$ )	I <sub>OH</sub> = -300 μA	2.4		V
I <sub>IL</sub>	Logical 0 Input Current P1, P2, P3	V <sub>IN</sub> = 0.45 V		-500	μA
I <sub>IL1</sub>	Logical 0 Input Current to $\bar{E}A/V_{pp}$	V <sub>IN</sub> = 0.45 V		-15	mA
I <sub>IL2</sub>	Logical 0 Input Current to XTAL <sub>2</sub>	XTAL <sub>1</sub> = V <sub>SS</sub> , V <sub>IN</sub> = 0.45 V		-4.5	mA
I <sub>LI</sub>	Input Leakage Current to Port 0	0.45 < V <sub>IN</sub> < V <sub>CC</sub>		±100	μA
I <sub>IH</sub>	Logical Input Current to $\bar{E}A/V_{pp}$	V <sub>IN</sub> = 2.4 V		500	μA
I <sub>IH1</sub>	Input Current to RST/ $\bar{V}_{pp}$ to Activate Reset	V <sub>IN</sub> < (V <sub>CC</sub> - 1.5 V)		500	μA
I <sub>CC</sub>	Power Supply Current (Note 3)	All Outputs Disconnected, EA = V <sub>CC</sub>		275	mA
C <sub>IO</sub> ††	Capacitance of I/O Buffers	f <sub>C</sub> = 1 MHz, T <sub>A</sub> = 25°C		30*	pF
I <sub>PD</sub>	Power-Down Current (Note 2)	T <sub>A</sub> = 25°C, V <sub>PD</sub> = 5.0 V, V <sub>CC</sub> = 0 V		10	mA

- Notes: 1. Capacitive loading on Ports 0 and 2 may cause spurious noise pulses to be superimposed on the V<sub>OL</sub>s of ALE and Ports 1 and 3. The noise is due to external bus capacitance discharging into the Port 0 and Port 2 pins when these pins make 1-to-0 transitions during bus operations. In the worst cases (capacitive loading > 100 pF), the noise pulse on the ALE line may exceed 0.8 V. In such cases it may be desirable to qualify ALE with a Schmitt Trigger, or use an address latch with a Schmitt Trigger STROBE input.
2. Power-Down I<sub>CC</sub> is measured with all output pins disconnected;  $\bar{E}A = V_{CC} = 0$ ; XTAL<sub>2</sub> = N.C.; RST = V<sub>PD</sub> = 5.0 V.
3. I<sub>CC</sub> is measured with all output pins disconnected; XTAL<sub>1</sub> driven with t<sub>CLCH</sub>, t<sub>CHCL</sub> = 5 ns; V<sub>IL</sub> = V<sub>SS</sub> + 5 V; V<sub>IH</sub> = V<sub>CC</sub> - 5 V; XTAL<sub>2</sub> = N.C.; EA = RST = V<sub>CC</sub>.

† Group A, Subgroups 7 and 8 only are tested.

†† Not included in Group A tests.

\* Not tested; guaranteed by design.

**SWITCHING CHARACTERISTICS** over operating range (for APL Products, Group A, Subgroups 9, 10, 11 are tested unless otherwise noted)

(Load Capacitance for Port 0, ALE, and PSEN = 100 pF, Load Capacitance for All Other Outputs = 80 pF)

### External Program Memory Characteristics

Parameter Symbol	Parameter Description	12-MHz Osc.		8-MHz Osc.		Variable Oscillator		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
1/t <sub>CLCL</sub>	Oscillator Frequency	3.5	12	3.5	8	3.5	12	MHz
t <sub>LHLL</sub>	ALE Pulse Width	112		195		2t <sub>CLCL</sub> -55		ns
t <sub>AVLL</sub>	Address Setup to ALE	28		70		t <sub>CLCL</sub> -55		ns
t <sub>LLAX</sub>	Address Hold After ALE	33		75		t <sub>CLCL</sub> -50		ns
t <sub>LLIV</sub>	ALE to Valid Instr In		168		335		4t <sub>CLCL</sub> -165	ns
t <sub>LLPL</sub>	ALE to PSEN	43		85		t <sub>CLCL</sub> -40		ns
t <sub>PLPH</sub>	PSEN Pulse Width	175		300		3t <sub>CLCL</sub> -75		ns
t <sub>PLIV</sub>	PSEN to Valid Instr In		85		210		3t <sub>CLCL</sub> -165	ns
t <sub>PXIX</sub>	Input Instr Hold After PSEN	0		0		0		ns
t <sub>PXIZ</sub>	Input Instr Float After PSEN		48		90		t <sub>CLCL</sub> -35	ns
t <sub>PXAV</sub>	Address Valid After PSEN	58		100		t <sub>CLCL</sub> -25		ns
t <sub>AVIV</sub>	Address to Valid Instr In		252		460		5t <sub>CLCL</sub> -165	ns
t <sub>PLAZ</sub>	Addr Float After PSEN		20		20		20	ns

### External Data Memory Characteristics

Parameter Symbol	Parameter Description	12-MHz Osc.		8-MHz Osc.		Variable Oscillator		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
t <sub>RLRH</sub>	RD Pulse Width	400		650		6t <sub>CLCL</sub> -100		ns
t <sub>WLWH</sub>	WR Pulse Width	400		650		6t <sub>CLCL</sub> -100		ns
t <sub>LLAX</sub>	Address Hold After ALE			75		t <sub>CLCL</sub> -50		ns
t <sub>RLDV</sub>	RD to Valid Data In		232		440		5t <sub>CLCL</sub> -185	ns
t <sub>RHDX</sub>	Data Hold After RD			0		0		ns
t <sub>RHDZ</sub>	Data Float After RD		82		165		2t <sub>CLCL</sub> -85	ns
t <sub>LLDV</sub>	ALE to Valid Data In		496		830		8t <sub>CLCL</sub> -170	ns
t <sub>AVDV</sub>	Address to Valid Data In		565		940		9t <sub>CLCL</sub> -185	ns
t <sub>LLWL</sub>	ALE to RD or WR	185	315	310	440	3t <sub>CLCL</sub> -65	3t <sub>CLCL</sub> +65	ns
t <sub>AVWL</sub>	Address to RD or WR	188		355		4t <sub>CLCL</sub> -145		ns
t <sub>QVWX</sub>	Data Valid to WR High Z	0		40		t <sub>CLCL</sub> -85		ns
t <sub>QVWH</sub>	Data Setup Before WR	508		800		7t <sub>CLCL</sub> -75		ns
t <sub>WHQX</sub>	Data Hold After WR	18		60		t <sub>CLCL</sub> -65		ns
t <sub>RLAZ</sub>	Address Float After RD		20		20		20	ns
t <sub>WHLH</sub>	RD or WR HIGH to ALE HIGH	18	148	60	190	t <sub>CLCL</sub> -65	t <sub>CLCL</sub> +65	ns

### External Clock Drive\*

Parameter Symbol	Parameter Description	Min.	Max.	Unit
1/t <sub>CLCL</sub>	Oscillator Frequency	1.2	12	MHz
t <sub>CHCX</sub>	HIGH Time	20		ns
t <sub>CLCX</sub>	LOW Time	20		ns
t <sub>CLCH</sub>	Rise Time		20	ns
t <sub>CHCL</sub>	Fall Time		20	ns

\*Not tested; these specs are controlled by the Teradyne J941, J983 tester.

**SWITCHING CHARACTERISTICS (Cont'd.)**  
**Serial Port Timing — Shift Register Mode** ( $C_L = 8 \text{ pF}$ )

Parameter Symbol	Parameter Description	12-MHz Osc.		8-MHz Osc.		Variable Oscillator		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
t <sub>XLXL</sub>	Serial Port Clock Cycle Time	1.0		1.0		12t <sub>CLCL</sub>		μs
t <sub>QVXH</sub>	Output Data Setup to Clock Rising Edge	700		1117		10t <sub>CLCL</sub> -133		ns
t <sub>XHOX</sub>	Output Data Hold After Clock Rising Edge	49		133		2t <sub>CLCL</sub> -117		ns
t <sub>XHDX</sub>	Input Data Hold After Clock Rising Edge	0		0		0		ns
t <sub>XHDV</sub>	Clock Rising Edge to Input Data Valid		700	1117			10t <sub>CLCL</sub> -133	ns

**EPROM Programming and Verification Characteristics**  
 ( $T_A = +21 \text{ to } +27^\circ\text{C}$ ,  $V_{CC} = +5 \text{ V} \pm 10\%$ ,  $V_{SS} = 0 \text{ V}$ )

Parameter Symbol	Parameter Description	Min.	Max.	Unit
V <sub>pp</sub>	Programming Supply Voltage	20.5	21.5	V
I <sub>pp</sub>	Programming Supply Current		30	mA
1/t <sub>CLCL</sub>	Oscillator Frequency	4	6	MHz
t <sub>AVGL</sub>	Address Setup to PROG	48t <sub>CLCL</sub>		
t <sub>GHAX</sub>	Address Hold After PROG	48t <sub>CLCL</sub>		
t <sub>DVGL</sub>	Data Setup to PROG	48t <sub>CLCL</sub>		
t <sub>GHDX</sub>	Data Hold After PROG	48t <sub>CLCL</sub>		
t <sub>ESH</sub>	P <sub>2,7</sub> (ENABLE) Float to V <sub>pp</sub>	48t <sub>CLCL</sub>		
t <sub>SHGL</sub>	V <sub>pp</sub> Setup to PROG	10		μs
t <sub>GHSL</sub>	V <sub>pp</sub> Hold after PROG	10		μs
t <sub>GLGH</sub>	PROG Width	45	55	ms
t <sub>AVQV</sub>	Address to Data Valid		48t <sub>CLCL</sub>	
t <sub>ELQV</sub>	ENABLE to Data Valid		48t <sub>CLCL</sub>	
t <sub>EHQZ</sub>	Data Float After ENABLE	0	48t <sub>CLCL</sub>	

\*Not tested; guaranteed by design.