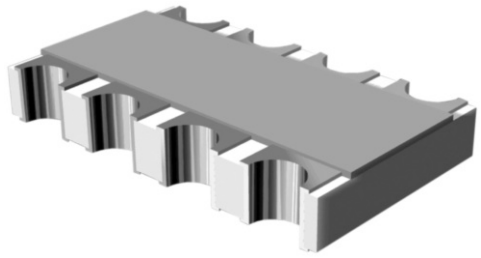
Precision Thin Film Chip Resistor Array



FEATURES

- Advanced thin film technology
- Two pairs or four equal resistor values
- TCR tracking down to 10 ppm/K (± 5 ppm/K)
- Tolerance matching down to 0.1 % (± 0.05 %)
- Pure Sn termination on Ni barrier layer
- RoHS compliant component, compatible with lead (Pb)-free and lead containing soldering processes

RoHS COMPLIANT

ACAC 0612 thin chip resistor arrays with concave terminations combine the proven reliability of precision thin film chip resistor products with the advantages of chip arrays. Defined tolerance matching and TCR tracking makes this product perfectly suited for applications with outstanding requirements towards stable fixed resistor ratios. A small package enables the design of high density circuits in combination with reduction of assembly costs. Four equal resistors values or two pairs are available.

APPLICATIONS

- Precision analogue circuits
- Voltage divider
- Feedback circuits
- Signal conditioning

TECHNICAL SPECIFICATIONS	
DESCRIPTION	**ACAC 0612**
EIA size	0612
Metric size	RR1632M
Configuration, isolated	4 x 0603
Design: All Equal Two Pairs	 AE TP
Resistance values	47 Ω to 221 kΩ (1)
Absolut tolerance	± 0.5 %; ± 0.25 %
Tolerance matching	0.5 % (equivalent to ± 0.25 %) 0.25 % (equivalent to ± 0.125 %) 0.1 % (equivalent to ± 0.05 %)
Absolut temperature coefficient	± 50 ppm/K; ± 25 ppm/K
Temperature coefficient tracking	25 ppm/K (equivalent to ± 12.5 ppm/K) 15 ppm/K (equivalent to ± 7.5 ppm/K) 10 ppm/K (equivalent to ± 5 ppm/K)
Max. resistance ratio $R_{min.}/R_{max.}$	1:5
Climatic category (LCT/UCT/duration)	- 55 °C/+ 125 °C/56 days
Rated dissipation: P_{70} (2) Element Package, 4 x 0603	 0.1 W 0.3 W
Operating voltage	75 V
Film temperature	125 °C
Insulation voltage (U_{ins}) against ambient and between isolated resistors, continuous	75 V

Notes

(1) Resistance values to be selected from E24, E48 or E96

(2) The power dissipation on the resistor generates a temperature rise against the local ambient, depending on the heat-flow support of the printed circuit board (thermal resistance). The rated dissipation applies only if the permitted film temperature is not exceeded. Furthermore, a high level of ambient temperature or of power dissipation may raise the temperature of the solder joint, hence special solder alloys or board materials may be required to maintain the reliability of the assembly.

- These resistors do not feature a limited lifetime when operated within the permissible limits. However, resistance value drift increasing over operating time may result in exceeding a limit acceptable to the specific application, thereby establishing a functional lifetime.

PART NUMBER AND PRODUCT DESCRIPTION (1)

PART NUMBER: ACAC06P0830000P500

A	C	A	C	0	6	P	0	8	3	0	0	0	0	P	5	0	0

MODEL	SIZE	TERMINAL	PIN	SCHEMATIC	DESIGN NUMBER	PACKAGING (2)	SPECIAL
ACAC	**06**	**P** = Concave	**08** = 8 Pins	**3** = 03	**Design number is available on request**	**P1** **P5** **PW**	**00** = Standard

PRODUCT DESCRIPTION: ACAC 0000 TP P5

ACA	C	0000	TP	P5
MODEL	**TERMINATION**	**DESIGN NUMBER**	**DESIGN**	**PACKAGING (2)**
ACA = Chip Array	**C** = Concave	**Design number is available on request**	**AE =** All Equal **TP =** Two Pairs (3)	**P1** **P5** **PW**

Notes

(1) Products can be ordered using either the PART NUMBER or the PRODUCT DESCRIPTION

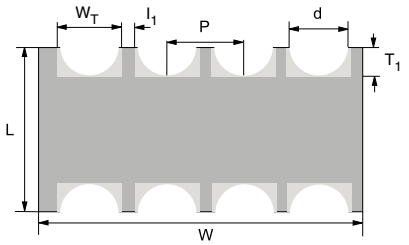
(2) Please refer to table PACKAGING, see below

(3) Different values (DF) are available on request

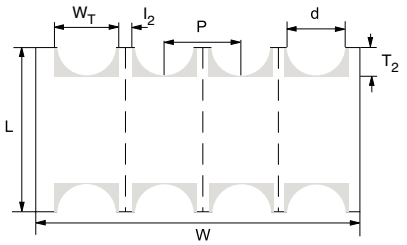
PACKAGING

MODEL	TAPE WIDTH	DIAMETER	PIECES	PITCH	PACKAGING CODE
					PAPER TAPE
ACAC 0612	8 mm	180 mm/7"	1000	4 mm	P1
	8 mm	180 mm/7"	5000	4 mm	P5
	8 mm	330 mm/13"	10 000	4 mm	PW

DIMENSIONS



Top view



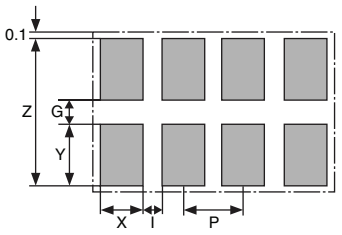
Bottom view

DIMENSIONS - chip resistor array, mass and relevant physical dimensions

TYPE	L (mm)	W (mm)	H (mm)	P (mm)	W_T (mm)	T_1 (mm)	T_2 (mm)	d (mm)	I_1 (mm)	I_2 (mm)	MASS (mg)
ACAC 0612	1.6 ± 0.15	3.2 ± 0.15	0.55 ± 0.1	0.8 ± 0.1	0.5 ± 0.15	0.3 ± 0.15	0.4 ± 0.15	0.3 ± 0.1	min. 0.15	min. 0.25	9.41

PATTERN STYLES FOR CHIP RESISTOR ARRAYS

Dimensions in mm



limits for solder resistance

occupied area

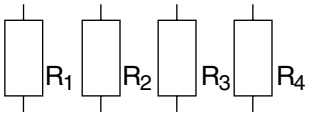
RECOMMENDED SOLDER PAD DIMENSIONS FOR CHIP RESISTOR ARRAYS						
TYPE	G (mm)	Y (mm)	X (mm)	Z (mm)	I (mm)	P (mm)
ACAC 0612	0.7	0.7	0.5	2.1	0.3	0.8

TEMPERATURE COEFFICIENT AND RESISTANCE RANGE				
DESCRIPTION				RESISTANCE VALUE
ABSOLUTE TCR	TCR TRACKING (1)	ABSOLUTE TOLERANCE	TOLERANCE MATCHING (1)	ACAC 0612
± 25 ppm/K	10 ppm/K	± 0.25 %	0.1 %	47 Ω to 221 kΩ
± 25 ppm/K	10 ppm/K	± 0.5 %	0.25 %	47 Ω to 221 kΩ
± 25 ppm/K	15 ppm/K	± 0.25 %	0.1 %	47 Ω to 221 kΩ
± 25 ppm/K	15 ppm/K	± 0.5 %	0.25 %	47 Ω to 221 kΩ
± 25 ppm/K	25 ppm/K	± 0.25 %	0.1 %	47 Ω to 221 kΩ
± 25 ppm/K	25 ppm/K	± 0.5 %	0.25 %	47 Ω to 221 kΩ
± 50 ppm/K	25 ppm/K	± 0.5 %	0.5 %	47 Ω to 221 kΩ

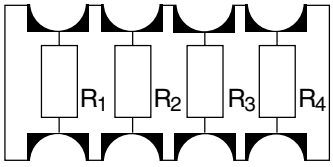
Note

(1) In applications with defined resistance ratios like voltage dividers or feedback circuits, an array with a defined tracking of e.g. 10 ppm/K is required to replace discrete resistors with a temperature coefficient of ± 5 ppm/K. Furthermore, in order to achieve the same tolerance of ± 0.05 % of individual resistors, an array requires a matching of 0.1 %.

APPLICATION INFORMATION



Circuit Type 03



Array configuration

DESCRIPTION

The production of the components is strictly controlled and follows an extensive set of instructions established for reproducibility. A homogeneous film of metal alloy is deposited on a high grade (96 % Al_2O_3) ceramic substrate and conditioned to achieve the desired temperature coefficient. Specially designed inner contacts are realised on both sides. A special laser is used to achieve the target value by smoothly cutting a meander groove in the resistive layer without damaging the ceramics.

The resistor elements are covered by a protective coating designed for electrical, mechanical and climatic protection. The terminations receive a final pure tin on nickel plating.

The result of the determined production is verified by an extensive testing procedure and optical inspection performed on 100 % of the individual chip resistors. Only accepted products are laid directly into the paper tape in accordance with **IEC 60286-3*.**

ASSEMBLY

The resistors are suitable for processing on automatic SMD assembly systems and for automatic soldering using wave, reflow or vapour phase as shown in **IEC 61760-1***. The encapsulation is resistant to all cleaning solvents commonly used in the electronics industry, including alcohols, esters and aqueous solutions.

The suitability of conformal coatings, if applied, shall be qualified by appropriate means to ensure the long-term stability of the whole system. The resistors are RoHS compliant; the pure tin plating provides compatibility with lead (Pb)-free and lead-containing soldering processes. The permitted storage time is 20 years, whereas the solderability is specified for 2 years after production or requalification. The immunity of the plating against tin whisker growth has been proven under extensive testing.

All products comply with the **GADSL** (1) and the **CEFIC-EECA-EICTA** (2) list of legal restrictions on hazardous substances. This includes full compliance with the following directives:

- 2000/53/EC End of Vehicle life Directive (ELV) an Annex II (ELV II)
- 2002/95/EC Restriction of the use of Hazardous Substances directive (RoHS)
- 2002/96/EC Waste Electrical and Electronic Equipment Directive (WEEE)

APPROVALS

Where applicable, the resistors are tested in accordance with **EN 140401-801** which refers to **EN 60115-1** and **EN 140400**.

Notes

(1) Global Automotive Declarable Substance List, see www.gadsl.org

(2) CEFIC (European Chemical Industry Council), EECA (European Electronic Component Manufacturers Association), EICTA (European trade organisation representing the information and communications technology and consumer electronics), see www.eicta.org → issues → environment policy → chemicals → chemicals for electronics

- The quoted IEC standards marked with an asterisk (*) are also released as EN standards with the same number and identical contents

TESTS AND REQUIREMENTS

Essentially all tests are carried out in accordance with the following specifications:

EN 60115-1, Generic specification (includes tests)

EN 140400, Sectional specification (includes schedule for qualification approval)

The testing also covers most of the requirements specified by EIA/IS-703 and JIS-C-5202.

The tests are carried out in accordance with IEC 60068* and under standard atmospheric conditions according to IEC 60068-1*, 5.3. Climatic category LCT/UCT/56 (rated temperature range: Lower Category Temperature, Upper Category Temperature; damp heat, long term, 56 days) is valid.

Unless otherwise specified the following values apply:

Temperature: 15 °C to 35 °C

Relative humidity: 45 % to 75 %

Air pressure: 86 kPa to 106 kPa (860 mbar to 1060 mbar)

In the following table only the tests and requirements are listed with reference to the relevant clauses of EN 60115-1 and IEC 60068-2*; a short description of the test procedure is also given.

TEST PROCEDURES AND REQUIREMENTS

EN 60115-1 CLAUSE	IEC 60068-2* TEST METHOD	TEST	PROCEDURE	REQUIREMENTS (1) PERMISSIBLE CHANGE (ΔR)
			Stability for product types: **ACAC 0612**	47 Ω to 221 kΩ
4.5	-	Resistance	-	± 0.5 %; ± 0.25 %
4.8.4.2	-	Temperature coefficient	At 20/LCT/ 20 °C and 20/UCT/20 °C	± 50 ppm/K; ± 25 ppm/K
4.25.1	-	Endurance	$U = \sqrt{P_{70} \times R}$ or $U = U_{max.}$; 1.5 h on; 0.5 h off; 70 °C; 1000 h	± (0.25 % R + 0.05 Ω)

TEST PROCEDURES AND REQUIREMENTS

EN 60115-1 CLAUSE	IEC 60068-2* TEST METHOD	TEST	PROCEDURE	REQUIREMENTS (1) PERMISSIBLE CHANGE (ΔR)
			Stability for product types: **ACAC 0612**	47 Ω to 221 kΩ
4.25.3	-	Endurance at upper category temperature	125 °C; 1000 h	± (0.25 % R + 0.05 Ω)
4.24	78 (Cab)	Damp heat, steady state	(40 ± 2) °C; 56 days; (93 ± 3) % RH	± (0.25 % R + 0.05 Ω)
4.13	-	Short time overload (2)	$U = 2.5 \times \sqrt{P_{70} \times R}$ or $U = 2 \times U_{max.}$; 5 s	± (0.1 % R + 0.01 Ω) no visible damage
4.19	14 (Na)	Rapid change of temperature	30 min at LCT and 30 min at UCT; 5 cycles	± (0.1 % R + 0.01 Ω) no visible damage
4.18.2	58 (Td)	Resistance to soldering heat	Reflow method 2 (IR/forced gas convention); (260 ± 5) °C; (10 ± 1) s	± (0.1 % R + 0.01 Ω) no visible damage
4.17.2	58 (Td)	Solderability	Solder bath method; SnPb; non-activated flux accelerated ageing 4 h/155 °C (215 ± 3) °C; (3 ± 0.3) s	Good tinning (≥ 95 % covered); no visible damage
			Solder bath method; SnAgCu; non-activated flux accelerated ageing 4 h/155 °C (245 ± 3) °C; (3 ± 0.3) s	
4.32	21 (Ue_3)	Shear (adhesion)	45 N	No visible damage
4.33	21 (Ue_1)	Substrate bending	Depth 2 mm, 3 times	± (0.1 % R + 0.01 Ω) no visible damage; no open circuit in bent position
4.7	-	Voltage proof	$U_{rms} = U_{ins}$ 60 ± 5 s; against ambient, between adjacent resistors	No flashover or breakdown

Notes

(1) Figures are given for equal values

(2) For a single element

- The quoted IEC standards marked with an asterisk (*) are also released as EN standards with the same number and identical contents

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