

Preliminary Data Sheet VSC8063

STM-16/STS-48 16:1 Multiplexer
with Integrated Clock Generation

Features

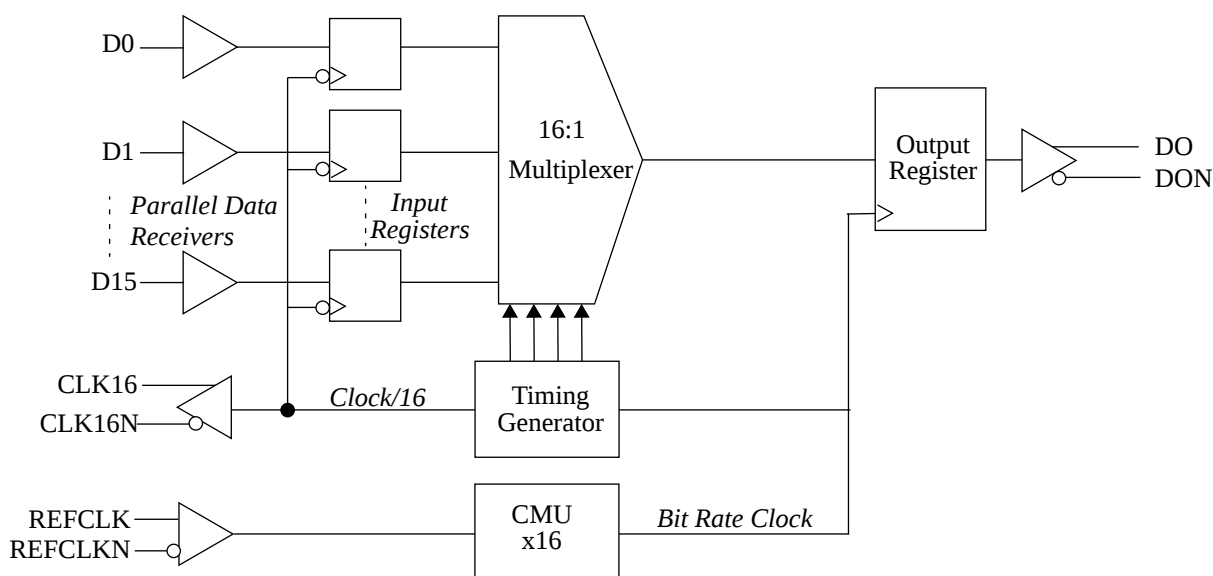
- 16:1 2.488 Gb/s Multiplexer
- Integrated PLL for Clock Generation - No External Components
- 16-bit Wide, Single-ended, ECL 100K Compatible Parallel Data Interface
- 155.52 MHz Reference Clock Frequency
- Differential High Speed Data Output
- Standard ECL Power Supplies: $V_{EE} = -5.2V$
 $V_{TT} = -2.0V$
- Commercial (0° to $85^{\circ}C$) Temperature Range
- Available In 52-pin Plastic Quad Flat Pack

Functional Description

The VSC8063 is a high speed multiplexer designed for STM-16/STS-48 data rates at low power dissipation. For ease of system design, it uses industry standard, -5.2V and -2V, power supplies and has ECL-compatible I/O for parallel data interfaces. The VSC8063 provides an integrated solution for SDH/SONET transmission and instrumentation systems.

The VSC8063 consists of a 16:1 multiplexer circuit and a clock multiplier unit (CMU). The 16:1 multiplexer accepts 16 parallel single-ended ECL compatible inputs (D0..D15) at data rates of 155.52Mb/s then bit-wise serializes the data word onto a 2.488Gb/s serial output (DO/DON). The internal timing of the VSC8063 is referenced to the negative going edge of the 155.52 MHz clock true input (REFCLK). A divided-by-16 clock output is also provided (CLK16/CLK16N). The setup and hold time of the parallel inputs (D0..D15) are specified with respect to the falling edge of CLK16, so that CLK16/CLK16N can be used to clock the data source of D0..D15.

VSC8063 Block Diagram

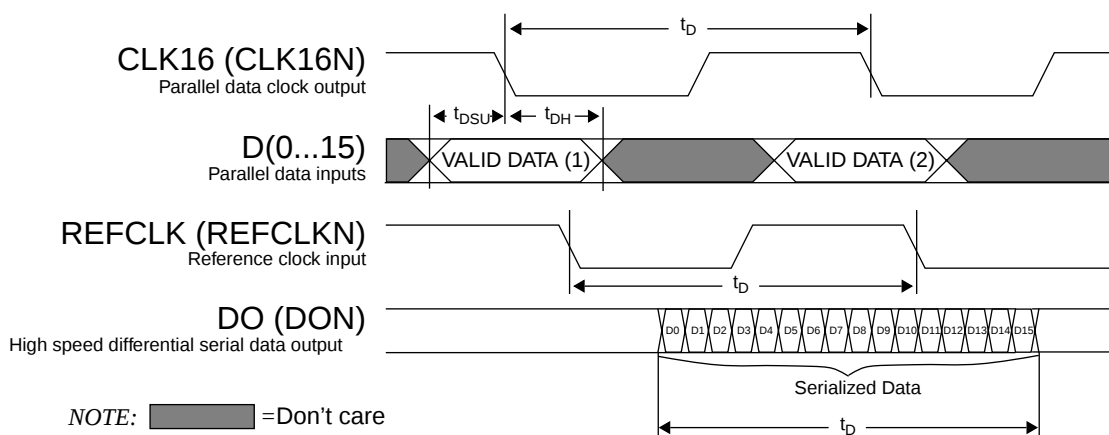


VSC8063 AC Characteristics

Table 1: VSC8063 Multiplexer AC Characteristics (Over recommended operating range)

Parameter	Description	Min	Typ	Max	Units
t_D	CLK16, REFCLK period		6.4	-	ns
t_{DSU}	Parallel data set-up time (wrt CLK16 falling edge)	1.5	-	-	ns
t_{DH}	Data hold time (wrt CLK16 falling edge)	0.5	-	-	ns
t_{DC}	CLK16 duty cycle	45	-	55	%
t_r, t_f	REFCLK (REFCLKN) rise and fall times (10%-90%)	-	-	1.5	ns
t_r, t_f	D(0..15) rise and fall times (10%-90%)	-	-	2.0	ns
t_r, t_f	CLK16 (CLK16N) rise and fall times (10%-90%)	-	0.5	1	ns
t_r, t_f	DO (DON) rise and fall times (20%-80%)	-	150	170	ps

Figure 1: VSC8063 Multiplexer Waveforms



VSC8063 DC Characteristics

(Over recommended operating conditions with internal V_{REF} , $V_{CC} = GND$, Output load = 50 ohms to -2.0V)

Table 2: ECL Inputs and Outputs

Parameter	Description	Min	Typ	Max	Units	Conditions
V_{OH}	Output HIGH voltage	-1100	-	-700	mV	$V_{IN} = V_{IH} \text{ (max)} \text{ or } V_{IL} \text{ (min)}$

Preliminary Data Sheet

VSC8063

STM-16/STS-48 16:1 Multiplexer
with Integrated Clock Generation

Table 2: ECL Inputs and Outputs

Parameter	Description	Min	Typ	Max	Units	Conditions
V_{OL}	Output LOW voltage	V_{TT}	-	-1750	mV	$V_{IN} = V_{IH} \text{ (max) or } V_{IL} \text{ (min)}$
V_{IH}	Input HIGH voltage	-1040	-	-600	mV	Guaranteed HIGH signal for all inputs
V_{IL}	Input LOW voltage	V_{TT}	-	-1600	mV	Guaranteed LOW signal for all inputs
ΔV_{ECL_OUT}	Output voltage swing	0.850	-	-	V	Output load 50 ohm to V_{TT}
ΔV_{ECL_IN}	Input voltage swing	0.600	0.800	1.2	V	AC coupled

Note: Differential ECL output pins must be terminated identically.

Table 3: High Speed Output Specifications

(Over recommended operating conditions, $V_{CC} = GND$)

Parameter	Description	Min	Typ	Max	Units	Conditions
ΔV_{HSOUT}	Data output voltage swing	0.7	0.9	-	V	AC couple per Figure 3
V_{CM}	Data output common mode voltage		-1.0		V	

Table 4: Clock Multiplier Unit Performance

Name	Description	Min	Typ	Max	Units
RC_d	Reference clock duty cycle	45		55	%
OC_d	CLK16 duty cycle	45		55	%
RC_f	Reference clock frequency		155.52		MHz
Δf_{RC}	Reference clock frequency range	-30		+30	ppm
t_{jitter}	High speed output jitter (12 KHz to 20 MHz)			0.01	UI_{RMS}
f_{-3dB}	Jitter transfer -3dB bandwidth		1500		KHz
g_{JT}	Jitter transfer peaking		0.5		dB

Power Dissipation

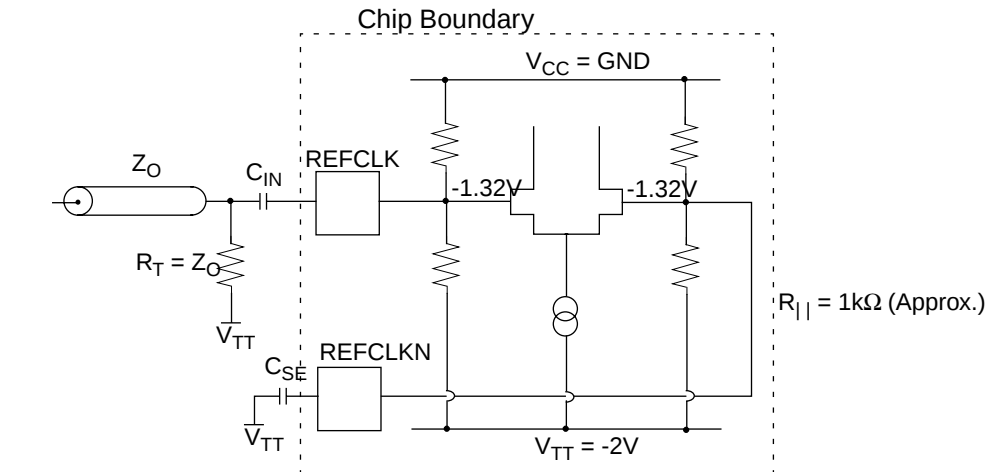
Table 5: Power Dissipation

(Over recommended operating conditions, $V_{CC} = GND$, outputs open circuit)

Parameter	Description	Typ	Max	Units
I_{EE}	Power supply current from V_{EE}	380	450	mA
I_{TT}	Power supply current from V_{TT}	200	250	mA
P_D	Power dissipation	2.4	3.0	W

Interface Recommendations

Figure 2: Single-ended AC-Coupling for REFCLK, REFCLKN Inputs



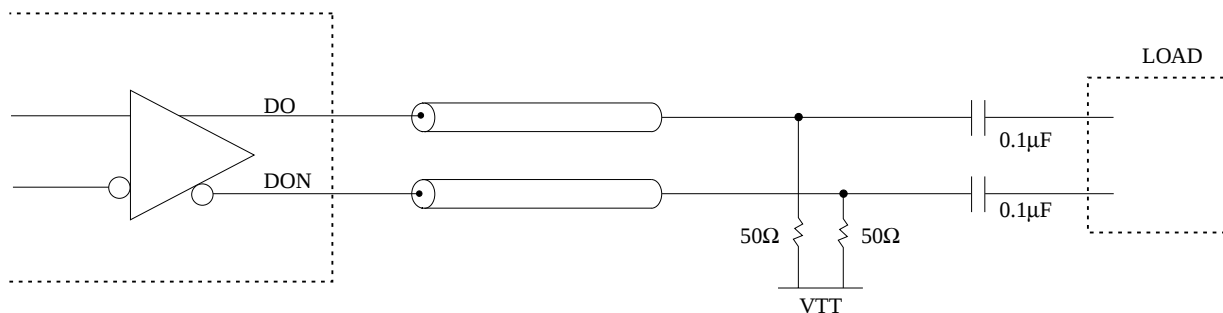
C_{IN} TYP = 0.1 μ F

C_{SE} TYP = 0.1 μ F for single ended applications. (Capacitor values are selected for REFCLK = 155.52 MHz)

REFCLK, REFCLKN Inputs

Internal biasing will position the reference voltage of approximately -1.32V on both the true and complement inputs. This input can either be DC-coupled or AC-coupled; it can also be driven single-ended or differentially. Figure 2 shows the configuration for single-ended, AC-coupling operation. In the case of direct coupling and single-ended input, it is recommended that a stable V_{REF} for ECL levels be used for the complementary input.

Figure 3: High Speed Output Termination



Preliminary Data Sheet

VSC8063

*STM-16/STS-48 16:1 Multiplexer
with Integrated Clock Generation*

Absolute Maximum Ratings⁽¹⁾

Power Supply Voltage (V_{TT})	-3.0V to 0.5V
Power Supply Voltage (V_{EE})	$V_{TT} + 0.7V$ to -7.0V
Input Voltage Applied (V_{ECLIN})	-2.5V to 0.5V
Output Current, I_{OUT} (DC, output HI)	-50 mA
Case Temperature Under Bias (T_C)	-55° to 125°C
Storage Temperature (T_{STG})	-65° to 150°C

Notes: (1) Caution: Stresses listed under “Absolute Maximum Ratings” may be applied to devices one at a time without causing permanent damage. Functionality at or exceeding the values listed is not implied. Exposure to these values for extended periods may affect device reliability.

(2) V_{TT} must be applied before the magnitude of any input signal voltage ($|V_{IN}|$, $|V_{HSIN}|$) can be greater than $|V_{TT} - 0.5V|$

Recommended Operating Conditions

Power Supply Voltage (V_{TT})	-2.0V $\pm 5\%$
Power Supply Voltage (V_{EE})	-5.2V $\pm 5\%$
Operating Temperature Range* (T)	(Commercial) 0° to 85°C

* Lower limit of specification is ambient temperature and upper limit is case temperature.

STM-16/STS-48 16:1 Multiplexer
with Integrated Clock Generation

Preliminary Data Sheet
VSC8063

Figure 4: VSC8063QH (52-Pin PQFP) Pin Diagrams

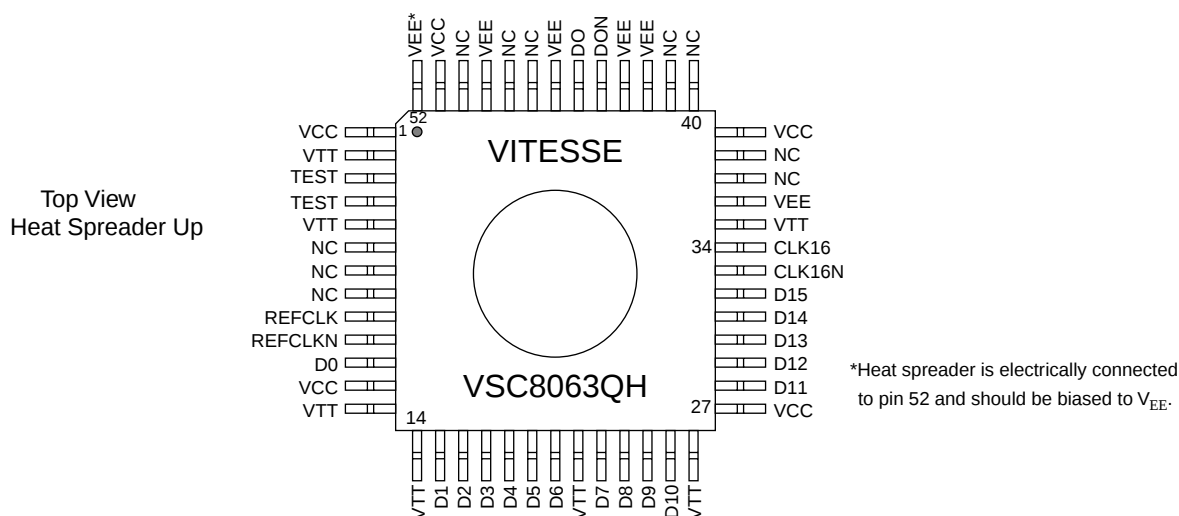


Table 6: VSC8063 Pin Description

Pin # For QH	Name	I/O	Level	Description
9	REFCLK	I	ECL	Reference clock true ¹
10	REFCLKN	I	ECL	Reference clock complement ¹
34	CLK16	O	ECL	Clock divide-by-16 true
33	CLK16N	O	ECL	Clock divide-by-16 complement
11, 15-20, 22-25, 28-32	D[0:15]	I	ECL	Parallel data inputs
45	DO	O	HS	Serial data output true
44	DON	O	HS	Serial data output complement
1,12,27, 39,51	V _{CC}	-	-	Most positive supply
2,5,13,14,21, 26,35	V _{TT}	-	-	DCFL negative supply
36,42,43, 46, 49	V _{EE}	-	-	SCFL negative supply
6,7,8,37,38,40,41, 47,48,50,	NC	-	-	Do not connect, leave open
3, 4	Test	I	-	Test input. Used in factory for testing, connect to VTT through a 1KΩ resistor
52	V _{EE} *	-	-	Heat sink bias, connect to V _{EE}

¹ Can be used single-ended.

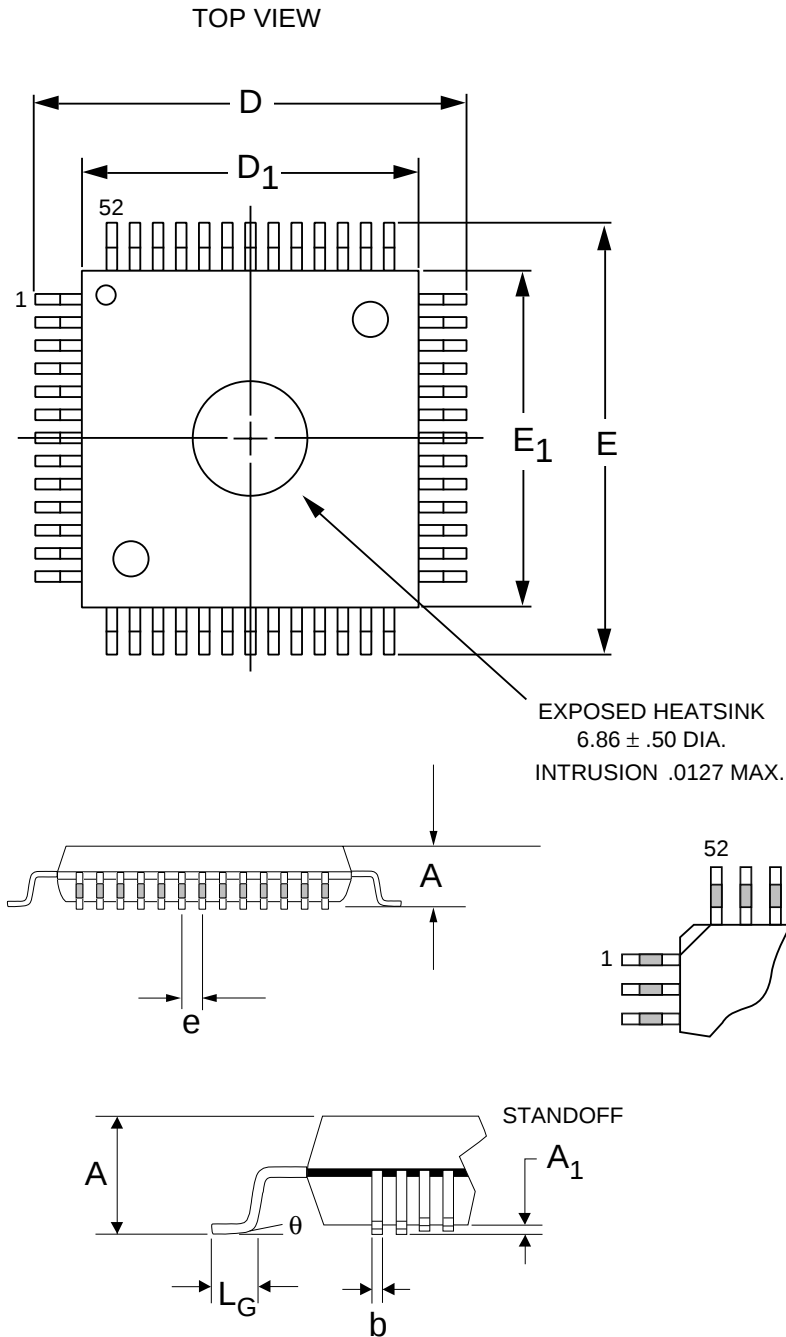
Preliminary Data Sheet

VSC8063

STM-16/STS-48 16:1 Multiplexer
with Integrated Clock Generation

Package Information

52 Pin PQFP (QH) Package Drawings

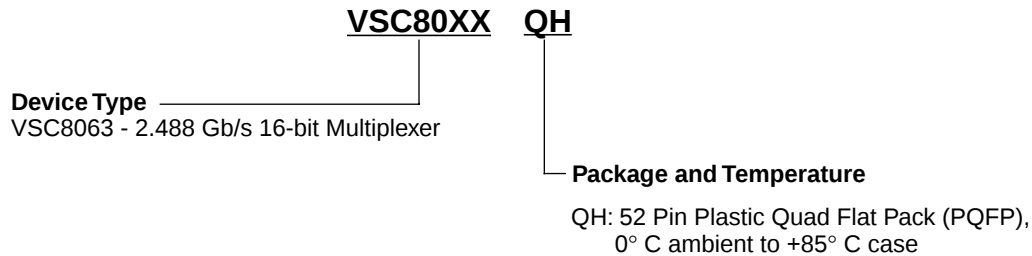


Item	mm	Tol.
A	2.35	MAX
A1	0.25	MAX
D	17.20	±.25
D1	14.00	±.10
E	17.20	±.25
E1	14.00	±.10
e	1.00	BASIC
L _G	0.88	+.15/-.10
b	0.35	±.05
θ	0°-10°	MAX

Notes:
Heat spreader up
All units in mm unless otherwise noted
Heat spreader is connected to V_{EE} .
Drawings not to scale.
Package Drawing #101-255-0 Issue #1

Ordering Information

The order number for this product is formed by a combination of the device number, package type, and the operating temperature range.



Notice

This document contains preliminary information about a new product in the preproduction phase of development. The information in this document is based on initial product characterization. Vitesse reserves the right to alter specifications, features, capabilities, functions, manufacturing release dates, and even general availability of the product at any time. The reader is cautioned to confirm this datasheet is current prior to using it for design.

Warning

Vitesse Semiconductor Corporation's product are not intended for use in life support appliances, devices or systems. Use of a Vitesse product in such applications without the written consent is prohibited.