

TOSHIBA CMOS DIGITAL INTEGRATED CIRCUIT SILICON MONOLITHIC

TMPN3150B1AFG

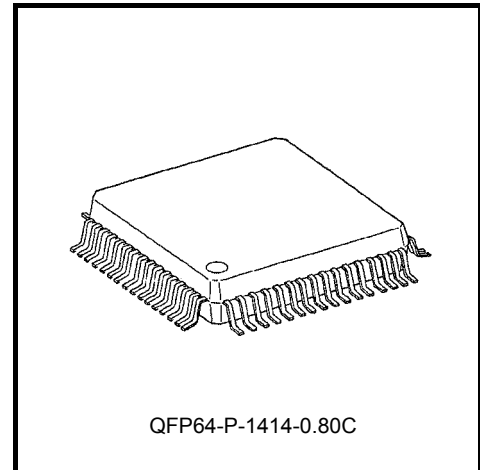
Neuron[®] Chip
For Distributed Intelligent Control Networks (LONWORKS[®])

The TMPN3150B1AFG is a Neuron Chip which configures LONWORKS nodes in combination with external memory. Neuron Chips have all the built-in communications and control functions required to implement LONWORKS nodes. These nodes may then be easily integrated into highly-reliable distributed intelligent control networks.

The typical functions for this chip are explained below.

FEATURES

- I / O Functions
 - Eleven programmable I / O pins.
 - Two programmable 16-bit timers and counters built in.
 - 34 different types of I / O functions to handle a wide range of input and output.
 - ROM firmware image containing pre-programmed I / O drivers, greatly simplifying application programs. (Stored in external ROM)
- Network functions
 - Two CPUs for communication protocol processing built in. The communications and application CPUs execute in parallel.
 - Equipped with a built-in LonTalk protocol which supports all seven levels of the OSI reference model with ISO.
 - Highly reliable communication protocol is supplied as firmware.
 - Built-in twisted-pair wire transceiver
 - Equipped with communications modes and communication speeds which support various types of external transceivers. Supports twisted-pair wire, power line, radio (RF), infrared, coaxial cables and fiber optics.
 - Communication port transceiver modes and logical addresses stored within the EEPROM. Can be amended via the network.



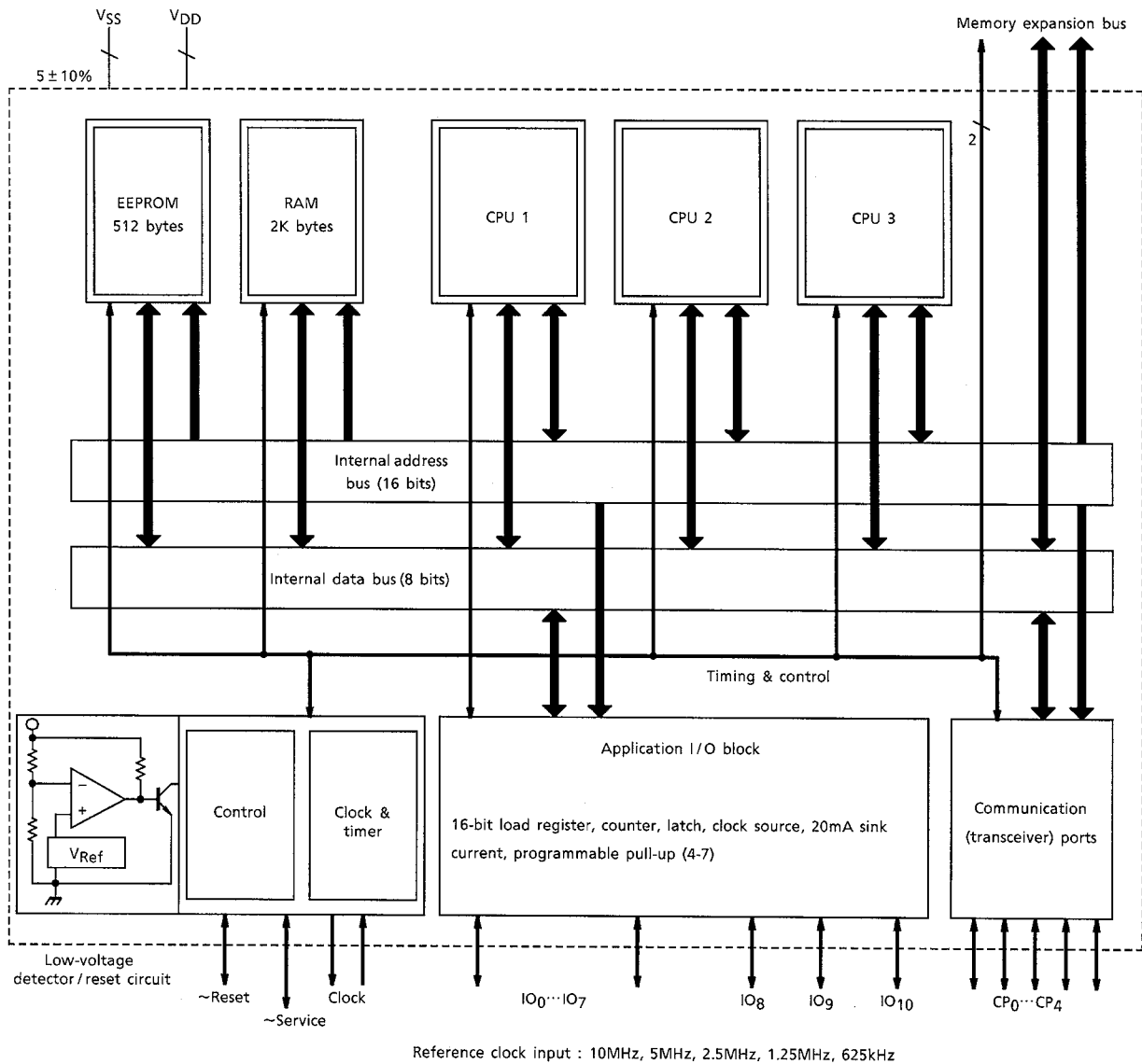
Weight : 1.0g (Typ.)

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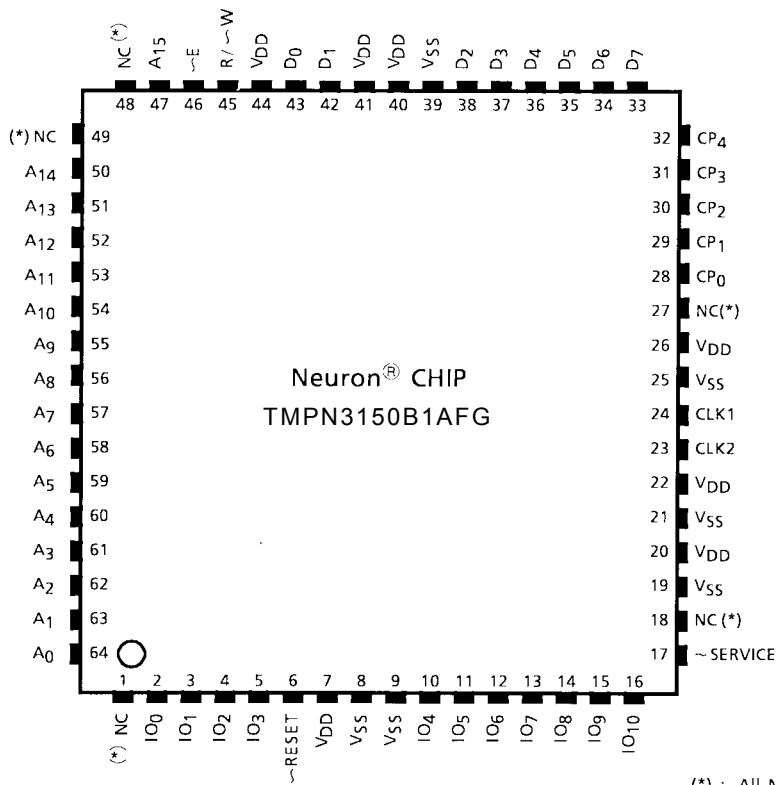
- Other functions
 - Application programs are also stored within the EEPROM.
Can be updated by downloading over the network. EEPROM can be externally added.
 - Built-in watch-dog timer.
 - Each chip has a unique ID number.
Effective during the logical installation of networks.
 - Low electrical consumption mode supported with a sleep mode.
 - Built-in low-voltage detection circuit.
Prevents incorrect operations and writing errors in the EEPROM during drops in power voltage.
 - The package is QFP64-P-1414-0.80C (Lead-Free Type (Pd PrePlated Frame)).

BLOCK DIAGRAM



| ITEM | TMPN3150B1AFG |
|---------------------------|---------------|
| CPU | 8-bit CPU×3 |
| RAM | 2,048 bytes |
| ROM | — |
| EEPROM | 512 bytes |
| 16-bit Timer / Counter | 2 channels |
| External Memory Interface | Available |
| Package | 64-pin SOP |

PIN ASSIGNMENT



(*) : All NC pins should be open.

PIN FUNCTION

| PIN No. | PIN NAME | I / O | PIN FUNCTION |
|---------------------------|---|--|--|
| 24 | CLK1 | Input | Oscillator connection, or external clock input. |
| 23 | CLK2 | Output | Oscillator connection. Leave open when external clock is input to CLK1. |
| 6 | ~RESET | I / O (built-in pull-up) | Reset pin. (Active low) |
| 17 | ~SERVICE | I / O (built-in configurable pull-up) | Service pin. Indicator output during operation. |
| 2~5 | IO ₀ ~IO ₃ | I / O | Large current sink capacity (20mA). General I / O port. |
| 10~13 | IO ₄ ~IO ₇ | I / O (built-in configurable pull-up) | General I / O port. One of IO ₄ to IO ₇ can be specified as No.1 timer / counter input. Output signal can be output to IO ₀ . IO ₄ can be used as the No.2 timer / counter input with IO ₁ as output. |
| 14~16 | IO ₈ ~IO ₁₀ | I / O | General I / O port. Can be used for serial communication with other device. |
| 43, 42, 38~33 | D ₀ , D ₁ , D ₂ ~D ₇ | I / O | Data bus for memory expansion |
| 45 | R / ~W | Output | Output port for controlling read / write for memory expansion |
| 46 | ~E | Output | Output port for controlling memory expansion |
| 47, 50~64 | A ₁₅ , A ₁₄ ~A ₀ | Output | Address output port for memory expansion |
| 7, 20, 22, 26, 40, 41, 44 | V _{DD} | Input | Power input (5.0V Typ.) |
| 8, 9, 19, 21, 25, 39 | V _{SS} | Input | Power input (0V GND) |
| 1, 18, 27, 48, 49 | NC | — | Do not connect anything. Leave pins open. |
| 28~32 | CP ₀ ~CP ₄ | I / O | Bidirectional port for communications. Supports several communications protocols by specifying mode. |

- * :
- The ~SERVICE and IO₄ ~ IO₇ terminals are programmable pull-ups.
 - All V_{DD} terminals must be externally connected.
 - All V_{SS} terminals must be externally connected.

MAXIMUM RATINGS ($V_{SS} = 0V$, V_{SS} typ.)

| CHARACTERISTICS | SYMBOL | RATING | UNIT |
|----------------------|-----------|--------------------|------|
| Power Supply Voltage | V_{DD} | -0.3~7.0 | V |
| Input Voltage | V_{IN} | -0.3~ $V_{DD}+0.3$ | V |
| Power Dissipation | PD | 800 | mW |
| Storage Temperature | T_{stg} | -65~150 | °C |

OPERATING CONDITIONS

| ITEM | SYMBOL | MIN | TYP. | MAX | UNIT |
|------------------------|-------------|--------------|------|----------|------|
| Operating Voltage | V_{DD} | 4.5 | 5.0 | 5.5 | V |
| Input Voltage (TTL) | $V_{IH(1)}$ | 2.0 | — | V_{DD} | V |
| | $V_{IL(1)}$ | V_{SS} | — | 0.8 | V |
| Input Voltage (CMOS) | $V_{IH(2)}$ | $V_{DD}-0.8$ | — | V_{DD} | V |
| | $V_{IL(2)}$ | V_{SS} | — | 0.8 | V |
| Operating Frequency | f_{osc} | 0.625 | — | 10 | MHz |
| Operating Temperature | T_{opr} | -40 | — | 85 | °C |

ELECTRICAL CHARACTERISTICS

DC characteristic ($V_{DD} = 5.0 V \pm 10\%$, $V_{SS} = 0 V$, $T_a = -40\sim 85^\circ C$)

(Above operating conditions apply unless otherwise states.)

| CHARACTERISTICS | SYMBOL | PINS | TEST CONDITION | MIN | MAX | UNIT | |
|-----------------------------|-------------|---|----------------------------|---------------|----------|------|---|
| LOW Output Voltage (1) | $V_{OL(1)}$ | IO ₀ ~IO ₃ | $I_{OL}=20mA$ | 0 | 0.8 | V | |
| | | | $I_{OL}=10mA$ | 0 | 0.4 | V | |
| LOW Output Voltage (2) | $V_{OL(2)}$ | ~SERVICE | Duty cycle=50% | $I_{OL}=20mA$ | 0 | 0.8 | V |
| | | | | $I_{OL}=10mA$ | 0 | 0.4 | V |
| LOW Output Voltage (3) | $V_{OL(3)}$ | CP ₂ , CP ₃ | $I_{OL}=40mA$ | 0 | 1.0 | V | |
| LOW Output Voltage (4) | $V_{OL(4)}$ | Others (Note 1) | $I_{OL}=1.4mA$ | 0 | 0.4 | V | |
| HIGH Output Voltage (1) | $V_{OH(1)}$ | IO ₀ ~IO ₃ | $I_{OH}=-1.4mA$ | $V_{DD}-0.4$ | V_{DD} | V | |
| HIGH Output Voltage (2) | $V_{OH(2)}$ | ~SERVICE | $I_{OH}=-1.4mA$ | $V_{DD}-0.4$ | V_{DD} | V | |
| HIGH Output Voltage (3) | $V_{OH(3)}$ | CP ₂ , CP ₃ | $I_{OH}=-40mA$ | $V_{DD}-1.0$ | V_{DD} | V | |
| HIGH Output Voltage (4) | $V_{OH(4)}$ | Others (Note 1) | $I_{OH}=-1.4mA$ | $V_{DD}-0.4$ | V_{DD} | V | |
| Input Current | I_{IN} | (Note 2) | $V_{IN}=V_{SS}\sim V_{DD}$ | -10 | +10 | μA | |
| Pull-up Current | I_{PU} | IO ₄ ~IO ₇ ~SERVICE, ~RESET (Note 3) | $V_{IN}=0V$ | -30 | -300 | μA | |
| Low-voltage Detection Level | V_{LVD} | V_{DD} | — | 3.8 | 4.5 | V | |

Note1 : Output voltage characteristics exclude the ~RESET pin and CLK2 pin.

Note2 : Excludes pull-up input pins.

Note3 : The IO₄ to IO₇ and ~SERVICE pins have programmable pull-ups. ~RESET has a fixed pull-up.

| ITEM | | SYMBOL | TYP. | MAX | UNIT |
|------------------------------------|-----------------|-----------------------|------|-----|------|
| Operating Mode Current Consumption | 10 MHz Clock | I _{DD} (OP) | 18 | 30 | mA |
| | 5 MHz Clock | | 10 | 15 | |
| | 2.5 MHz Clock | | 5 | 8 | |
| | 1.25 MHz Clock | | 2.5 | 5 | |
| | 0.625 MHz Clock | | 1.5 | 3 | |
| Sleep Mode Current Consumption | | I _{DD} (SLP) | 18 | 100 | μA |

Note: Test conditions for current dissipation

V_{DD}=5V, all output=with no load, all input=0.2V or below or V_{DD}-0.2V, programmable pull-up=off, crystal oscillator clock input, differential receiver disabled.

The current value (typ.) is a typical value when Ta=25°C.

The current value (max) applies to the rated temperature range at V_{DD}=5.5V.

200μA (typ.) to 600μA (max) is added to the current of the differential receiver when the receiver is enabled.

The differential receiver is enabled by either of the following conditions :

- When the Neuron chip is in Run mode and the communication ports are in Differential mode.
- When the Neuron chip is in Sleep mode, the communication ports are in Differential mode, and the Comm Port Wakeup is not masked.

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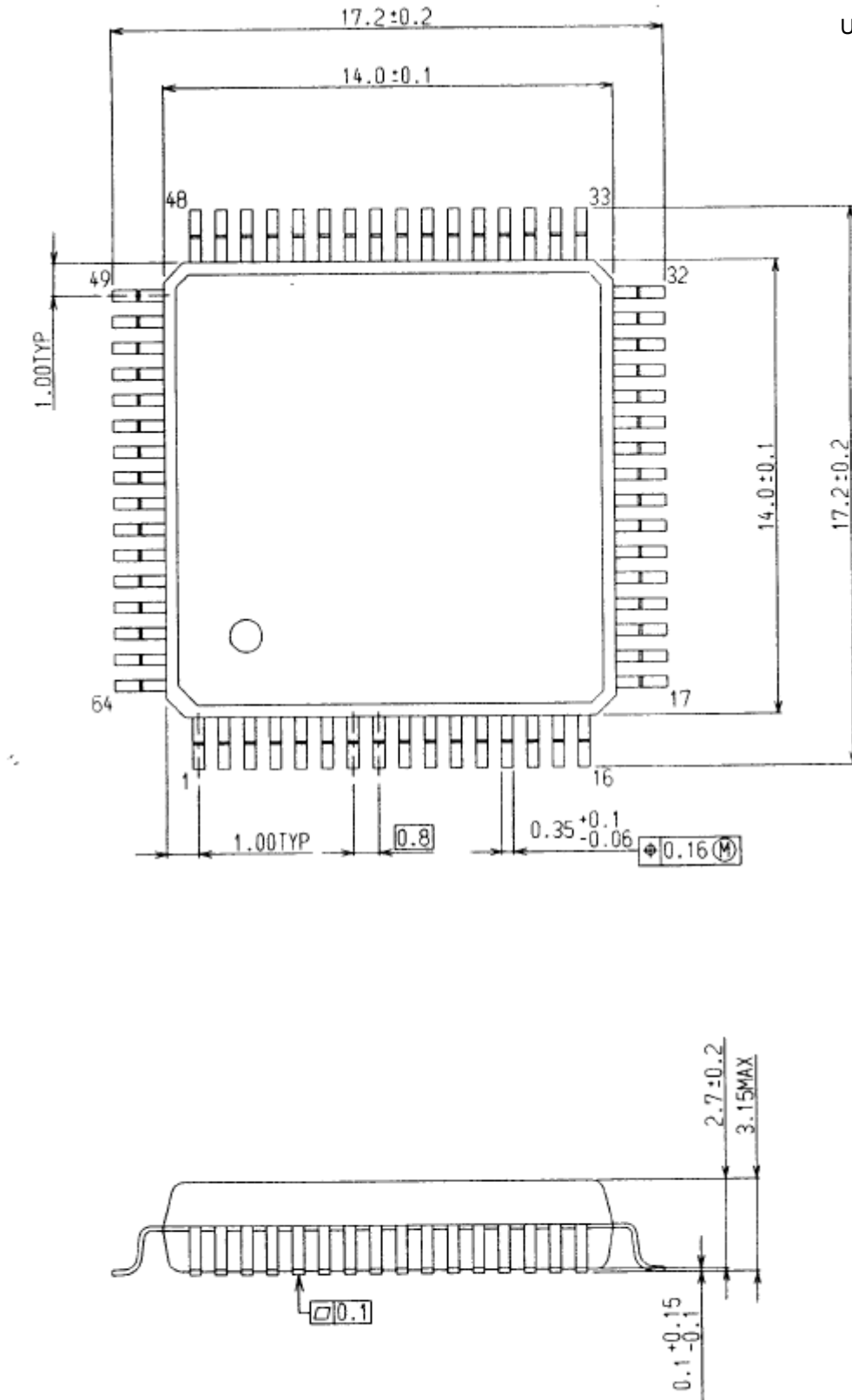
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PACKAGE DIMENSIONS

QFP64-P-1414-0.80C

UNIT: mm



UNIT: mm

