262,144 WORD ×4 BIT DYNAMIC RAM

PRELIMINARY

DESCRIPTION

The TC514256BP/BJ/BZ/BFT is the new generation dynamic RAM organized 262,144 words by 4 bits. The TC514256BP/BJ/BZ/BFT utilizes TOSHIBA's CMOS Silicon gate process technology as well as advanced circuit techniques to provide wide operating margins, both internally and to the system user.

Multiplexed address inputs permit the TC514256BP/BJ/BZ/BFT to be packaged in a standard 20 pin plastic DIP, 26/20 pin plastic SOJ, 20/19 pin plastic ZIP, 24/20 pin plastic TSOP. The package size provides high system bit densities and is compatible with widely available automated testing and insertion equipment. System oriented features include single power supply of 5V±10% tolerance direct interfacing capability with high performance logic families such as Schottky TTL.

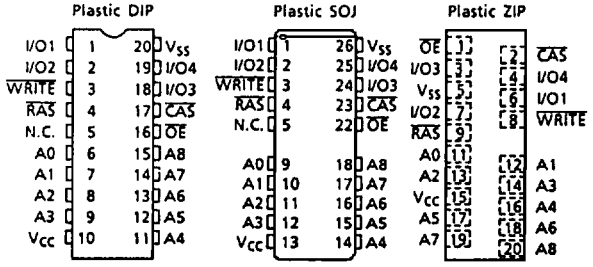
FEATURES

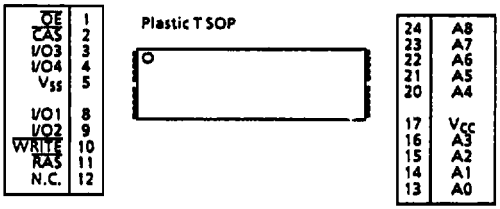
- 262,144 word by 4 bit organization
- Fast access time and cycle time

		TC514256BP/BJ/BZ/BFT-60
t_{RAC}	$\overline{RAS}$ Access Time	60ns
t_{AA}	Column Address Access Time	30ns
t_{CAC}	$\overline{CAS}$ Access Time	20ns
t_{RC}	Cycle Time	110ns
t_{PC}	Fast Page Mode Cycle Time	40ns

- Single power supply of 5V±10% with a built-in V_{BB} generator
- Low Power
  495mW MAX. Operating
  5.5mW MAX. Standby
- Outputs unlatched at cycle end allows two-dimensional chip selection
- Read-Modify-Write, $\overline{CAS}$ before $\overline{RAS}$ refresh, $\overline{RAS}$-only refresh, Hidden refresh, and Fast Page Mode Capability
- All inputs and outputs TTL Compatible
- 512 refresh cycles/8ms
- Package
  TC514256BP : DIP20-P-300B
  TC514256BJ : SOJ26-P-300
  TC514256BZ : ZIP20-P-400
  TC514256BFT : TSOP24-P-0616

PIN CONNECTION

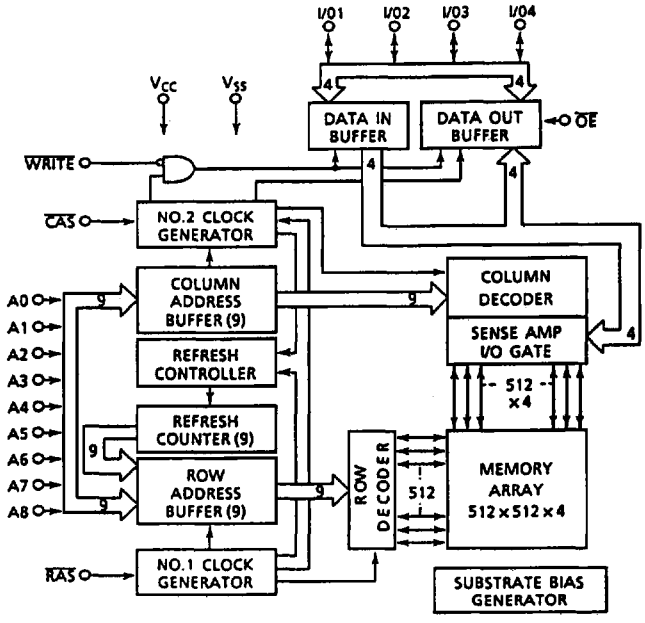




PIN NAMES

A0~A8	Address Inputs
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{WRITE}$	Read/Write Input
$\overline{OE}$	Output Enable
I/O1~I/O4	Data Input/Output
V_{CC}	Power (+5V)
V_{SS}	Ground
N.C.	No Connection

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

ITEM	SYMBOL	RATING	UNITS	NOTES
Input Voltage	V_{IN}	−1~7	V	1
Output Voltage	V_{OUT}	−1~7	V	1
Power Supply Voltage	V_{CC}	−1~7	V	1
Operating Temperature	T_{OPR}	0~70	°C	1
Storage Temperature	T_{STG}	−55~150	°C	1
Soldering Temperature·Time	T_{SOLDER}	260·10	°C·sec	1
Power Dissipation	P_D	600	mW	1
Short Circuit Output Current	I_{OUT}	50	mA	1

RECOMMENDED DC OPERATING CONDITIONS (Ta = 0~70°c)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT	NOTES
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	2
V_{IH}	Input High Voltage	2.4	-	6.5	V	2
V_{IL}	Input Low Voltage	-1.0	-	0.8	V	2

DC ELECTRICAL CHARACTERISTICS (V_{CC} = 5V ± 10%, Ta = 0~70°c)

SYMBOL	PARAMETER		MIN.	MAX.	UNITS	NOTES
I_{CC1}	OPERATING CURRENT Average Power Supply Operating Current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: t_{RC} = t_{RC} MIN.)	TC514256BP/BJ/BZ/BFT-60	–	90	mA	3, 4 5
I_{CC2}	STANDBY CURRENT Power Supply Standby Current ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})		–	2	mA	
I_{CC3}	$\overline{RAS}$ ONLY REFRESH CURRENT Average Power Supply Current, $\overline{RAS}$ Only Mode ($\overline{RAS}$ Cycling, $\overline{CAS}$ = V_{IH}: t_{RC} = t_{RC} MIN.)	TC514256BP/BJ/BZ/BFT-60	–	90	mA	3, 5
I_{CC4}	FAST PAGE MODE CURRENT Average Power Supply Current, Fast Page Mode ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$, Address Cycling: t_{PC} = t_{PC} MIN.)	TC514256BP/BJ/BZ/BFT-60	–	60	mA	3, 4 5
I_{CC5}	STANDBY CURRENT Power Supply Standby Current ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} – 0.2V)		–	1	mA	
I_{CC6}	$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CURRENT Average Power Supply Current, $\overline{CAS}$ Before $\overline{RAS}$ Mode ($\overline{RAS}$, $\overline{CAS}$ Cycling: t_{RC} = t_{RC} MIN.)	TC514256BP/BJ/BZ/BFT-60	–	90	mA	3
$I_{I(L)}$	INPUT LEAKAGE CURRENT Input Leakage Current, any input (0V ≤ V_{IN} ≤ 6.5V, All Other Pins Not Under Test = 0V)		– 10	10	μA	
$I_{O(L)}$	OUTPUT LEAKAGE CURRENT (D_{OUT} is disabled, 0V ≤ V_{OUT} ≤ 5.5V)		– 10	10	μA	
V_{OH}	OUTPUT LEVEL Output "H" Level Voltage (I_{OUT} = – 5mA)		2.4	–	V	
V_{OL}	OUTPUT LEVEL Output "L" Level Voltage (I_{OUT} = 4.2mA)		–	0.4	V	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(V_{CC} = 5V ± 10%, Ta = 0~70°c) (Notes 6, 7, 8)

SYMBOL	PARAMETER	TC514256BP/BJ/BZ/BFT-60		UNIT	NOTES
		MIN.	MAX.		
t_{RC}	Random Read or Write Cycle Time	110	-	ns	
t_{RMW}	Read-Modify-Write Cycle Time	165	-	ns	
t_{PC}	Fast Page Mode Cycle Time	40	-	ns	
t_{PRMW}	Fast Page Mode Read-Modify-Write Cycle Time	95	-	ns	
t_{RAC}	Access Time from $\overline{RAS}$	-	60	ns	9,14
t_{CAC}	Access Time from $\overline{CAS}$	-	20	ns	9,14
t_{AA}	Access Time from Column Address	-	30	ns	9,15
t_{CPA}	Access Time from $\overline{CAS}$ Precharge	-	35	ns	9
t_{CLZ}	$\overline{CAS}$ to output in Low-Z	0	-	ns	9
t_{OFF}	Output Buffer Turn-off Delay	0	20	ns	10
t_T	Transition Time (Rise and Fall)	3	50	ns	8
t_{RP}	$\overline{RAS}$ Precharge Time	40	-	ns	
t_{RAS}	$\overline{RAS}$ Pulse Width	60	10,000	ns	
t_{RASP}	$\overline{RAS}$ Pulse Width (Fast Page Mode)	60	100,000	ns	
t_{RSH}	$\overline{RAS}$ Hold Time	20	-	ns	
t_{RHCP}	$\overline{RAS}$ Hold Time From $\overline{CAS}$ Precharge (Fast Page Mode)	35	-	ns	
t_{CSH}	$\overline{CAS}$ Hold Time	60	-	ns	
t_{CAS}	$\overline{CAS}$ Pulse Width	20	10,000	ns	
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	20	40	ns	14
t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	15	30	ns	15
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	5	-	ns	
t_{CP}	$\overline{CAS}$ Precharge Time	10	-	ns	
t_{ASR}	Row Address Set-Up Time	0	-	ns	
t_{RAH}	Row Address Hold Time	10	-	ns	
t_{ASC}	Column Address Set-Up Time	0	-	ns	
t_{CAH}	Column Address Hold Time	15	-	ns	
t_{AR}	Column Address Hold Time referenced to $\overline{RAS}$	50	-	ns	
t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	30	-	ns	
t_{RCS}	Read Command Set-Up Time	0	-	ns	
t_{RCH}	Read Command Hold Time	0	-	ns	11
t_{RRH}	Read Command Hold Time referenced to $\overline{RAS}$	0	-	ns	11
t_{WCH}	Write Command Hold Time	10	-	ns	

ELECTRICAL CHARACTGERISTICS AND RECOMMENDED AC OPERATING CONDITIONS
(Continued)

SYMBOL	PARAMETER	TC514256BP/BJ/BZ/BFT-60		UNITS	NOTES
		MIN.	MAX.		
t_{WCR}	Write Command Hold Time referenced to $\overline{RAS}$	45	–	ns	
t_{WP}	Write Command Pulse Width	10	–	ns	
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	20	–	ns	
t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	20	–	ns	
t_{DS}	Data Set-Up Time	0	–	ns	12
t_{DH}	Data Hold Time	15	–	ns	12
t_{DHR}	Data Hold Time referenced to $\overline{RAS}$	50	–	ns	
t_{REF}	Refresh Period	–	8	ms	
t_{WCS}	Write Command Set-UP Time	0	–	ns	13
t_{CWD}	$\overline{CAS}$ to $\overline{WRITE}$ Delay Time	50	–	ns	13
t_{RWD}	$\overline{RAS}$ to $\overline{WRITE}$ Delay Time	90	–	ns	13
t_{AWD}	Column Address to $\overline{WRITE}$ Delay Time	60	–	ns	13
t_{CPWD}	$\overline{CAS}$ Precharge to $\overline{WRITE}$ Delay Time	65	–	ns	13
t_{CSR}	$\overline{CAS}$ Set-Up Time ($\overline{CAS}$ before $\overline{RAS}$ Cycle)	5	–	ns	
t_{CHR}	$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Cycle)	15	–	ns	
t_{RPC}	$\overline{RAS}$ to $\overline{CAS}$ Precharge Time	0	–	ns	
t_{CPT}	$\overline{CAS}$ Precharge Time ($\overline{CAS}$ before $\overline{RAS}$ Counter Test Cycle)	30	–	ns	
t_{ROH}	$\overline{RAS}$ Hold Time referenced to $\overline{OE}$	10	–	ns	
t_{OEA}	$\overline{OE}$ Access Time	–	20	ns	
t_{OED}	$\overline{OE}$ to Data Delay	20	–	ns	
t_{OEZ}	Output buffer turn off Delay Time from $\overline{OE}$	0	20	ns	
t_{OEH}	$\overline{OE}$ Command Hold Time	20	–	ns	

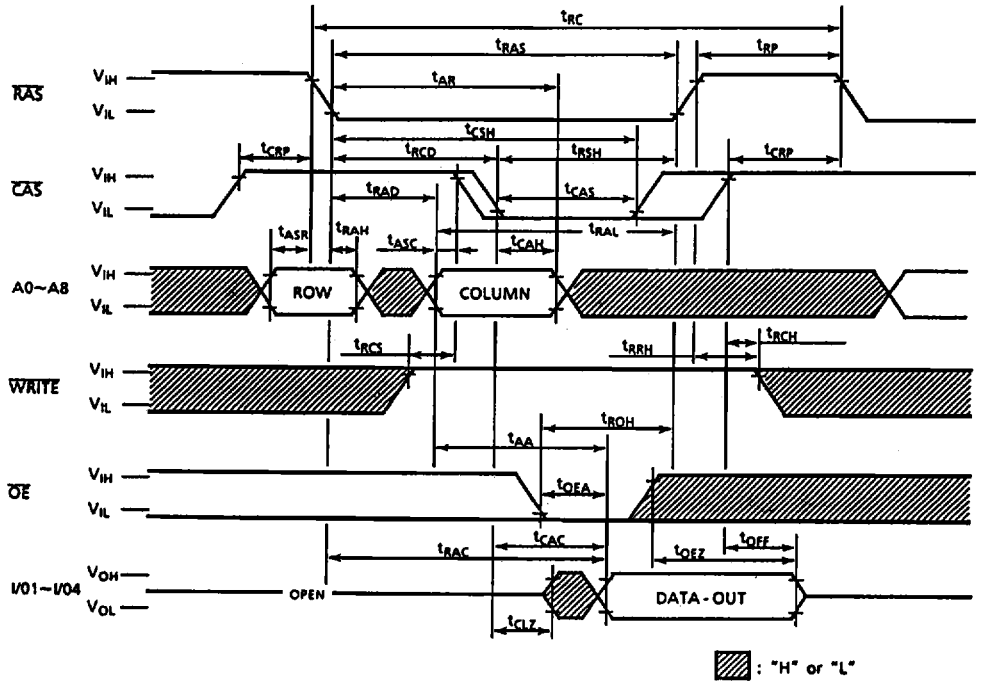
CAPACITANCE (V_{CC} = 5V ± 10%, f = 1MHz, Ta = 0~70°c)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
C_{I1}	Input Capacitance (A0~A8)	–	5	pF
C_{I2}	Input Capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WRITE}$, $\overline{OE}$)	–	7	pF
C_O	Input/Output Capacitance (I/01~I/04)	–	7	pF

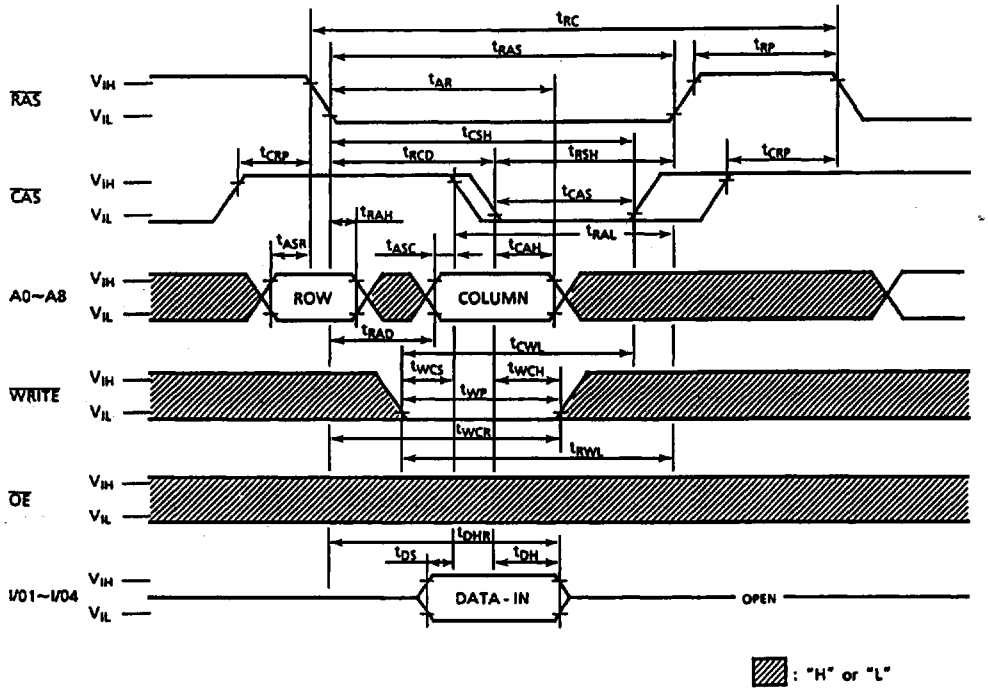
NOTES:

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.
2. All voltages are referenced to V_{SS}.
3. I_{CC1}, I_{CC3}, I_{CC4}, I_{CC6} depend on cycle rate.
4. I_{CC1}, I_{CC4} depend on output loading. Specified values are obtained with the output open.
5. Column address can be changed once or less while $\overline{RAS}=V_{IL}$ and $\overline{CAS}=V_{IH}$.
6. An initial pause of 200μs is required after power-up followed by 8 $\overline{RAS}$ cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$ before $\overline{RAS}$ initialization cycles instead of 8 $\overline{RAS}$ cycles are required.
7. AC measurements assume $t_T=5ns$.
8. V_{IH} (min.) and V_{IL} (max.) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
9. Measured with a load equivalent to 2 TTL loads and 100pF.
10. t_{OFF} (max.) and t_{OEZ} (max.) define the time at which the output achieves the open circuit condition and are not referenced to output voltage levels.
11. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
12. These parameters are referenced to $\overline{CAS}$ leading edge in early write cycles and to $\overline{WRITE}$ leading edge in Read-Modify-Write cycles.
13. t_{WCS}, t_{RWD}, t_{CWD}, t_{AWD} and t_{CPWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$ (min.), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) through the entire cycle; If $t_{RWD} \geq t_{RWD}$ (min.), $t_{CWD} \geq t_{CWD}$ (min.), $t_{AWD} \geq t_{AWD}$ (min.) and $t_{CPWD} \geq t_{CPWD}$ (min.) (Fast Page Mode), the cycle is a Read-Modify-Write cycle and the data out will contain data read from the selected cell: If neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
14. Operation within the t_{RCD} (max.) limit insures that t_{RAC} (max.) can be met. t_{RCD} (max.) is specified as a reference point only: If t_{RCD} is greater than the specified t_{RCD} (max.) limit, then access time is controlled by t_{CAC}.
15. Operation within the t_{RAD} (max.) limit insures that t_{RAC} (max.) can be met. t_{RAD} (max.) is specified as a reference point only: If t_{RAD} is greater than the specified t_{RAD} (max.) limit, then access time is controlled by t_{AA}.

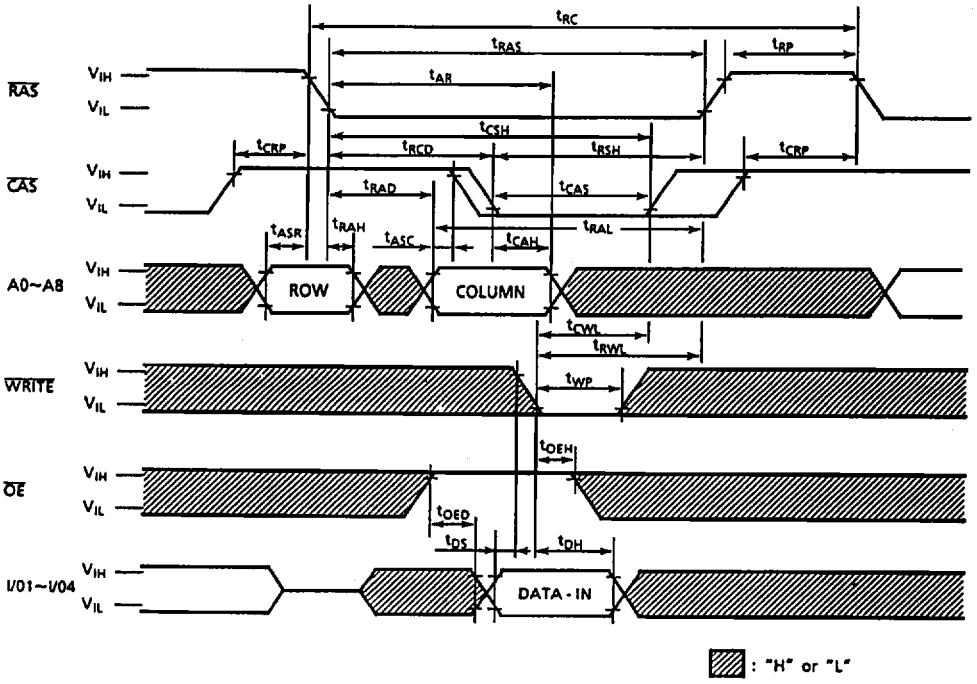
READ CYCLE


tRC
tRAS
tRP
tAR
tCSH
tCRP
tRCD
tRSH
tCRP
tRAD
tCAS
tRAL
tASR
tRAH
tASC
tCAH
ROW
COLUMN
tRCS
tRRH
tRCH
tROH
tAA
tOEA
tCAC
tRAC
tOEZ
tOFF
tCLZ
OPEN
DATA-OUT
RAS
CAS
A0~A8
WRITE
OE
I/O1~I/O4
VIH
VIL
VOH
VOL
: "H" or "L"

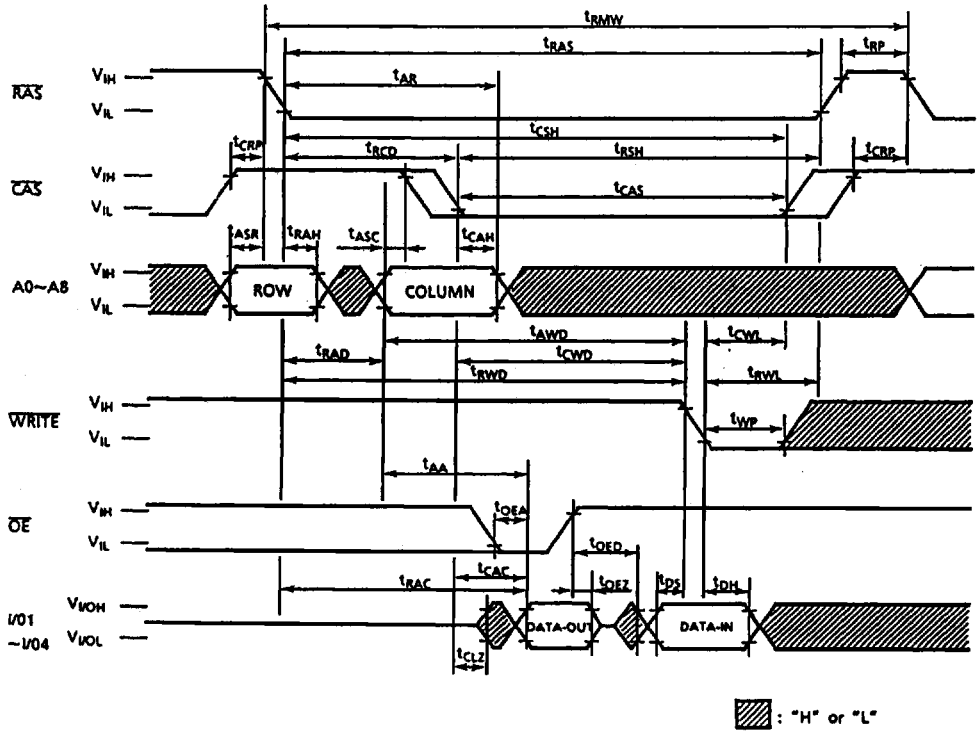
WRITE CYCLE (EARLY WRITE)



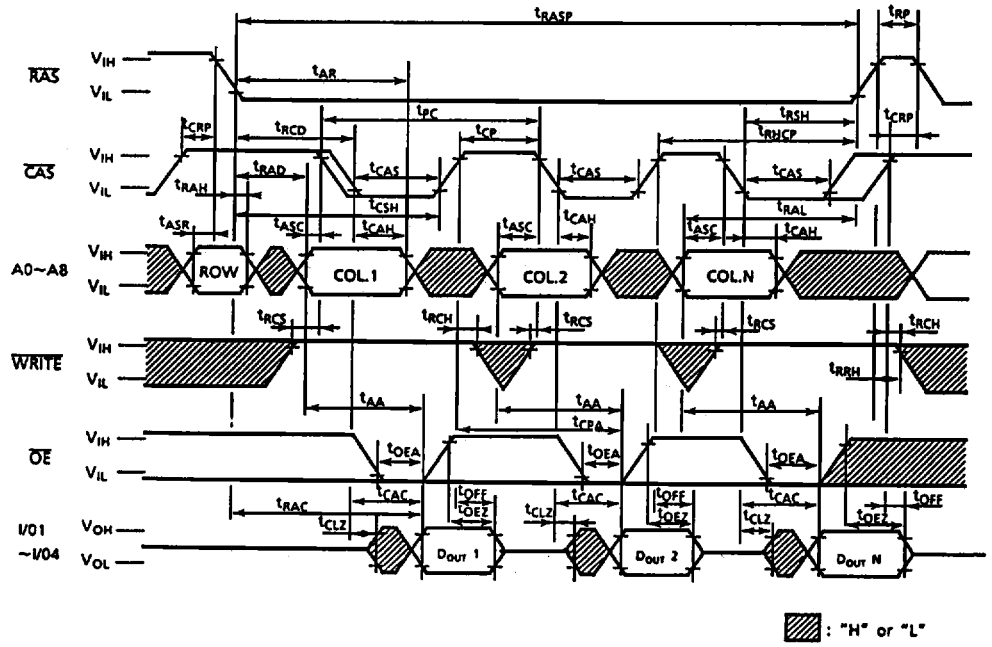
WRITE CYCLE ($\overline{OE}$ CONTROLLED WRITE)



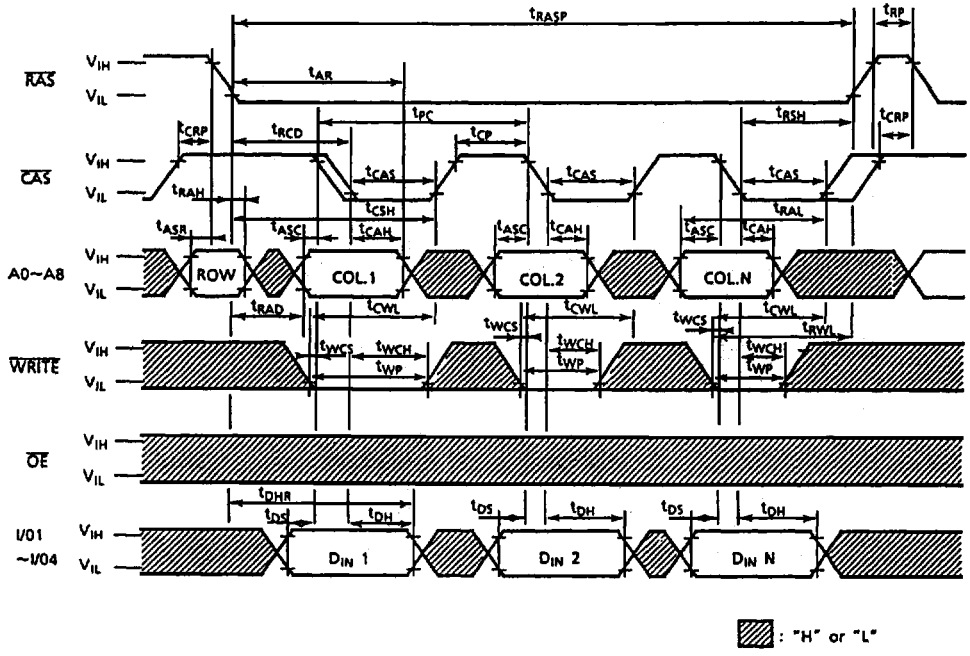
READ-MODIFY-WRITE CYCLE



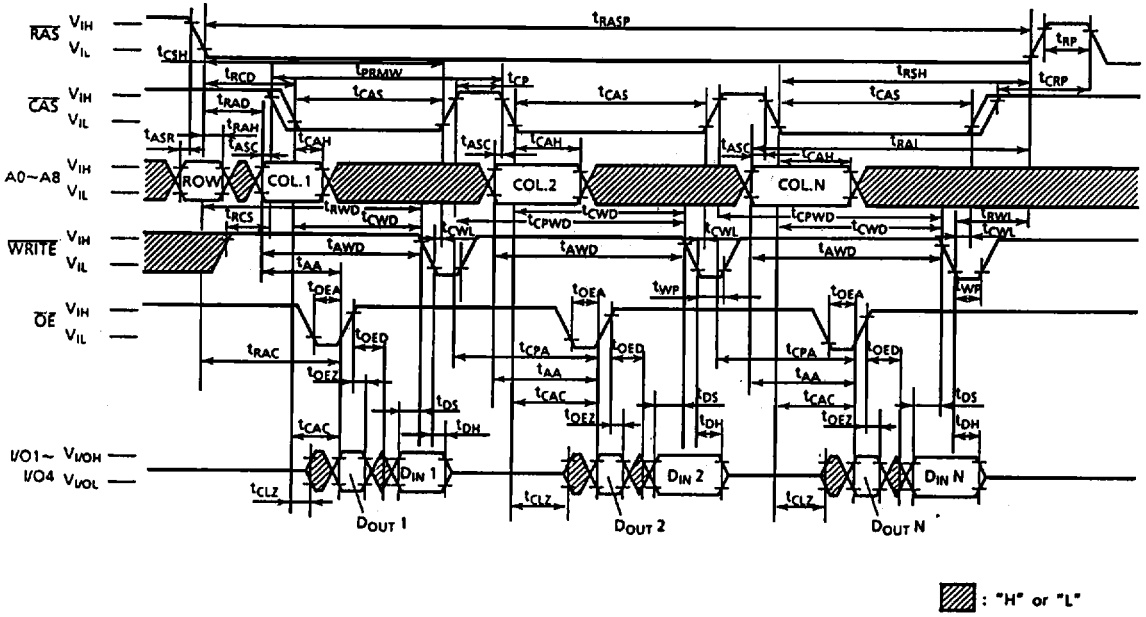
FAST PAGE MODE READ CYCLE



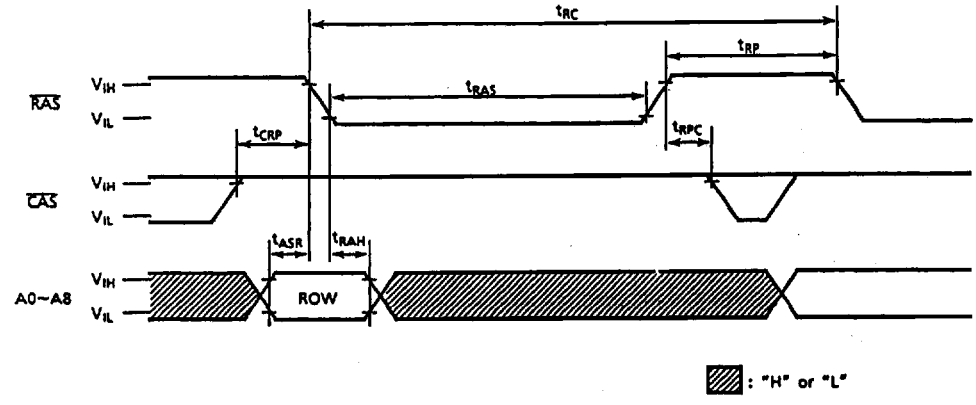
FAST PAGE MODE WRITE CYCLE



FAST PAGE MODE READ-MODIFY-WRITE CYCLE

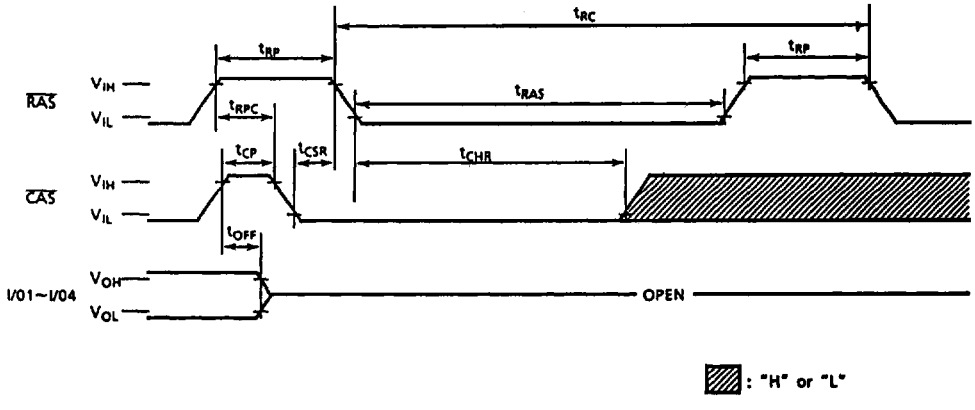


$\overline{RAS}$ ONLY REFRESH CYCLE



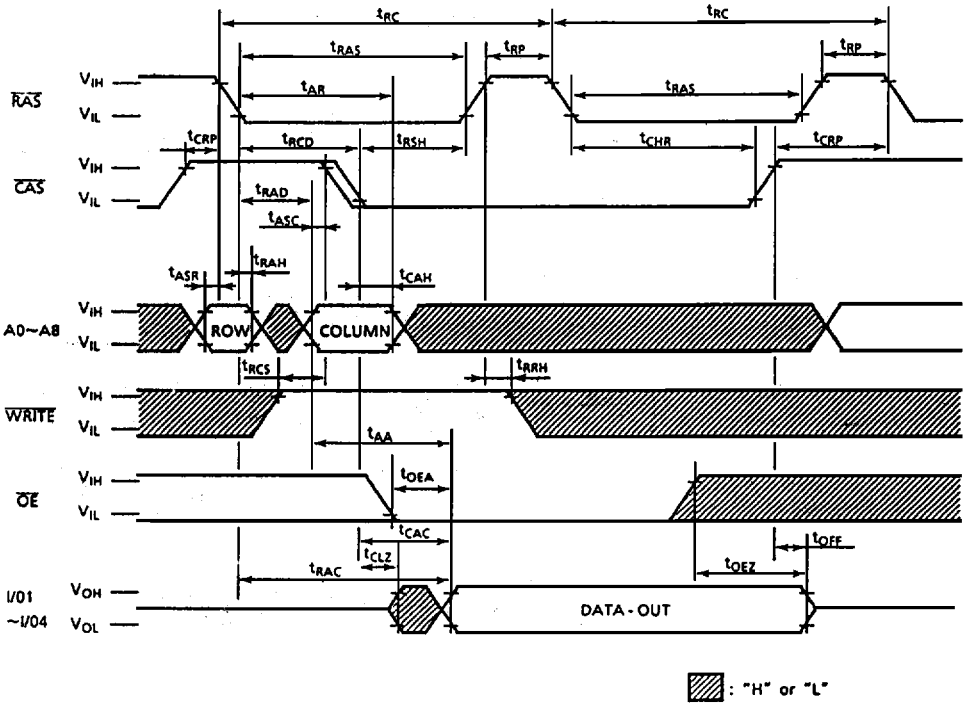
Note: WRITE, $\overline{OE}$="H" or "L"

$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CYCLE

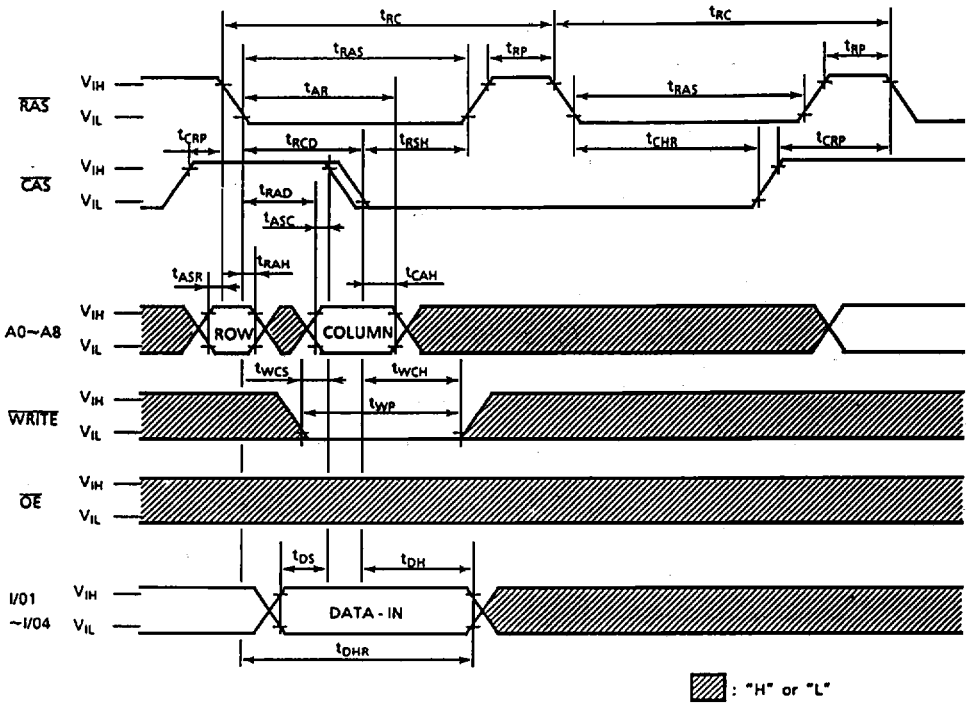


Note: WRITE, $\overline{OE}$=A0~A8="H" or "L"

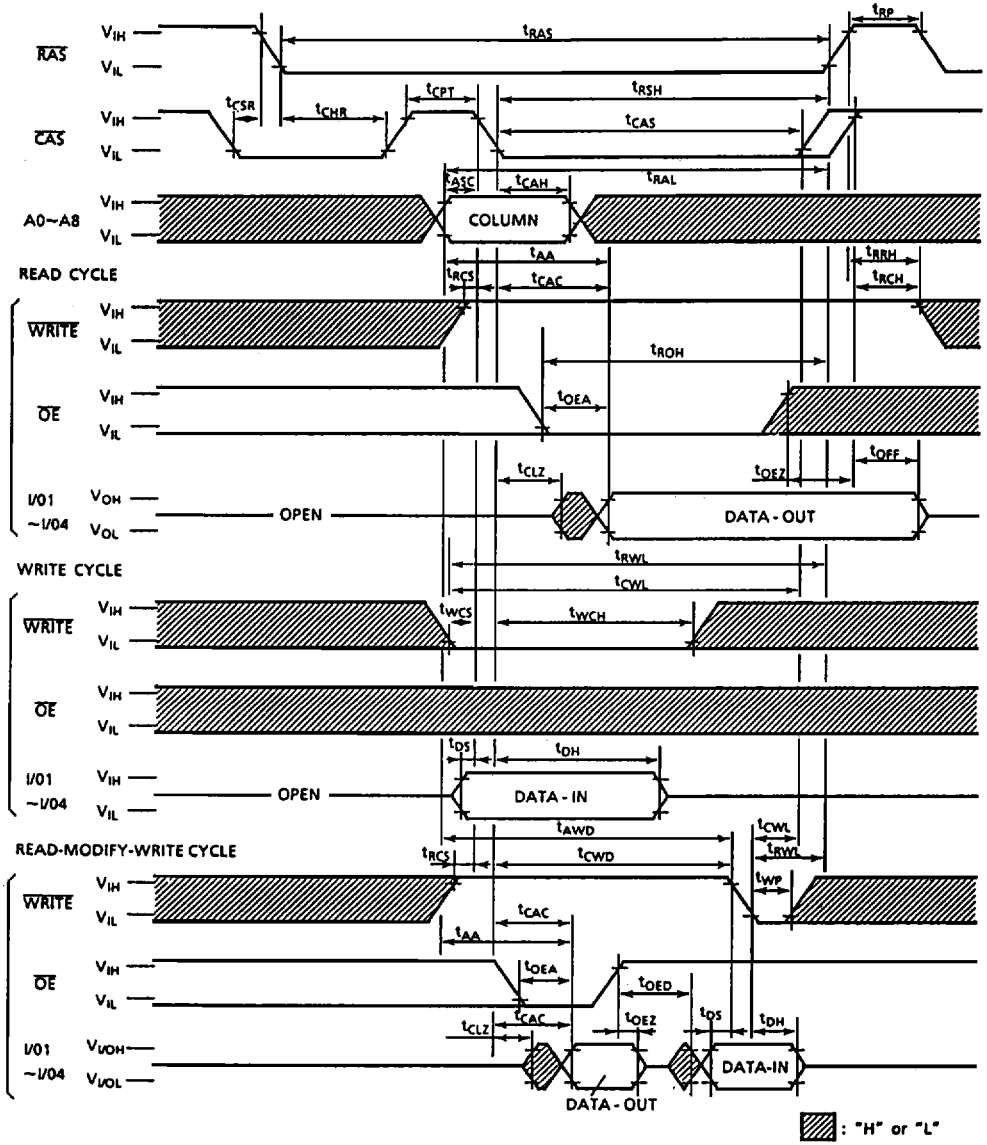
HIDDEN REFRESH CYCLE (READ)



HIDDEN REFRESH CYCLE (WRITE)



$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH COUNTER TEST CYCLE



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