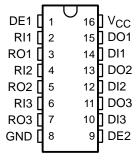
- Meets or Exceeds the Requirements of IBM™ 360/370 Input/Output Interface Specification for 4.5-Mb/s Operation
- Single 5-V Supply
- **Uncommitted Emitter-Follower Output** Structure for Party-Line Operation
- **Driver Output Short-Circuit Protection**
- **Driver Input/Receiver Output Compatible** With TTL
- Receiver Input Resistance . . . 7.4 k Ω to 20 k Ω
- **Ratio Specification for Propagation Delay** Time, Low to High/High to Low

description/ordering information

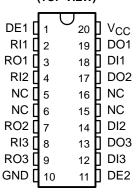
The SN751730 triple line driver/receiver is specifically designed to meet the input/output interface specifications for IBM System 360/370. It also is compatible with standard TTL logic and supply voltage levels.

The low-impedance emitter-follower driver outputs of the SN751730 drive terminated lines, such as coaxial cable or twisted pair. Having the outputs uncommitted allows wired-OR logic to be performed in party-line applications. Output short-circuit protection is provided by an internal clamping network that turns on when the output voltage drops below approximately 2.5 V.

D OR N PACKAGE (TOP VIEW)



NS PACKAGE (TOP VIEW)



An open line affects the receiver input as does a low-level input voltage.

All the driver inputs and receiver outputs are in conventional TTL configuration and the gating can be used during power-up and power-down sequences to ensure that no noise is introduced to the line by pulling either DE1 or DE2 to a low level.

ORDERING INFORMATION

TA	PACKAGE [†]		PACKAGE [†] ORDERABLE PART NUMBER	
	PDIP (N)	Tube	SN751730N	SN751730N
0°C to 70°C	SOIC (D)	Tube	SN751730D	SN751730
0.0 10 70.0	301C (D)	Tape and reel	SN751730DR	311/31/30
	SOP (NS)	Tape and reel	SN751730NSR	SN751730

[†]Package drawings, standard packing quantities, thermal data, symbolization, and PCB design quidelines are available at www.ti.com/sc/package.



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ISTRUMENTS

Function Tables

EACH DRIVER

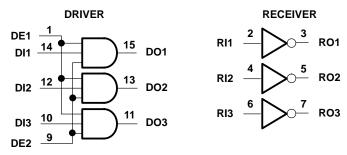
	OUTPUT		
DI	DE1	DE2	DO
L	Х	Х	L
Х	L	Χ	L
Х	X	L	L
Н	Н	Н	Н

EACH DRIVER

INPUT RI	OUTPUT RO
L	Н
Н	L
Open	Н

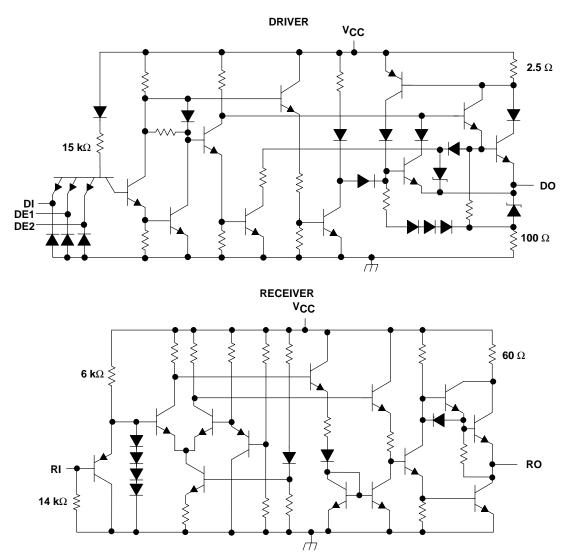
H = high level, L = low level, X = irrelevant

logic diagram (positive logic)





equivalent schematics of driver and receiver†



† All resistor values are nominal.

SLLS062D - MAY 1990 - REVISED AUGUST 2002

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V _{CC} (see Note 1)	7 V
Input voltage range, V _I : Driver	
Receiver	$-0.5\ V$ to 7 V
Output voltage range, VO: Driver	$-0.5\ V$ to 7 V
Enable input voltage range	$-0.5\ V$ to 7 V
Package thermal impedance, θ _{JA} (see Note 2): D package	73°C/W
N package	67°C/W
NS package	60°C/W
Operating virtual junction temperature, T _{.j.}	150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C
Storage temperature range, T _{stg}	\dots -65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values are with respect to network ground terminal.

recommended operating conditions

			MIN	NOM	MAX	UNIT
Vcc	Supply voltage		4.75	5	5.25	V
V	Lligh lovel input voltage	Driver, Enable	2			V
VIH	High-level input voltage Rece	Receiver	1.55			l v
\/	Lour level input veltage	Driver, Enable			0.8	V
VIL	Low-level input voltage	Receiver			1.15	V
TA	Operating free-air temperature		0		70	°C



^{2.} The package thermal impedance is calculated in accordance with JESD 51-7.

DRIVER SECTION

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER			TEST C	TEST CONDITIONS			UNIT	
٧ıK	Input clamp voltage		V _{CC} = 4.75 V,	I _{IL} = -18 mA		-1.5	V	
			$V_{CC} = 4.75 \text{ V},$ $I_{OH} = -59.3 \text{ mA}$	V _{IH} = 2 V, T _A = 25°C	3.11			
\/-··	High lovel output voltage		$V_{CC} = 5.25 \text{ V},$ $I_{OH} = -78.1 \text{ mA}$	V _{IH} = 2 V,		4.10		
VOH	High-level output voltage		$V_{CC} = 4.75 \text{ V},$ $R_L = 51.4 \Omega$	V _{IH} = 2 V,	3.05		V	
			$V_{CC} = 5.25 \text{ V},$ $R_L = 56.9 \Omega$	V _{IH} = 2 V,		4.20		
VODH	Differential high-level output voltage	ntial high-level output voltage		$R_L = 46.3 \Omega \text{ or } 56.9 \Omega$		0.50	V	
.,			$V_{CC} = 5.25 \text{ V},$ $V_{II} = 0.8 \text{ V},$	$I_{OL} = -0.24 \text{ mA}$	I _{OL} = -0.24 mA		.,	
VOL	Low-level output voltage	oltage		R _L = 56.9 Ω		0.15	V	
l	High-level input current	DI	V _{CC} = 5.25 V,	V _{IH} = 2.7 V		20	μА	
ΙН	nigri-ieverinput current		VCC = 5.25 V,	VIH = 2.7 V		60	μΑ	
Iμ	Low-level input current DI DE		V _{CC} = 5.25 V,	V _{IH} = 0.4 V		-400	μΑ	
ЧL			VCC = 3.23 V,	VIH = 0.4 V		-1200	μΑ	
ЮН	High-level output current	High level output ourrent		$V_{IL} = 0$		100	μΑ	
iОН	rigit-level output current		V _{OH} = 5 V	V _{IH} = 4.5 V		100	μΛ	
los	Short-circuit output current [†]		V _{CC} = 5.25 V	V _{IH} = 4.5 V		-30	mA	
Іссн	Supply current (total package)			$V_{I(D)} = 4.5 \text{ V},$ $V_{I(R)} = 0$		47	mA	
ICCL	- Supply current (total package)		No load	$V_{I(D)} = 0,$ $V_{I(R)} = 4.5 \text{ V}$		80	IIIA	

[†] Not more than one output should be shorted at a time, and duration of the short circuit should not exceed one second.

switching characteristics, V_{CC} = 5 V $\pm 5\%$, T_A = 25°C

	PARAMETER	TEST CON	MIN	TYP	MAX	UNIT	
^t PLH	Propagation delay time, low- to high-level output			6.5	12	18.5	ns
tPHL	Propagation delay time, high- to low-level output	$R_L = 47.5 \Omega$, Se	e Figure 1	6.5	12	18.5	ns
Δt_{pd}	Differential propagation delay time‡					10	ns
t _r	Output rise time) = 0.15 V to 3.05 V,	5	10		ns
tf	Output fall time	$R_L = 47.5 \Omega$, C_L See Figure 1	_ = 10.2 pF,	5	13		ns
SR	Slew rate	V_O = 1 V to 3 V average R_L = 47.5 Ω , C_L See Figure 1				0.65	V/ns

 $[\]pm \Delta t_{pd} = |t_{PLH} - t_{PHL}|$



RECEIVER SECTION

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

	PARAMETER	TEST CONDITIONS		MIN	MAX	UNIT
VOH	High-level output voltage	$V_{CC} = 4.75 \text{ V},$ $I_{OH} = -400 \mu\text{A}$	V _I = 1.15 V,	2.7		٧
V	Low level output voltage	$V_{CC} = 4.75 \text{ V},$	I _{OL} = 8 mA		0.5	V
VOL	Low-level output voltage	V _{IH} = 1.55 V	I _{OL} = 4 mA		0.4	V
rj	Input resistance	$V_{CC} = 0$,	V _I = 0.15 V to 3.9 V	7.4	20	kΩ
I _{IH}	High-level input current	$V_{CC} = 4.75 \text{ V},$	V _{IH} = 3.11 V		0.42	mA
I _{IL}	Low-level input current	$V_{CC} = 5.25 \text{ V},$	V _{IL} = 0.15 V	-0.24	0.04	mA
los†	Short-circuit output current	$V_{CC} = 5.25 \text{ V},$	V _{IL} = 0	-20	-100	mA
Іссн	Supply current (total package)	V _{CC} = 5.25 V,	$V_{I(D)} = 4.5 \text{ V},$ $V_{I(R)} = 0$	47		mA
ICCL		No load	$V_{I(D)} = 0,$ $V_{I(R)} = 4.5 \text{ V}$		80	IIIA

[†] Not more than one output should be shorted at a time, and duration of the short circuit should not exceed one second.

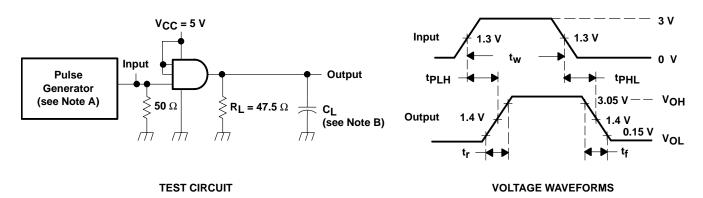
switching characteristics, V_{CC} = 5 V $\pm 5\%$, T_A = 25°C

	PARAMETER	TE	ST CONDITIO	NS	MIN	TYP	MAX	UNIT
t _{PLH}	Propagation delay time, low- to high-level output				7.5	12	19.5	ns
t _{PHL}	Propagation delay time, high- to low-level output	$R_L = 2 k\Omega$,	$C_L = 15 pF$,	See Figure 2	7.5	12	19.5	ns
∆t _{pd} ‡	Differential propagation delay time						10	ns

 $[\]pm \Delta t_{pd} = |t_{PLH} - t_{PHL}|$



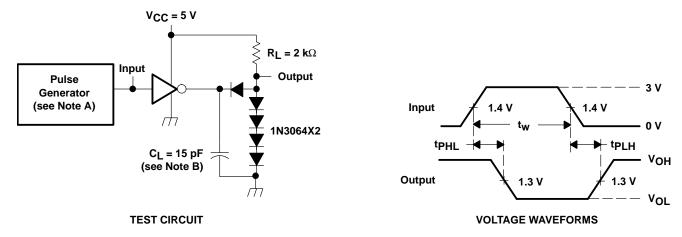
PARAMETER MEASUREMENT INFORMATION



NOTES: A. The pulse generator has the following characteristics: $Z_O \approx 50~\Omega$, $t_W \le 500$ ns, PRR ≤ 1 MHz, $t_f \le 6$ ns, $t_r \le 15$ ns.

B. C_L includes probe and jig capacitance.

Figure 1. Driver Test Circuit and Voltage Waveforms



- NOTES: A. The pulse generator has the following characteristics: $Z_O \approx 50~\Omega$, $t_W \le 500$ ns, PRR ≤ 1 MHz, $t_f \le 10$ ns.
 - B. C_L includes probe and jig capacitance.

Figure 2. Receiver Test Circuit and Voltage Waveforms





.com 12-Jan-2006

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	e Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
SN751730D	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1YEAR
SN751730DE4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1YEAR
SN751730DR	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1YEAR
SN751730DRE4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1YEAR
SN751730N	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN751730NE4	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN751730NSR	ACTIVE	SO	NS	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN751730NSRE4	ACTIVE	SO	NS	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



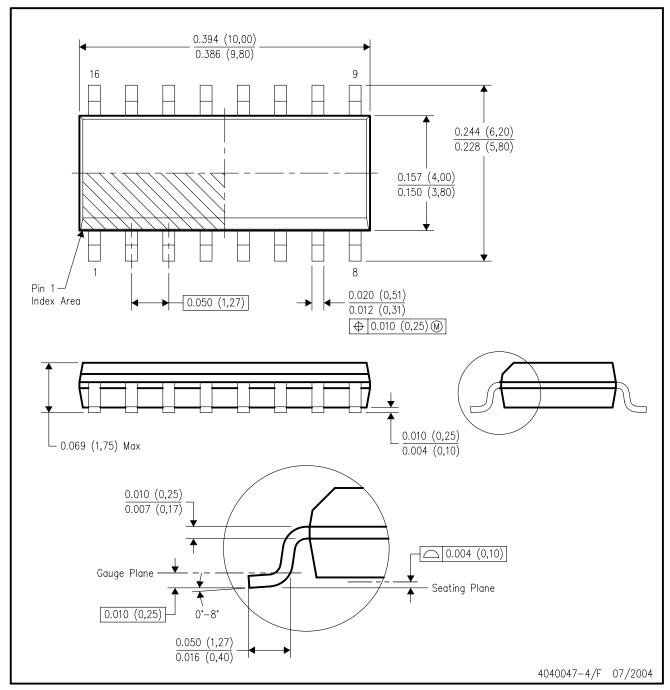
NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
- The 20 pin end lead shoulder width is a vendor option, either half or full width.



D (R-PDSO-G16)

PLASTIC SMALL-OUTLINE PACKAGE



NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
- D. Falls within JEDEC MS-012 variation AC.



MECHANICAL DATA

NS (R-PDSO-G**)

14-PINS SHOWN

PLASTIC SMALL-OUTLINE PACKAGE



NOTES:

- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.



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