SiRFstar IIe/LP Chip Set
A Low Power GPS Chip Set for Consumer Products

ARCHITECTURE HIGHLIGHTS

Industry Leading GPS Performance
- Builds on high performance SiRFstar IIe/LP architecture
- Supports user task integration
- Signal acquisition using 1,920 time/frequency search channels
- SBAS (WAAS and EGNOS), and DGPS support
- Multipath-mitigation hardware
- Cold Start under 45 seconds

Low Power
- Under 175 mW at full power
- TricklePower™ mode reduces power to under 60 mW
- Adaptive TricklePower intelligently switches between full and TricklePower.
- Push to fix reduces power by as much as 98%

Maximizes GPS Position Availability
- SingleSat™ updates in reduced visibility
- Superior urban canyon performance
- FoliageLock™ for weak signal tracking

FAMILY HIGHLIGHTS

GSP2e/LP - Flexible Digital IC
- Microprocessor throughput measured at up to 40 MIPS
- 8k of cache for improved throughput
- On-chip 1Mb SRAM for GPS navigation
- Integrated high-precision Real-Time Clock
- Extensive GPS receiver peripherals
- 2 UARTS, high speed serial bus, battery backed SRAM, >40 GPIO,

GRF2i/LP - Low Power RFIC
- On-chip VCO and reference oscillator
- Integrated LNA
- Uses less than 30 mA's of current
- Simplified digital interface

GSW2 Modular Software
- Easily integrated into existing systems
- 95% CPU throughput available for user tasks
- Tunable performance in all applications
- Robust development environment
- Compatible with SiRFloc and SiRFxtrac

SiRFstar II ARCHITECTURE

SiRFstar IIe/LP architecture sets the standard for high volume GPS performance. The SiRFstar IIe/LP still uses 1,920 correlators and 12 channels to provide fast acquisition and re-acquisition times, while keeping peak current to under 65 mA. TricklePower extends battery life even further by reducing average current to under 20mA. Now superior performance features like SingleSat, SnapLock, and FoliageLock are available using less power.

The chipset consists of the GSP2e/LP, a highly integrated digital chip with 40 MIPS of processing power and the GRF2i/LP, a lower power version of the GRF2i integrated front end. The GSW2 software completes the package providing flexible system architecture for stand-alone GPS based products. The SiRFstar IIe/LP also supports SiRF's high sensitivity stand-alone software, SiRFxtrac and multi-mode software, SiRFloc. When low power, low cost, and high performance matter SiRFstar IIe/LP is the best solution.

SiRFstar IIe/LP BLOCK DIAGRAM
APPLICATIONS

The SiRFstarIIe/LP is a flexible low-power GPS chip set that integrates into a postage-stamp sized receiver. It works well where GPS is the main function such as handheld GPS, marine GPS, or personal locators or where the design calls for stand-alone GPS functionality such as GPS integrated into the batteryback of a cell phone or in an add on compact flash card. The excess processing power can be used for user tasks such as running an LCD or controlling an Automatic Vehicle Location module.

CHIP ORDERING CONFIGURATION

<table>
<thead>
<tr>
<th>RF CHIP PACKAGES</th>
<th>Digital Chip Packages</th>
<th>Additional Software Options</th>
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</thead>
<tbody>
<tr>
<td>Chip Name</td>
<td>Chip PN</td>
<td>Package</td>
</tr>
<tr>
<td>SiRFstarII GRF2i/LP</td>
<td>GRF2i/LP-0210</td>
<td>LQFP, 48 pin</td>
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<tr>
<td>SiRFstarII GRF2i/LP (QFN)</td>
<td>GRF2i/LP-0214</td>
<td>(LPCC), 32 pin</td>
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<tr>
<td>SiRFstarII GSP2e/LP</td>
<td>GSP2e/LP-7450</td>
<td>TOFP, 16-bit, 100 pin</td>
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<tr>
<td>SiRFstarII GSP2e/LP</td>
<td>GSP2e/LP-7451</td>
<td>BGA, 16-bit, 144 pin</td>
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<tr>
<td>SiRFstarII GSP2e/LP</td>
<td>GSP2e/LP-7460</td>
<td>LQFP, 32-bit, 144 pin</td>
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<tr>
<td>SiRFxtrac (High Sensitivity stand alone software)</td>
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<td>SiRFLoc (High Sensitivity multimode software)</td>
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For more information, contact your SiRF representative, call our sales force on +1 (408) 467-0410, or visit us at www.sirf.com.