



# SiI9022A/SiI9024A HDMI Transmitter

## Data Brief

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## General Description

The SiI9022A/SiI9024A HDMI transmitter supports the High Definition Multimedia Interface (HDMI) Specification on a wide range of mobile products. High definition camcorders, digital still cameras, and personal mobile devices connect directly to a large installed base of HDMI TVs and DVI PC monitors by using the flexible audio and video interfaces provided by this ultra-low-power solution. S/PDIF or I<sup>2</sup>S inputs enable a pure digital audio connection to virtually any system audio processor or codec. This transmitter is the next generation of its family and is an enhanced replacement for the SiI9022/SiI9024 device, with lower power and enhanced features.

The SiI9024A transmitter supports High-bandwidth Digital Content Protection (HDCP) for devices that require secure content delivery.

## Video Input

- xvYCC metadata support
- BTA-T1004 video input format
- Integrated color space converter allows direct connection to all major MPEG decoders, including those that provide only an ITU-R.656 output
- Internal DE generator supports non-embedded sync formats.

## HDMI Output

- HDMI, HDCP, and DVI compatible
- TMDS<sup>®</sup> core runs at 165 MHz
- Video resolutions up to 1080p and UXGA (72-pin QFN package supports 165-MHz dual-edge mode)
- The SiI9024A transmitter is pre-programmed with HDCP keys and has completely self-sequencing HDCP detection and authentication, including SHA-1 for repeaters.

## Control Capability

- Consumer Electronics Control (CEC) interface incorporates an HDMI-compliant CEC I/O with hardware protocol and arbitration logic, and requires no external calibration
- Monitor detection is supported through both Hot Plug and Receiver Sense circuits
- Single slave I<sup>2</sup>C from host, passing through to master I<sup>2</sup>C interface for DDC connection, simplifies board layout and lowers cost
- Defaults to SiI9020 transmitter register-compatible mode for operation with existing legacy software.

## Digital Audio Interface:

- Four I<sup>2</sup>S inputs for Dolby Digital, DTS, or MPEG2 audio with programmable channel mapping (49-ball package supports one I<sup>2</sup>S input)
- DVD-Audio input (2 or up to 8 channels)
- MCLK is not required for I<sup>2</sup>S and S/PDIF
- S/PDIF input supports 2-channel PCM or compressed Dolby Digital and DTS digital
- 2:1 and 4:1 down-sampling to handle 96-kHz and 192-kHz audio streams.

## Power Management

- Flexible power management with hot-plug wakeup
- Ultra low power requirement: less than 90 mW active, 150  $\mu$ W standby.

## Packaging

- 81-ball VFBGA (4.0 x 4.0 mm) package
- 72-pin QFN (10 x 10 mm) package
- 49-ball VFBGA (4.0 x 4.0 mm) package
- Standard part covers extended (-20 to +85 °C) temperature range.

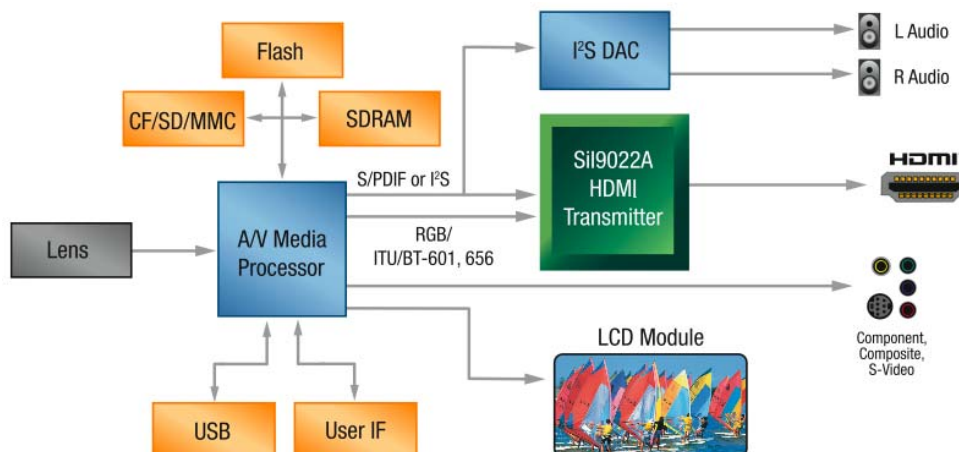


Figure 1. Typical Application (SiI9022A HDMI Transmitter Shown)

## Comparison of the SiI9022A/SiI9024A Device With Other HDMI Transmitters

Table 1 summarizes the differences among the previous Silicon Image HDMI transmitters and the SiI9022A/SiI9024A HDMI transmitters.

**Table 1. Summary of Features**

HDMI Transmitter	SiI9030	SiI9020	SiI9022	SiI9022-6	SiI9024	SiI9024-6	SiI9022A	SiI9024A	SiI9022A	SiI9024A	
							VFBGA	QFN			
<b>Video Input</b>											
Clock duty cycle	60/40	60/40	70/30	70/30	70/30	70/30	70/30	70/30	70/30	70/30	70/30
Max frequency	150 MHz	84 MHz	82.5 MHz	165 MHz	82.5 MHz	165 MHz	165 MHz	165 MHz	165 MHz <sup>3</sup>	165 MHz <sup>3</sup>	
Input signal level <sup>2</sup>	3.3 V	3.3 V	3.3 V or 1.8 V	3.3 V or 1.8 V	3.3 V or 1.8 V	3.3 V or 1.8 V	3.3 V or 1.8 V	3.3 V or 1.8 V	3.3 V or 1.8 V	3.3 V or 1.8 V	
<b>Audio Input</b>											
Max S/PDIF frequency	96 kHz	96 kHz	192 kHz	192 kHz	192 kHz	192 kHz	192 kHz	192 kHz	192 kHz	192 kHz	
I <sup>2</sup> S MCLK required?	Yes	Yes	Optional	Optional	Optional	Optional	Optional	Optional	Optional	Optional	
S/PDIF MCLK required?	Yes	Yes	Optional	Optional	Optional	Optional	Optional	Optional	Optional	Optional	
<b>DDC I<sup>2</sup>C Bus</b>											
Voltage tolerance <sup>1</sup>	5 V	5 V	5 V	5 V	5 V	5 V	5 V	5 V	5 V	5 V	
<b>HDCP</b>											
Encryption engine	Yes	No	No	No	Yes	Yes	No	Yes	No	Yes	
Auto authentication	No	No	No	No	Yes	Yes	No	Yes	No	Yes	
<b>Other</b>											
Core power supply	1.8 V	1.8 V	1.2 V	1.2 V	1.2 V	1.2 V	1.2 V	1.2 V	1.2 V	1.2 V	
I/O power supply <sup>2</sup>	3.3 V	3.3 V	3.3 V or 1.8 V	3.3 V or 1.8 V	3.3 V or 1.8 V	3.3 V or 1.8 V	3.3 V or 1.8V	3.3 V or 1.8 V	3.3 V or 1.8V <sup>4</sup>	3.3 V or 1.8 V <sup>4</sup>	
Package	80-pin TQFP	84-ball TFBGA	84-ball TFBGA or 81-ball VFBGA	84-ball TFBGA	84-ball TFBGA or 81-ball VFBGA	84-ball TFBGA	81-ball VFBGA or 49-ball VFBGA	81-ball VFBGA or 49-ball VFBGA	72-pin QFN	72-pin QFN	

**Notes:**

1. I<sup>2</sup>C inputs are 3.3-V or 5-V tolerant only when chip IOVCC is applied, except in the case of the SiI9022A/SiI9024A devices, for which the state of chip IOVCC doesn't matter.
2. The SiI9022A/SiI9024A 81-ball and 72-pin package supports both 1.8-V and 3.3-V threshold-compliant operation. The 49-ball package only supports 1.8-V compliant I/O. Both devices have 3.3-V tolerant I/O when IOVCC is 1.8 V.
3. Supports up to 165 MHz dual-edge and single-edge modes.
4. For dual-edge mode above 82.5 MHz, only 3.3 V ± 10% can be used for IOVCC.

## Ball and Pin Diagrams

### 81-ball VFBGA Package

Figure 2 shows the ball diagram for the SiI9022A/SiI9024A transmitter in the 81-ball package. Balls are shaded using the grouping shown in Figure 4 on page 5.

	1	2	3	4	5	6	7	8	9
A	HCTRL_IO	RSVD	GND	HDATA_O	HDATA_O	HDATA_O	HDATA_O	GND	EXT_SWING
B	CCTRL_IO	VDD	HDATA_O	HDATA_O	HDATA_O	HDATA_O	CCTRL_IO	CCTRL_I	RSVD
C	CCTRL_IO	CCTRL_IO	CCTRL_I	CVCC12	GND	AVCC12	AVCC12	HCTRL_IO	HCTRL_IO
D	GND	GND	VCC12	GND	VCC	GND	VCC12	HCTRL_O	CCTRL_O
E	VDATA_1	VDATA_1	VDATA_1	VDATA_1	VCC	ADATA_1	VCC12	VCC	VCC
F	VDATA_1	VDATA_1	VDATA_1	VDATA_1	VCC12	ADATA_1	ACTRL_1	ACTRL_1	ADATA_1
G	VDATA_1	VDATA_1	VDATA_1	VDATA_1	GND	VCC12	ADATA_1	ACTRL_1	ADATA_1
H	VDATA_1	VDATA_1	VCTRL_1	VDATA_1	GND	VDATA_1	VDATA_1	VDATA_1	VCTRL_I
J	VDATA_1	VDATA_1	VDATA_1	VDATA_1	GND	VDATA_1	VDATA_1	VCTRL_I	VCTRL_I

Ball Name	Purpose
VDATA_I	Video data Input
VCTRL_I	Video control Input
ADATA_I	Audio data Input (S/PDIF, I <sup>2</sup> S)
ACTRL_I	Audio control Input (WS, MCLK, SCK)
CCTRL_x	Chip control Input, Output, or Input/Output (INT, RESET, CSCL, CSDA, etc.)
HDATA_O	HDMI data Output (TMDS-level signals)
HCTRL_x	HDMI control Input, Output, or Input/Output

Figure 2. 81-ball Ball Diagram (Top View)

### 49-ball VFBGA Package

Figure 3 shows the ball diagram for the SiI9022A/SiI9024A transmitter in the 49-ball package. Balls are shaded using the grouping shown in Figure 4 on the next page.

	1	2	3	4	5	6	7
A	HDATA_O	HDATA_O	HDATA_O	HDATA_O	HDATA_O	HDATA_O	HDATA_O
B	HCTRL_IO	HDATA_O	GND	VCC12	CCTRL_IO	RSVDL	CCTRL_I
C	CCTRL_IO	CCTRL_IO	VDD	VCC12	CCTRL_I	CCTRL_O	CCTRL_IO
D	VDATA_I	VDATA_I	GND	GND	HCTRL_I	ACTRL_I	ADATA_I
E	VDATA_I	VDATA_I	VCC	VDATA_I	ACTRL_I	VDATA_I	ACTRL_I
F	VDATA_I	VDATA_I	VCTRL_I	VDATA_I	VDATA_I	VDATA_I	VCTRL_I
G	VDATA_I	VDATA_I	VDATA_I	VDATA_I	VDATA_I	VCTRL_I / ADATA_I	VCTRL_I

Ball Name	Purpose
VDATA_I	Video data Input
VCTRL_I	Video control Input
ADATA_I	Audio data Input (S/PDIF, I <sup>2</sup> D)
ACTRL_I	Audio control Input (WS, MCLK, SCK)
CCTRL_x	Chip control Input, Output, or Input/Output (INT, RESET, CSCL, CSDA, etc.)
HDATA_O	HDMI data Output (TMDS-level signals)
HCTRL_x	HDMI control Input, Output, or Input/Output

Figure 3. 49-ball Ball Diagram (Top View)

## 72-pin QFN Package

Figure 4 shows the pin diagram for the SiI9022A/SiI9024A transmitter in the 72-pin package.

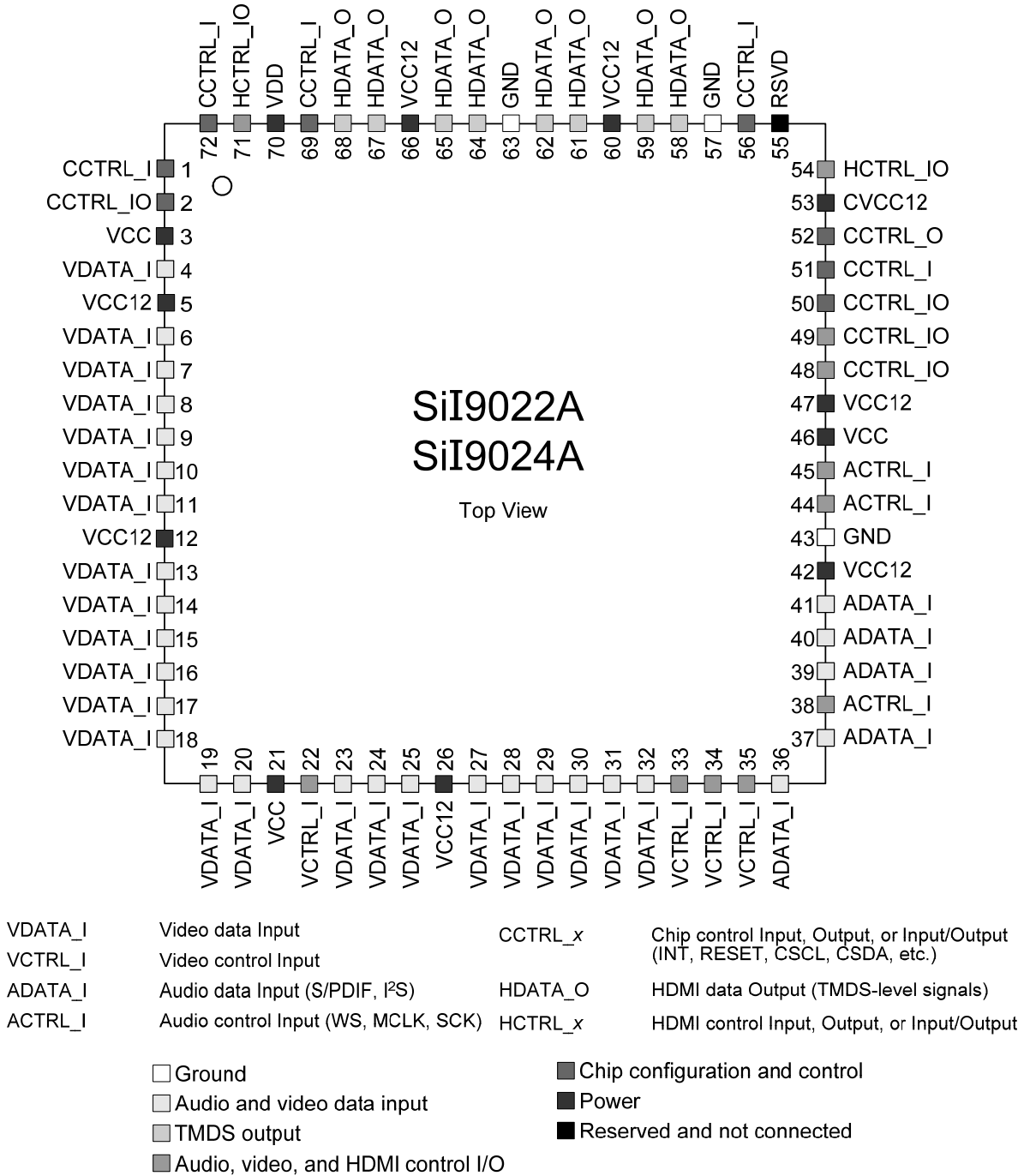


Figure 4. 72-pin QFN Pin Diagram (Top View)

# Packaging

## 49-ball Package Dimensions

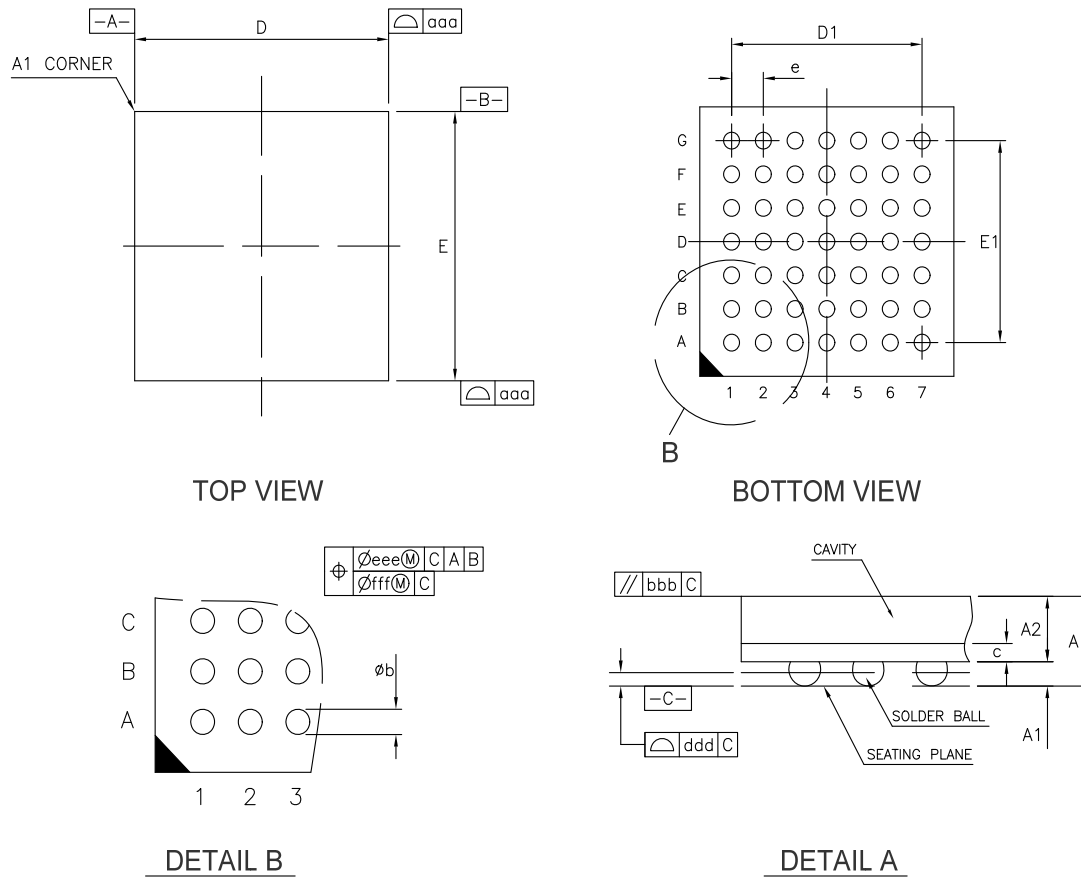


Figure 5. 49-ball VFBGA Package Diagram (SiI902nAYBT)

### JEDEC Package Code MO-225

Item	Description	Min	Typ	Max
A	Thickness	—	—	0.80
A1	Stand-off	0.13	0.18	0.23
A2	Substrate thickness + Mold thickness	0.446	0.486	0.526
D	Body size	3.90	4.00	4.10
E	Body size	3.90	4.00	4.10
D1	Footprint	—	3.00	—
E1	Footprint	—	3.00	—
b	Ball width	0.20	0.25	0.30
e	Ball pitch	—	0.50	—
aaa	Package edge tolerance	0.10		
bbb	Mold flatness	0.10		
ddd	Coplanarity	0.08		
eee	Ball offset (package)	0.15		
fff	Ball offset (ball)	0.05		

All dimensions are in millimeters.



## 81-ball Package Dimensions

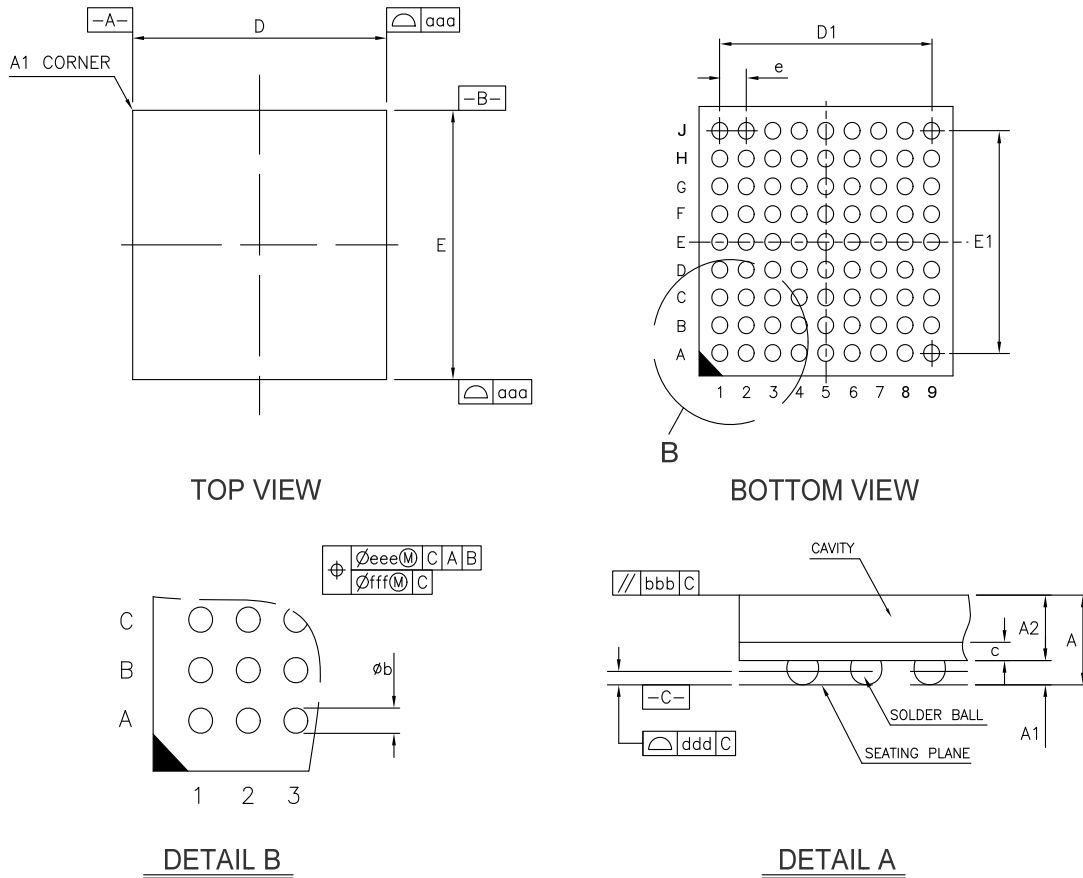


Figure 6. 81-ball VFBGA Package Diagram (SiI902nARBT)

### JEDEC Package Code MO-225

Item	Description	Min	Typ	Max
A	Thickness	—	—	0.80
A1	Stand-off	0.13	0.18	0.23
A2	Substrate thickness + Mold thickness	0.446	0.486	0.526
D	Body size	3.90	4.00	4.10
E	Body size	3.90	4.00	4.10
D1	Footprint	—	3.20	—
E1	Footprint	—	3.20	—
b	Ball width	0.20	0.25	0.30
e	Ball pitch	—	0.40	—
aaa	Package edge tolerance	0.10		
bbb	Mold flatness	0.10		
ddd	Coplanarity	0.08		
eee	Ball offset (package)	0.15		
fff	Ball offset (ball)	0.05		

All dimensions are in millimeters.

## 72-pin Package Dimensions

These drawings are not to scale.

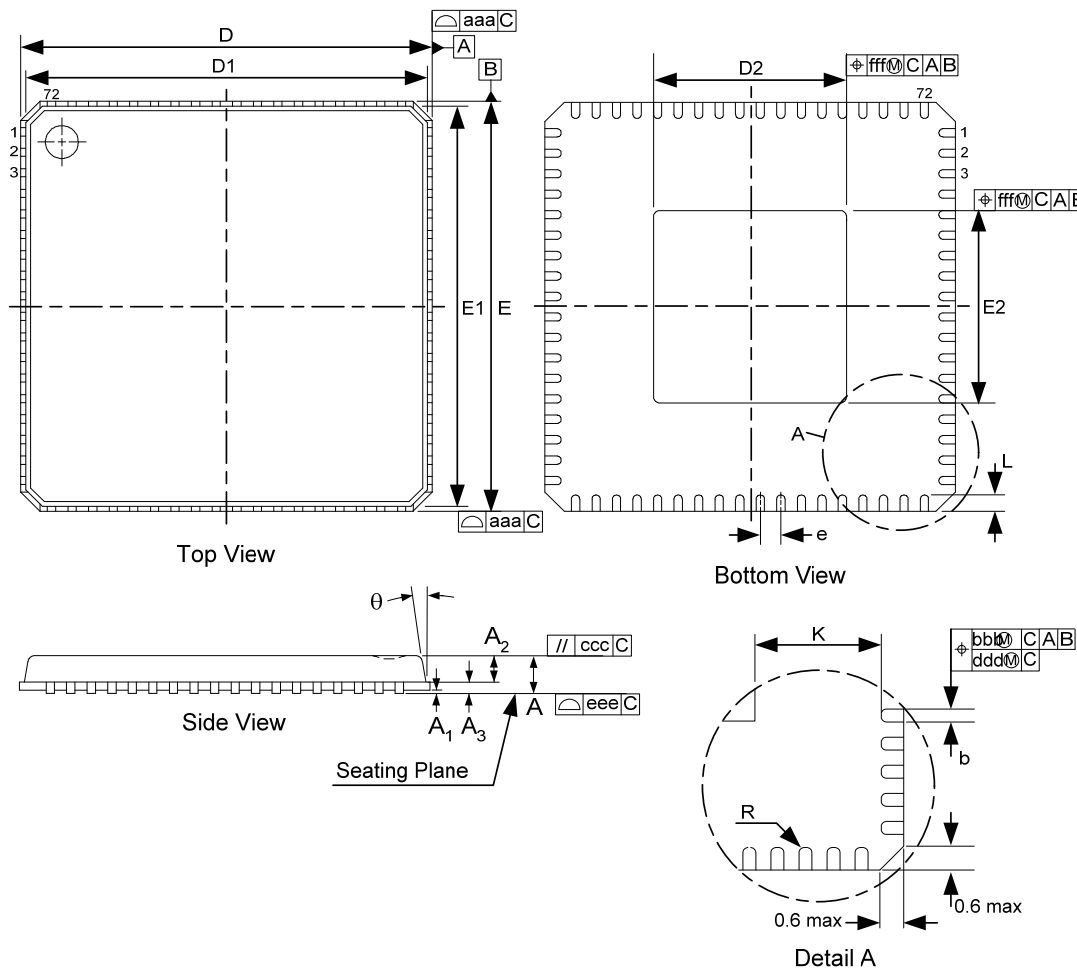


Figure 7. 72-pin QFN Package Diagram (SiI902nACNU)

JEDEC Package Code MO-220

Item	Description	Min	Typ	Max
A	Thickness	0.80	0.85	0.90
A <sub>1</sub>	Stand-off	0.00	0.02	0.05
A <sub>2</sub>	Body thickness	0.60	0.65	0.70
A <sub>3</sub>		0.20 REF		
D	Footprint	10.00 BSC		
E	Footprint	10.00 BSC		
D <sub>1</sub>	Body size	9.75 BSC		
E <sub>1</sub>	Body size	9.75 BSC		
D <sub>2</sub>	ePad size	4.55	4.70	4.85
E <sub>2</sub>	ePad size	4.55	4.70	4.85
b	Plated lead width	0.18	0.23	0.28

Item	Description	Min	Typ	Max
e	Lead pitch	0.50 BSC		
K	ePad-to-pin clearance	0.20	—	—
L	Lead foot length	0.30	0.40	0.50
R	Lead radius	0.09	—	—
θ	Lead foot angle	0°	—	14°
aaa	Package edge tolerance	—	—	0.15
bbb		—	—	0.10
ccc		—	—	0.10
ddd		—	—	0.05
eee		—	—	0.08
fff	ePad edge tolerance	—	—	0.10

# Marking Specification

Marking drawings are not to scale.

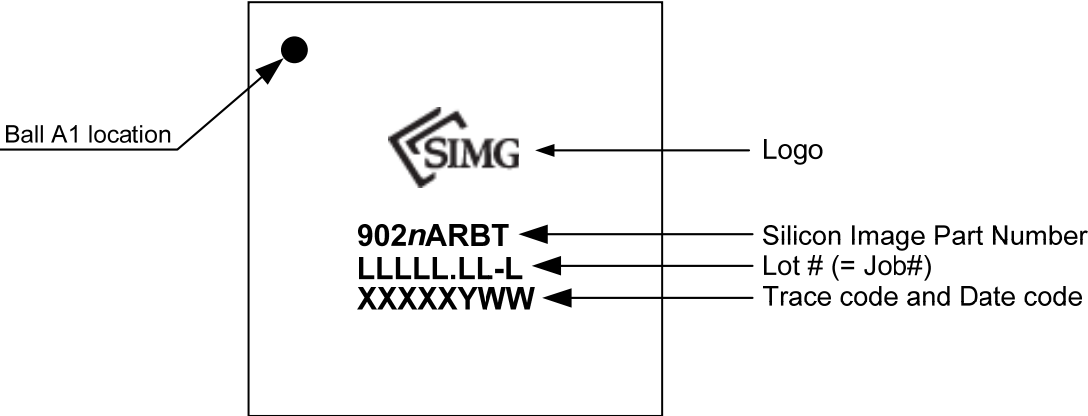


Figure 8. Marking Diagram (SiI902nARBT)

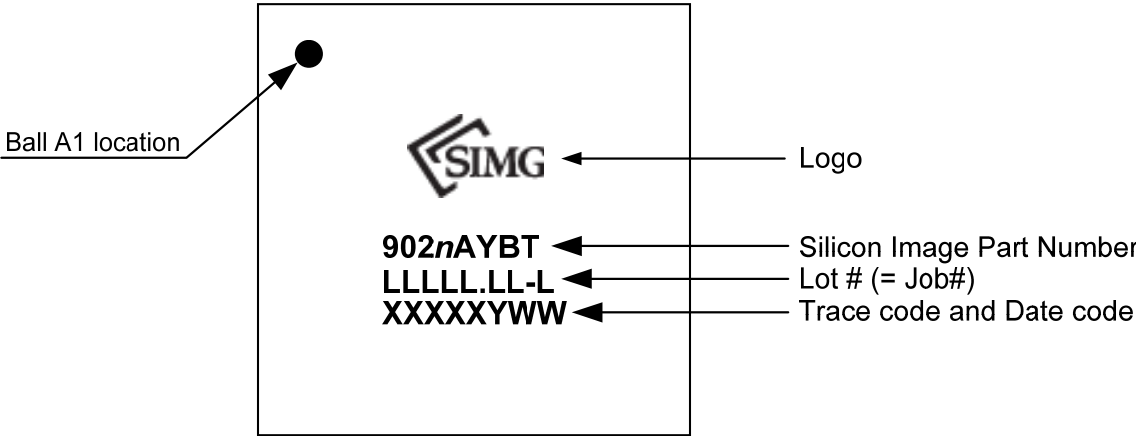


Figure 9. Marking Diagram (SiI902nAYBT)

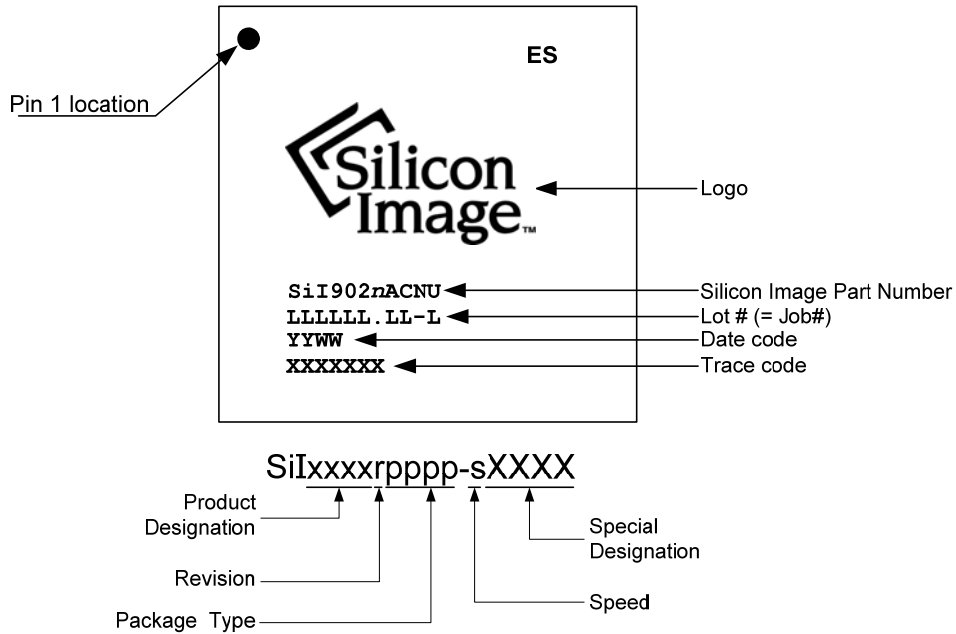


Figure 10. Marking Diagram (SiI902nACNU)

## Ordering Information

Part Numbers	Package Type	Pixel Clock Range	Security	Temperature Grade
SiI9022ARBT	81-ball 4 x 4 mm VFBGA	25–165 MHz	—	Extended (–20 to +85 °C)
SiI9022AYBT	49-ball 4 x 4 mm VFBGA	25–165 MHz	—	Extended (–20 to +85 °C)
SiI9022ACNU	72-pin 10 x 10 mm QFN	25–165 MHz	—	Extended (–20 to +85 °C)
SiI9024ARBT	81-ball 4 x 4 mm VFBGA	25–165 MHz	HDCP	Extended (–20 to +85 °C)
SiI9024AYBT	49-ball 4 x 4 mm VFBGA	25–165 MHz	HDCP	Extended (–20 to +85 °C)
SiI9024ACNU	72-pin 10 x 10 mm QFN	25–165 MHz	HDCP	Extended (–20 to +85 °C)

The universal package can be used in both lead-free and ordinary process lines.

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1060 E. Arques Avenue  
Sunnyvale, CA 94085  
T 408.616.4000 F 408.830.9530  
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