

Voltage comparator

NE527

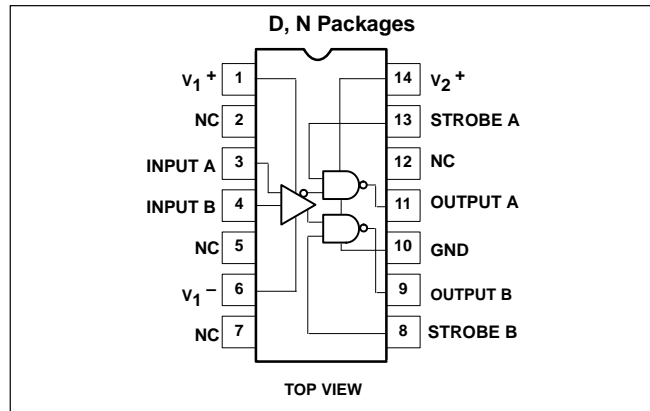
DESCRIPTION

The NE527 is a high-speed analog voltage comparator which, for the first time, mates state-of-the-art Schottky diode technology with the conventional linear process. This allows simultaneous fabrication of high speed TTL gates with a precision linear amplifier on a single monolithic chip. The NE527 is similar in design to the Philips Semiconductors NE529 voltage comparator except that it incorporates an "Emitter-Follower" input stage for extremely low input currents. This opens the door to a whole new range of applications for analog voltage comparators.

FEATURES

- 15ns propagation delay
- Complementary output gates
- TTL or ECL compatible outputs
- Wide common-mode and differential voltage range
- Typical gain of 5000

PIN CONFIGURATIONS



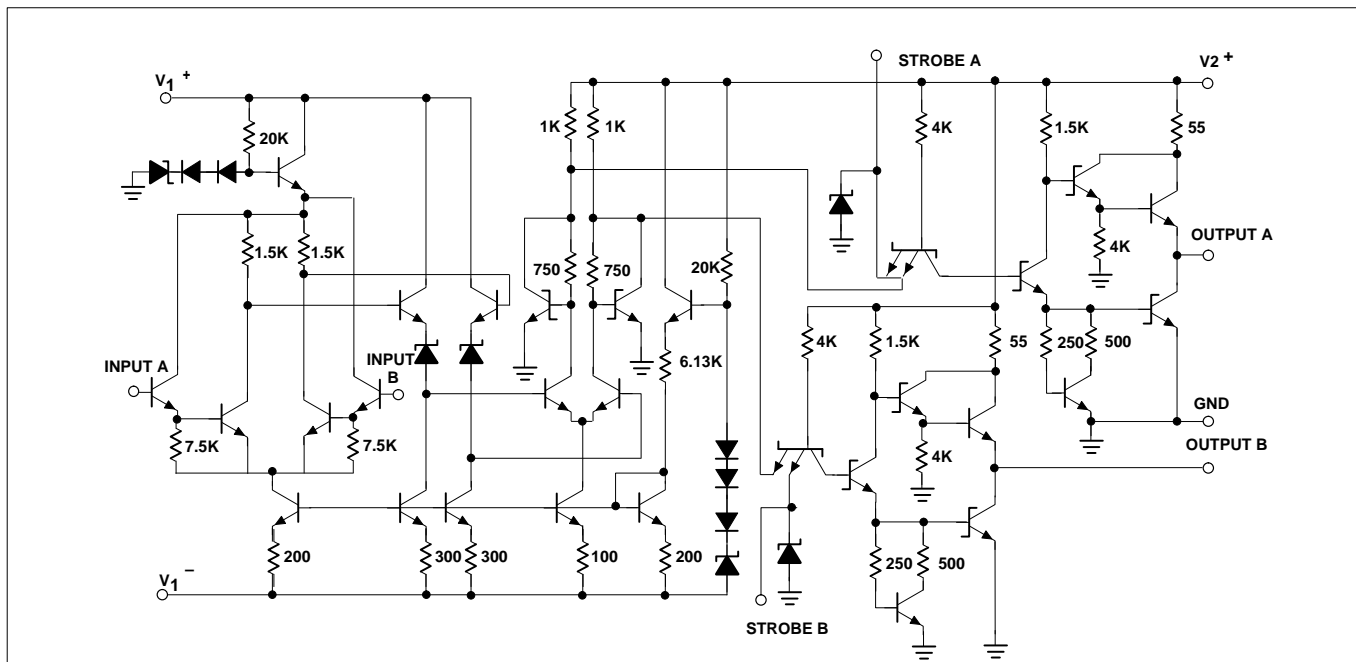
APPLICATIONS

- A/D conversion
- ECL-to-TTL interface
- TTL-to-ECL interface
- Memory sensing
- Optical data coupling

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
14-Pin Plastic Dual In-Line Package (DIP)	0 to +70°C	NE527N	0405B
14-Pin Small Outline (SO) Package	0 to +70°C	NE527D	0175D

EQUIVALENT SCHEMATIC



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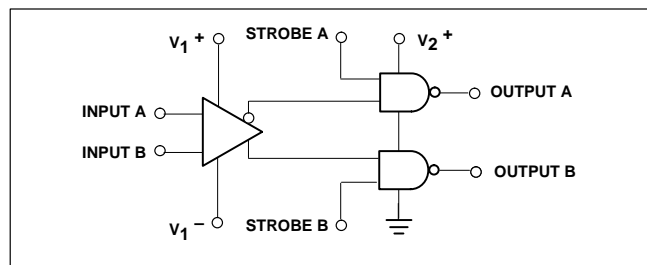
ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{1+}	Positive supply voltage	+15	V
V_{1-}	Negative supply voltage	-15	V
V_{2+}	Gate supply voltage	+7	V
V_{OUT}	Output voltage	+7	V
V_{IN}	Differential input voltage	± 5	V
V_{CM}	Input common mode voltage	± 6	V
P_D	Max power dissipation ¹ 25°C ambient (still air)		
	N package	1420	mW
	D package	1040	mW
T_A	Operating temperature range	0 to +70	°C
T_{STG}	Storage temperature range	-65 to +150	°C
T_{SOLD}	Lead soldering temperature (10sec max)	+300	°C

NOTES:

- Derate above 25°C, at the following rates:
 N package 11.4mW/°C
 D package 8.3mW/°C

BLOCK DIAGRAM



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DC ELECTRICAL CHARACTERISTICSV₁₊=10V, V₁₋=-10V, V₂₊=+5.0V, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	NE527			UNIT
			Min	Typ	Max	
Input characteristics						
V _{OS}	Input offset voltage @ 25°C over temperature range				6 10	mV
I _{BIAS}	Input bias current @ 25°C over temperature range				2 4	μA
I _{OS}	Input offset current @ 25°C over temperature range	V _{IN} =0V			0.75 1	μA
V _{CM}	Common-mode voltage range		-5		+5	V
Gate characteristics						
V _{OUT}	Output Voltage "1" State "0" State	V ₂₊ =4.75V, I _{SOURCE} =-1mA V ₂₊ =4.75V, I _{SINK} =10mA	2.7	3.3		V V
	Strobe inputs "0" Input current ¹ "1" Input current @ 25°C ¹ Over temperature range "0" Input voltage "1" Input voltage	V ₂₊ =5.25V, V _{STROBE} =0.5V V ₂₊ =5.25V, V _{STROBE} =2.7V V ₂₊ =5.25V, V _{STROBE} =2.7V V ₂₊ =4.75V V ₂₊ =4.75V			-2 100 200 0.8	mA μA μA V V
I _{SC}	Short-circuit output current	V ₂₊ =5.25V, V _{OUT} =0V	-18		-70	mA
Power supply requirements						
V ₁₊ V ₁₋ V ₂₊	Supply voltage		5 -6 4.75		10 -10 5.25	V V V
I ₁₊ I ₁₋ I ₂₊	Supply current	V ₁₊ =10V, V ₁₋ =-10V V ₂₊ =5.25V Over temp. Over temp. Over temp.			5 10 20	mA mA mA

NOTES:

1. See Logic Function Table.

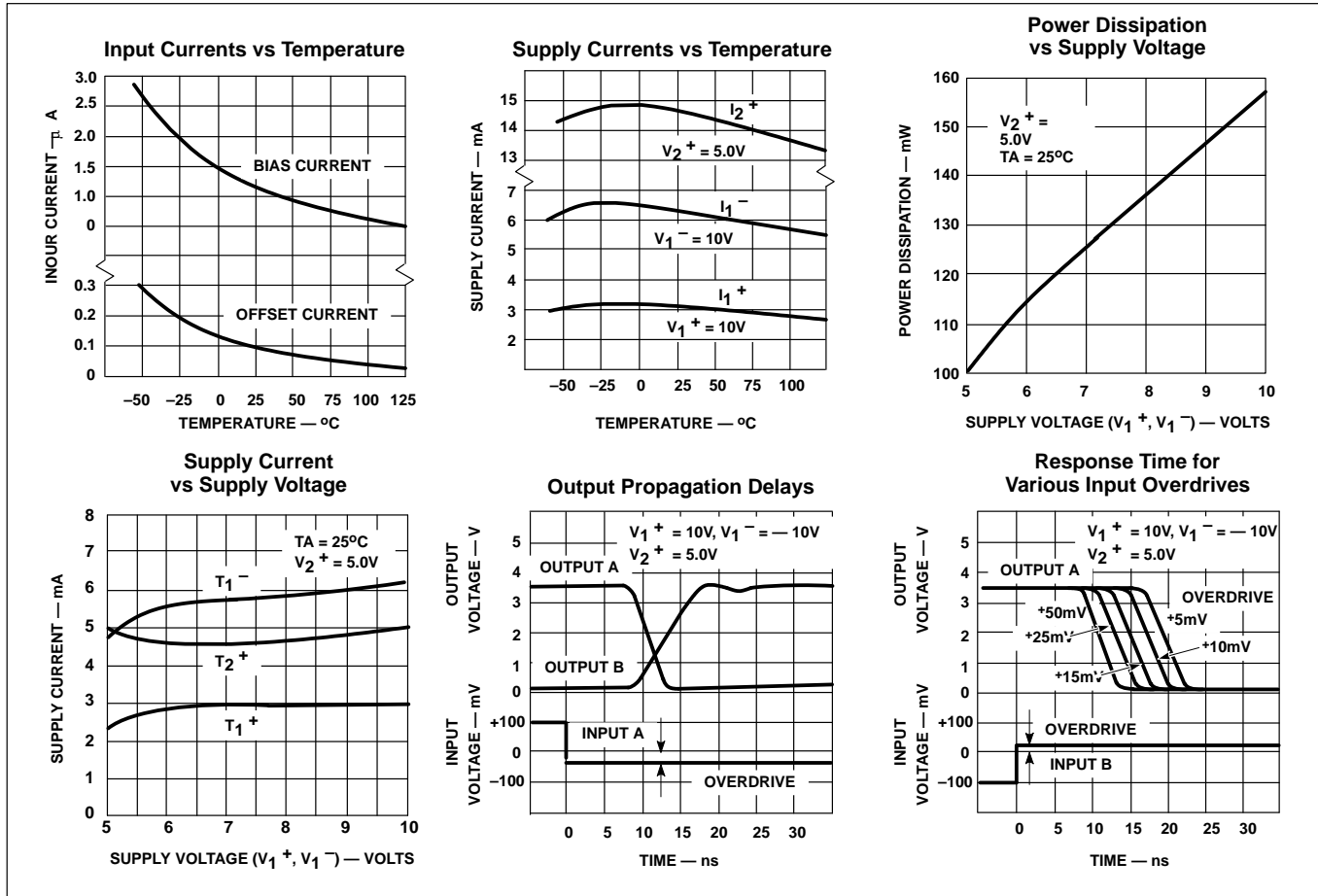
AC ELECTRICAL CHARACTERISTICST_A=25°C, unless otherwise specified. (See AC test circuit)

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
t _{PLH} t _{PHL}	Transient response propagation delay time Low-to-High High-to-Low	V _{IN} =±100mV step		16 14	26 24	ns ns
	Delay between output A and B			2	5	ns
t _{ON} t _{OFF}	Strobe delay time Turn-on time Turn-off time			6 6		ns ns

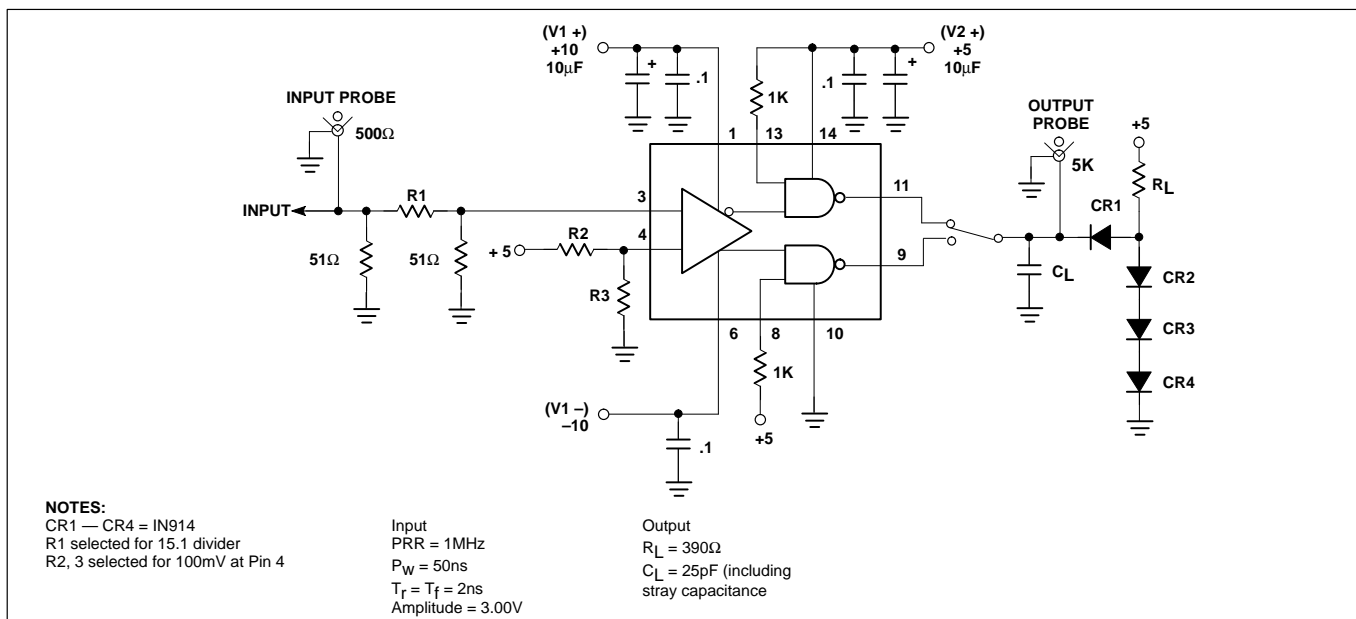
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TYPICAL PERFORMANCE CHARACTERISTICS



RESPONSE TIME TEST CIRCUIT



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APPLICATIONS

One of the main features of the device is that supply voltages (V_{1+} , V_{1-}) need not be balanced, as in the following diagrams. For proper operation, however, negative supply (V_{1-}) should always be at least 6V more than the ground terminal (Pin 6). Input common-mode

range should be limited to values of 2V less than the supply voltages (V_{1+} and V_{1-}) up to a maximum of $\pm 5V$ as supply voltages are increased. It is also important to note that Output A is in phase with Input A and Output B is in phase with Input B.

LOGIC FUNCTION

V_{ID} (A+, B-)	STROBE A	STROBE B	OUTPUT A	OUTPUT B	COMMENT
$V_{ID} \leq -V_{OS}$	H	X	L	H	Read I_{IHA} , I_{ILB}
$-V_{OS} < V_{ID} < V_{OS}$	H	H	Undefined	Undefined	
$V_{ID} \geq V_{OS}$	X	H	H	L	Read I_{ILA} , I_{IHB}
X	L	L	H	H	

TYPICAL APPLICATIONS

