10104
Gate

Quad 2-Input AND Gate
Product Specification

ECL Products

DESCRIPTION

The 10104 is a high-speed logic, low power, AND function.

All unused inputs can be left open due to integrated pull-down resistors which avoid the need for a supply voltage.

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT ($-I_{EE}$)
10104	2.7ns	20mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGE $V_{CC1} = V_{CC2} = GND$; $V_{EE} = -5.2V$ $T_A = -30°C$ to $+85°C$
Plastic DIP	10104N
Ceramic DIP	10104F

PIN DESCRIPTION

PINS	DESCRIPTION
D_0–D_7	Data Inputs
Q_0, Q_1, Q_2, Q_4	Data Outputs (AND)
$\overline{Q}_3$	Data Output (NAND)

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PIN CONFIGURATION

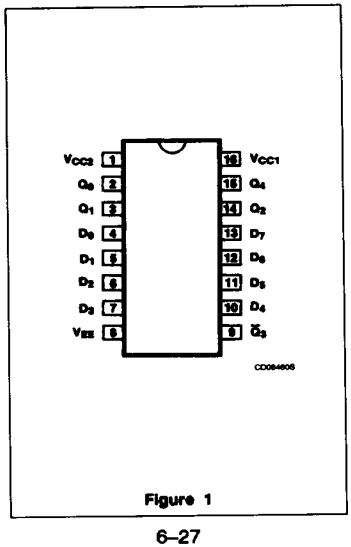


Figure 1

LOGIC SYMBOL

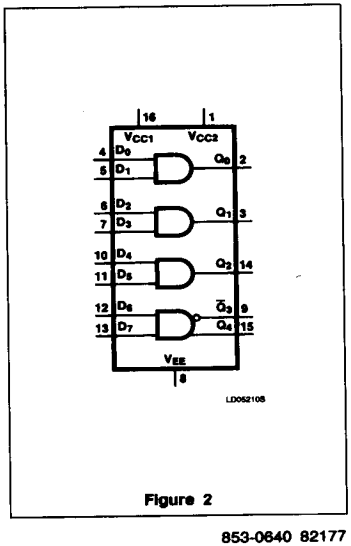


Figure 2

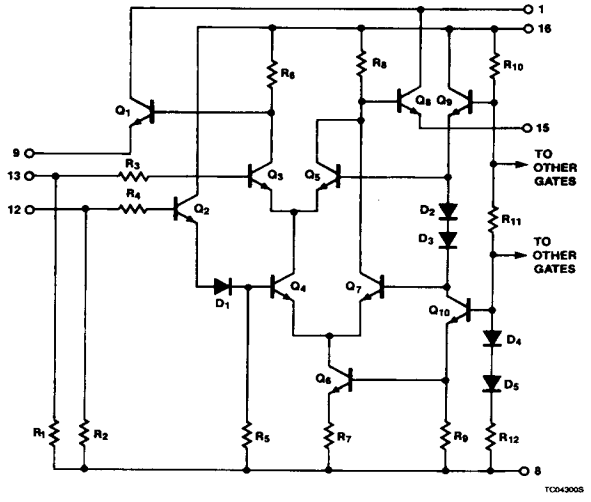
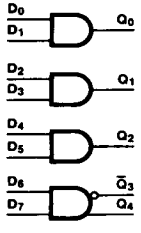


Figure 3. Circuit Diagram (One Gate)



$Q_0 = D_0 \cdot D_1$
$Q_1 = D_2 \cdot D_3$
$Q_2 = D_4 \cdot D_5$
$Q_3 = \overline{Q}_4$
$Q_4 = D_6 \cdot D_7$

Positive logic
H = HIGH state
(the more positive voltage) = 1
L = LOW state
(the more negative voltage) = 1

LD04651S

Figure 4. Logic Diagram

ABSOLUTE MAXIMUM RATINGS (Operation beyond the limits set forth in this table may impair useful life of the device. Unless otherwise noted, these limits are specified over the operating ambient temperature range.)

PARAMETER			10K ECL	UNIT
V_{EE}	Supply voltage		−8.0	V
V_{IN}	Input voltage (V_{IN} should never be more negative than V_{EE})		0 to V_{EE}	V
I_O	Output current		−50	mA
T_S	Storage temperature		−55 to +150	°C
T_J	Maximum junction temperature	Ceramic package	+165	°C
		Plastic package	+150	°C

DC OPERATING CONDITIONS

PARAMETER			10K ECL			UNIT
			Min	Nom	Max	
V_{CC1}, V_{CC2}	Circuit ground		0	0	0	V
V_{EE}	Supply voltage (negative)			−5.2		V
V_{IH}	HIGH level input voltage	T_A = −30°C			−890	mV
		T_A = +25°C			−810	mV
		T_A = +85°C			−700	mV
V_{IHT}	HIGH level input threshold voltage	T_A = −30°C	−1205			mV
		T_A = +25°C	−1105			mV
		T_A = +85°C	−1035			mV
V_{ILT}	LOW level input threshold voltage	T_A = −30°C			−1500	mV
		T_A = +25°C			−1475	mV
		T_A = +85°C			−1440	mV
V_{IL}	LOW level input voltage	T_A = −30°C	−1890			mV
		T_A = +25°C	−1850			mV
		T_A = +85°C	−1825			mV
T_A	Operating ambient temperature		−30	+25	+85	°C

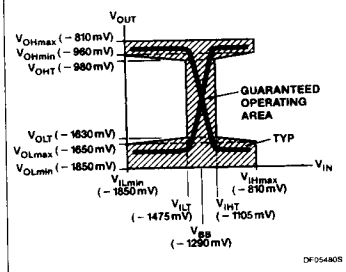
NOTE:
When operating at V_{EE} other than specified voltage (−5.2V), the DC and AC Characteristics will vary slightly from specified values. (See table of DC Characteristics)

DC ELECTRICAL CHARACTERISTICS $V_{CC1} = V_{CC2} = GND$, $V_{EE} = -5.2V \pm 0.010V$, $T_A = -30°C$ to $+85°C$, output loading with 50Ω to $-2.0V \pm 0.010V$, unless otherwise specified[1,3]

PARAMETER			MIN	TYP	MAX	UNIT	TEST CONDITIONS[2]
V_{OH}	HIGH level output voltage	$T_A = -30°C$	-1060		-890	mV	For Q_n outputs, apply V_{IHmax} to all inputs. For $\overline{Q}_3$ output, apply V_{ILmin} to all inputs.
		$T_A = +25°C$	-960		-810	mV	
		$T_A = +85°C$	-890		-700	mV	
V_{OHT}	HIGH level output threshold voltage	$T_A = -30°C$	-1080			mV	For Q_n outputs, apply V_{IHT} to one gate input with V_{IHmax} applied to the other gate input. For $\overline{Q}_3$ output, apply V_{ILT} to one gate input with V_{IHmax} applied to the other gate input.
		$T_A = +25°C$	-980			mV	
		$T_A = +85°C$	-910			mV	
V_{OLT}	LOW level output threshold voltage	$T_A = -30°C$			-1655	mV	For Q_n outputs, apply V_{ILT} to one gate input with V_{IHmax} applied to the other gate input. For $\overline{Q}_3$ output, apply V_{IHT} to one gate input with V_{IHmax} applied to the other gate input.
		$T_A = +25°C$			-1630	mV	
		$T_A = +85°C$			-1595	mV	
V_{OL}	LOW level output voltage	$T_A = -30°C$	-1890		-1675	mV	For Q_n outputs, apply V_{ILmin} to all inputs. For $\overline{Q}_3$ output, apply V_{IHmax} to all inputs.
		$T_A = +25°C$	-1850		-1650	mV	
		$T_A = +85°C$	-1825		-1615	mV	
I_{IH}	HIGH level input current (D_0, D_3, D_4, D_7 inputs)	$T_A = -30°C$			425	µA	Apply V_{IHmax} to each input under test, one at a time, with V_{ILmin} applied to all other inputs.
		$T_A = +25°C$			265	µA	
		$T_A = +85°C$			265	µA	
	HIGH level input current (D_1, D_2, D_5, D_6 inputs)	$T_A = -30°C$			350	µA	
		$T_A = +25°C$			220	µA	
		$T_A = +85°C$			220	µA	
I_{IL}	LOW level input current	$T_A = -30°C$	0.5			µA	Apply V_{ILmin} to each input under test, one at a time, with V_{IHmax} applied to all other inputs.
		$T_A = +25°C$	0.5			µA	
		$T_A = +85°C$	0.3			µA	
$-I_{EE}$	V_{EE} supply current	$T_A = -30°C$			39	mA	
		$T_A = +25°C$		20	35	mA	
		$T_A = +85°C$			39	mA	
$\frac{\Delta V_{OH}}{\Delta V_{EE}}$	HIGH level output voltage compensation	$T_A = +25°C$		0.016		V/V	
$\frac{\Delta V_{OL}}{\Delta V_{EE}}$	LOW level output voltage compensation			0.250		V/V	
$\frac{\Delta V_{BB}}{\Delta V_{EE}}$	Reference bias voltage compensation			0.148		V/V	

NOTES:

1. The specified limits represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
2. Conditions for testing shown in the tables are not necessarily worst case. For worst-case testing guidelines, refer to Section 3 Testing, DC Testing.
3. The specified limits shown in the DC Characteristics can be met only after thermal equilibrium has been established. Thermal equilibrium is established by applying power for at least 2 minutes while maintaining transverse air flow of 2.5 meters/s (500 linear feet/min) over the device either mounted in the test socket or on the printed circuit board. Test voltage values are given in the DC Operating Conditions and defined in Figure 5.



NOTES:

V_{IHmax} – Maximum HIGH level input voltage (the most positive V_{IH}).
V_{IHT} – HIGH level input threshold voltage.
V_{ILT} – LOW level input threshold voltage.
V_{ILmin} – Minimum LOW level input voltage (the most negative V_{IL}).
V_{OHmax} – Maximum HIGH level output voltage (the most positive V_{OH}) under the specified input and loading condition.
V_{OHmin} – Minimum HIGH level output voltage (the most negative V_{OH}) under the specified input and loading condition.
V_{OHT} – HIGH level output threshold voltage with the inputs set to their respective threshold levels.
V_{OLT} – LOW level output threshold voltage with the inputs set to their respective threshold levels.
V_{OLmax} – Maximum LOW level output voltage (the most positive V_{OL}) under the specified input and loading conditions.
V_{OLmin} – Minimum LOW level output voltage (the most negative V_{OL}) under the specified input and loading conditions.
V_{BB} – Reference bias voltage (the internally generated reference voltage which is used to set the input and output threshold level).

Figure 5. Transfer Characteristics

AC ELECTRICAL CHARACTERISTICS $V_{CC1} = V_{CC2} = +2.0V \pm 0.010V$, $V_{EE} = -3.2V \pm 0.010V$

PARAMETER	$T_A = -30°C$		$T_A = +25°C$			$T_A = +85°C$		UNIT	TEST CONDITIONS
	Min	Max	Min	Typ	Max	Min	Max		
t_{PLH} Propagation delay	1.0	4.3	1.0	2.7	4.0	1.0	4.2	ns	Figs. 6, 7, 8
t_{PHL} D_n to Q_n, $\overline{Q}_3$	1.0	4.3	1.0	2.7	4.0	1.0	4.2	ns	
t_{TLH} Transition time	1.5	3.7	1.5	2.0	3.5	1.5	3.6	ns	Figs. 6, 7, 8
t_{THL} 20% to 80%, 80% to 20%	1.5	3.7	1.5	2.0	3.5	1.5	3.6	ns	

AC WAVEFORMS

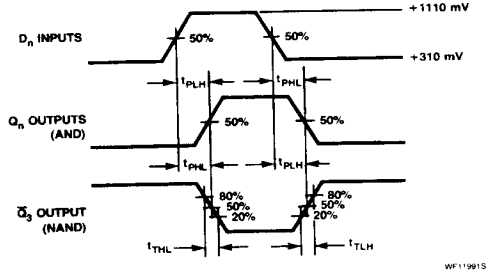
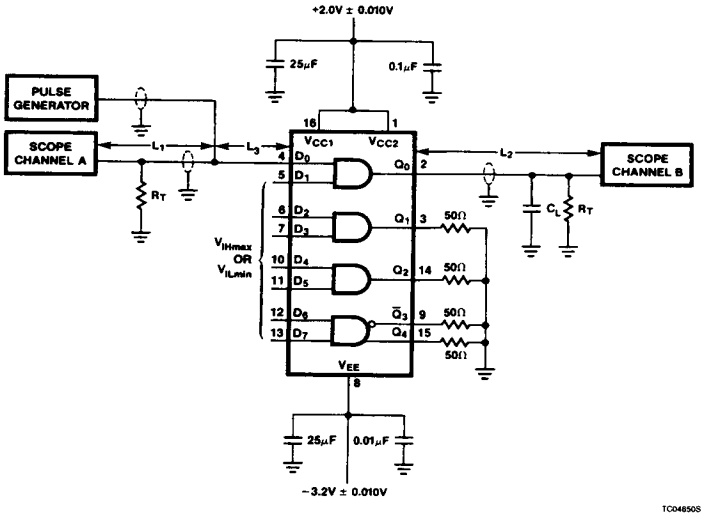


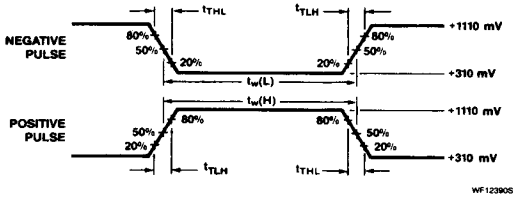
Figure 6. Propagation Delay and Transition Times

TEST CIRCUITS AND WAVEFORMS



NOTES:
1. $V_{CC1} = V_{CC2} = +2V \pm 0.010V$, $V_{EE} = -3.2V \pm 0.010V$
2. Decoupling 0.1μF and 25μF from GND to V_{CC}. 0.01μF and 25μF from GND to V_{EE}. (0.01 and 0.1μF capacitors should be NPO Ceramic or MLC type). Decoupling capacitors should be placed as close as physically possible to the DUT and lead length should be kept to less than 1/4 inch (6mm).
3. All unused inputs should be connected to either HIGH or LOW state consistent with the LOGIC function required.
4. All unused outputs are loaded with 50Ω to GND.
5. L_1 and L_2 are equal length 50Ω impedance lines. L_3, the distance from the DUT pin to the junction of the cable from the Pulse Generator and the cable to the Scope, should not exceed 1/4 inch (6mm).
6. $R_T = 50\Omega$ terminator internal to Scope.
7. The unmatched wire stub between coaxial cable and pins under test must be less than 1/4 inch (6mm) long for proper test.
8. C_L = Fixture and stray capacitance ≤ 3pF.
9. Any unterminated stubs connected anywhere along the transmission line between the Pulse Generator and the DUT or between the DUT and the Scope should not exceed 1/4 inch (6mm) in length (refer to section on AC setup procedure).
10. All 50Ω resistors should have tolerance of ±1% or better.

Figure 7. AC Test Circuit for 10104



INPUT PULSE REQUIREMENTS $V_{CC1} = V_{CC2} = +2.0V \pm 0.010V$, $V_{EE} = -3.2V \pm 0.010V$, V_T = GND (0V)					
Family	**Amplitude**	**Rep Rate**	**Pulse Width**	**t_{TLH}**	**t_{THL}**
10K ECL	800mVp-p	1MHz	500ns	2.0 ±0.2ns	2.0 ±0.2ns

Figure 8. Input Pulse Definition