BF989

SILICON N-CHANNEL DUAL GATE MOS-FET

Depletion type field-effect transistor in a plastic SOT143 microminiature envelope with source and substrate interconnected. This MOS-FET tetrode is intended for use in u.h.f. applications in television tuners. The device is also suitable for use in professional communication equipment.

The device is protected against excessive input voltage surges by integrated back-to-back diodes between gates and source.
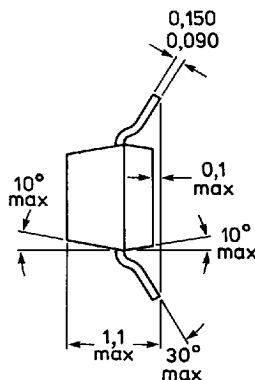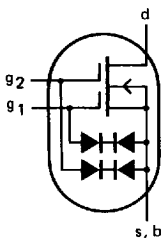
QUICK REFERENCE DATA

Drain-source voltage	V_{DS}	max.	20	V
Drain current	I_D	max.	20	mA
Total power dissipation up to $T_{amb} = 60\ ^\circ C$	P_{tot}	max.	200	mW
Junction temperature	T_j	max.	150	$^\circ C$
Transfer admittance at f = 1 kHz $I_D = 7$ mA; $V_{DS} = 10$ V; $+ V_{G2-S} = 4$ V	$|y_{fs}|$	typ.	12	mS
Input capacitance at gate 1; f = 1 MHz $I_D = 7$ mA; $V_{DS} = 10$ V; $+ V_{G2-S} = 4$ V	C_{ig1-s}	typ.	1.8	pF
Feedback capacitance at f = 1 MHz $I_D = 7$ mA; $V_{DS} = 10$ V; $+ V_{G2-S} = 4$ V	C_{rs}	typ.	25	fF
Noise figure at $G_S = 2$ mS; $B_S = B_S$ opt $I_D = 7$ mA; $V_{DS} = 10$ V; $+ V_{G2-S} = 4$ V; f = 800 MHz	F	typ.	2.8	dB

MECHANICAL DATA

Fig.1 SOT143.

Dimensions in mm

Marking code:
BF989 = MAp

Pinning:

1 = source
2 = drain
3 = gate 2
4 = gate 1
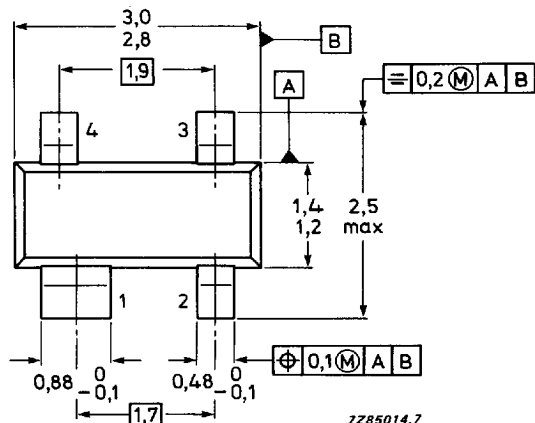
See also *Soldering recommendations.*

TOP VIEW

7Z85014.7

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	V_{DS}	max.	20	V
Drain current (DC or average)	I_D	max.	20	mA
Gate 1 - source current	$\pm I_{G1\text{-}S}$	max.	10	mA
Gate 2 - source current	$\pm I_{G2\text{-}S}$	max.	10	mA
Total power dissipation up to T_{amb} = 60 °C (note 1)	P_{tot}	max.	200	mW
Storage temperature range	T_{stg}		—65 to + 150	°C
Junction temperature	T_j	max.	150	°C

THERMAL RESISTANCE

From junction to ambient in free air (note 1)	$R_{th\ j\text{-}a}$	=	460	K/W

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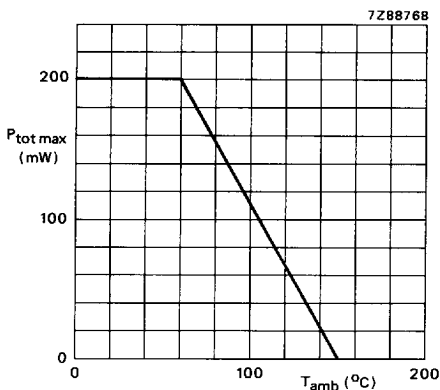
Fig.2 Power derating curve.

Note

1. Device mounted on a ceramic substrate of 8 mm x 10 mm x 0.7 mm.

Silicon n-channel dual gate MOS-FET

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STATIC CHARACTERISTICS

T_j = 25 ^{O}C unless otherwise specified

Gate cut-off currents
$\pm V_{G1-S}$ = 5 V; V_{G2-S} = V_{DS} = 0	$\pm I_{G1-SS}$	max.	50 nA
$\pm V_{G2-S}$ = 5 V; V_{G1-S} = V_{DS} = 0	$\pm I_{G2-SS}$	max.	50 nA

Drain current
V_{DS} = 10 V; V_{G1-S} = 0; + V_{G2-S} = 4 V	I_{DSS}		2 to 20 mA

Gate-source breakdown voltages
$\pm I_{G1-SS}$ = 10 mA; V_{G2-S} = V_{DS} = 0	$\pm V_{(BR)G1-SS}$		6 to 20 V
$\pm I_{G2-SS}$ = 10 mA; V_{G1-S} = V_{DS} = 0	$\pm V_{(BR)G2-SS}$		6 to 20 V

Gate-source cut-off voltages
I_D = 20 μA; V_{DS} = 10 V; + V_{G2-S} = 4 V	$-V_{(P)G1-S}$	max.	2.7 V
I_D = 20 μA; V_{DS} = 10 V; V_{G1-S} = 0	$-V_{(P)G2-S}$	max.	2.7 V

DYNAMIC CHARACTERISTICS

Measuring conditions (common source): I_D = 7 mA; V_{DS} = 10 V; + V_{G2-S} = 4 V; T_{amb} = 25 ^{O}C

Transfer admittance at f = 1 kHz	$|y_{fs}|$	min.	9.5 mS
		typ.	12 mS
Input capacitance at gate 1; f = 1 MHz	C_{ig1-s}	typ.	1.8 pF
Input capacitance at gate 2; f = 1 MHz	C_{ig2-s}	typ.	1.0 pF
Feedback capacitance at f = 1 MHz	C_{rs}	typ.	25 fF
Output capacitance at f = 1 MHz	C_{os}	typ.	0.9 pF
Noise figure at G_S = 2 mS; B_S = B_S opt			
f = 200 MHz	F	typ.	1.6 dB
f = 800 MHz	F	typ.	2.8 dB