OKI semiconductor

MSM5259

T-52-13-07

DOT MATRIX LCD 40 DOT SEGMENT DRIVER

GENERAL DISCRIPTION

The OKI MSM5259GS is a dot matrix LCD's segment driver which is fabricated by low power CMOS metal gate technology. This LSI consists of 40-bit shift register (two 20-bit shift registers), 40-bit latch and 40-bit 4-level driver.

It converts serial data, which is received from LCD controller LSI, to parallel data and output LCD driving waveform to LCD.

Expansion of display can be easily made according to the number and structure of characters. Its 40-bit shift register consists of two 20-bit shift registers and this make it possible to allot bits efficiently according to the numbers of characters.

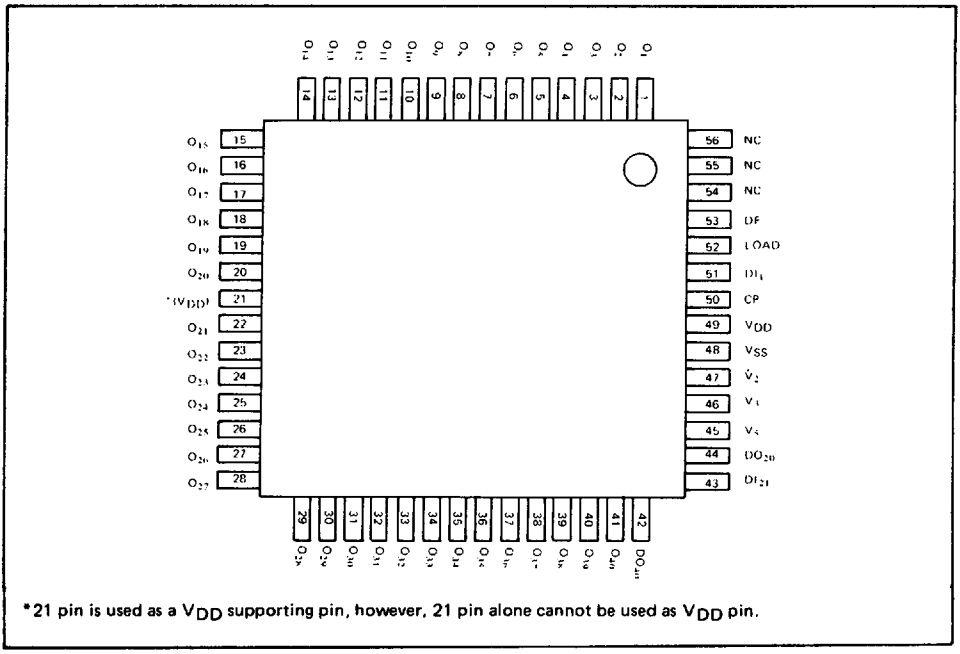
The MSM5259GS can drive a variety of LCD panel because the bias voltage, which determines the LCD driving voltage, can be optionally supplied from the external source.

FEATURES

- Supply voltage: 3.5 ~ 6.0V
- LCD driving voltage: 3.0 ~ 6.0V
- Applicable LCD duty: 1/8 ~ 1/16
- Interface with MSM6222GS (LCD controller LSI with 16-bit common driver and 40-bit segment driver)
- Bias voltage can be supplied externally
- 56 pin (s) plastic QFP (QFP56-P-910-K)
- 56 pin (s) plastic QFP (QFP56-P-910-L)
- 56 pin (s) -V plastic QFP (QFP56-P-910-VK)
- 56 pin (s) -V plastic QFP (QFP56-P-910-VL)

PIN CONFIGULATION

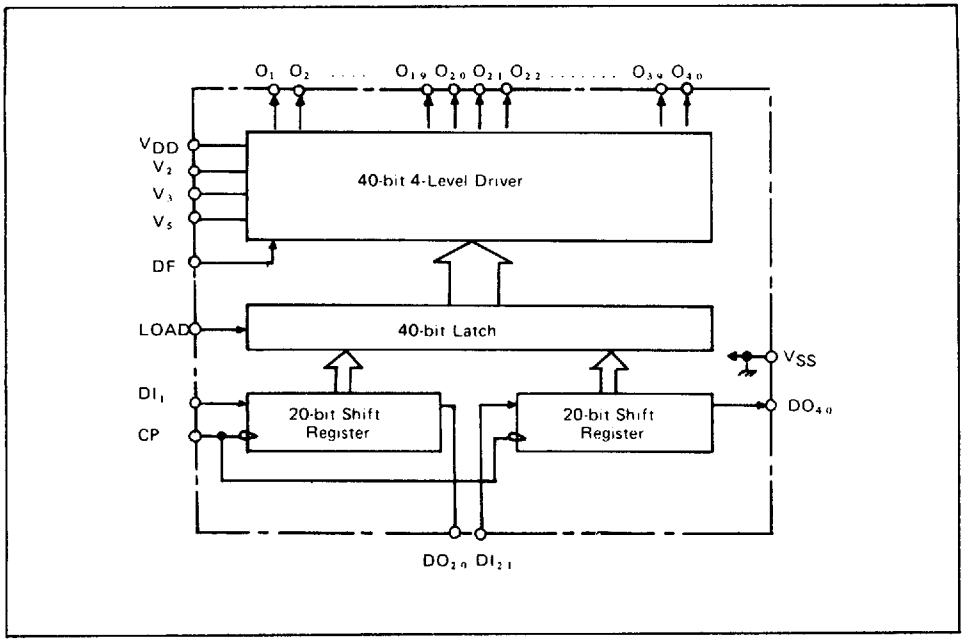
(Top view) 56 pin (s) plastic QFP



*21 pin is used as a V_{DD} supporting pin, however, 21 pin alone cannot be used as V_{DD} pin.

BLOCK DIAGRAM

T-52-13-07



ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Condition	Limits	Unit
Supply voltage (1)	V_{DD}	Ta = 25°C	−0.3 ~ +6.5	V
Supply voltage (2)	$V_{DD} - V_5$ *1		0 ~ +6.5	V
Input voltage	V_I		−0.3 ~ V_{DD} + 0.3	V
Storage temperature	T_{stg}	—	−55 ~ +150	°C

OPERATING RANGE

Parameter	Symbol	Condition	Limits	Unit
Supply voltage (1)	V_{DD}	—	3.5 ~ 6.0	V
Supply voltage (2)	$V_{DD} - V_5$ *1	—	3.0 ~ 6.0*2	V
Operating temperature	T_{op}	—	−20 ~ +85	°C

*1. $V_{DD} > V_2 \geq V_3 > V_5 \geq V_{SS}$ (Dynamic display)
$V_{SS} = V_3 > V_2 = V_5 = V_{SS}$ (Static display)

*2. To decide the LCD driving voltage, change the value of V_5. (Minimum 0V)

D.C. CHARACTERISTICS

(V_{DD} = 5 ± 10%, Ta = −20 ~ 85°C)

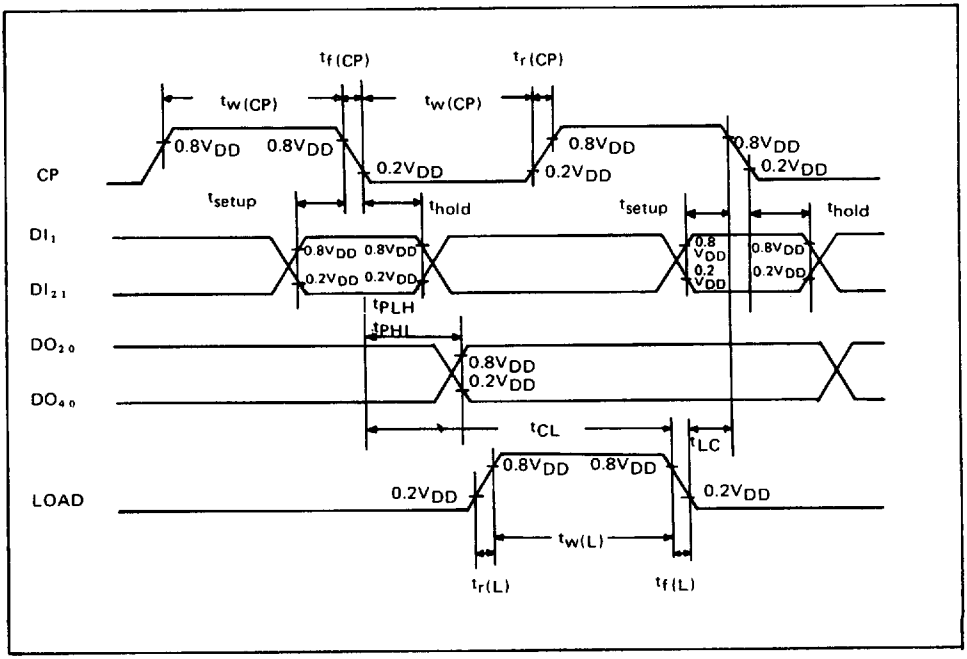
Parameter	Symbol	Condition	MIN	TYP	MAX	Unit
"H" input voltage	V_{IH}*1	—	0.8V_{DD}	–	–	V
"L" input voltage	V_{IL}*1	—	–	–	0.2V_{DD}	V
"H" input current	I_{IH}*1	$V_{IH} = V_{DD}$	–	–	1	μA
"L" input current	I_{IL}*1	V_{IL} = 0V	–	–	−1	μA
"H" output voltage	V_{OH}*2	I_O = −40μA	4.2	–	–	V
"L" output voltage	V_{OL}*2	I_O = 0.4mA	–	–	0.4	V
ON resistance	R_{ON}*3	$V_{DD} - V_5$ = 5V $\lvert V_N - V_O \rvert$ = 0.25V*4	–	–	5	kΩ
Current consumption	I_{DD}	CP = DC, No load	–	–	0.5	mA

*1. Applicable to DF, LOAD, DI_1 and DI_{21}.
*2. Applicable to DO_{20} and DO_{40}.
*3. Applicable to O_1 ~ O_{40}.
*4. $V_N = V_{DD} \sim V_5$, $V_2 = \frac{2}{3}(V_{DD} - V_5)$, $V_3 = \frac{1}{3}(V_{DD} - V_5)$

SWITCHING CHARACTERISTICS

(V_{DD} = 5 ± 10%, Ta = −20 ~ +85°C, C_L = 15pF)

Parameter	Symbol	Condition	MIN	TYP	MAX	Unit
"H", "L" propagation delay time	t_{PLH} t_{PHL}	—	–	–	250	ns
Max. clock frequency	f_{CP}	Duty = 50%	3.3	–	–	MHz
Clock pulse width	$t_{W(CP)}$	—	125	–	–	ns
Load pulse width	$t_{W(L)}$	—	125	–	–	ns
Data set-up time, DI → CP	t_{setup}	—	50	–	–	ns
CP → LOAD time	t_{CL}	—	250	–	–	ns
LOAD → CP time	t_{LC}	—	0	–	–	ns
Data hold time DI → CP	t_{hold}	—	50	–	–	ns
Clock pulse Rising/Falling time	$t_{r(CP)}$ $t_{f(CP)}$	—	–	–	50	ns
Load pulse Rising/Falling time	$t_{r(L)}$ $t_{f(L)}$	—	–	–	1	μs



PIN DESCRIPTION

T-52-13-07

- **DI_1, DI_{21}**
  The date (1st ~ 20th bit) from the LCD controller LSI is input to 20-bit shift register from DI_1. The data (21st ~ 40th bit) is input to another 20-bit shift register from DI_{21}.
  (Positive logic)

- **CP**
  Clock pulse input pin for the two 20-bit shift register. The data is shifted to 40-bit latch at the falling edge of the clock pulse. A data set up time (t_{setup}) and data hold time (t_{hold}) are required between a DI_1 signal and a clock pulse.
  Clock pulse rising time (t_r) and clock pulse falling time (t_f) should be maximum 50ns respectively.

- **DO_{20}**
  20th bit of the shift register contents is output from DO_{20}. The data which was input from DI_1 is output from this pin with 20 bits' delay, synchronized with the clock pulse. By connecting DO_{20} to DI_{21}, two 20-bit shift registers can be used as a 40-bit shift register.

- **DO_{40}**
  40th bit of the shift register contents is output from DO_{40}. The data which was input from DI_{21} is output from this pin with 20 bits' delay, synchronized with the clock pulse. By connecting DO_{40} to the next MSM5259GS's DI_1, this LSI is applicable to a wide screen LCD.
  Refer to the application circuit.

- **DF**
  Alternate signal input pin for LCD driving.

- **LOAD**
  The signal for latching the shift register contents is input from this pin.
  When LOAD pin is set at "H" level, the shift register contents are transferred to the 40-bit 4-level driver.
  When LOAD pin is set at "L" level, the last display output data (O_1 ~ O_{40}), which was transferred when LOAD pin was at "H" level, is held.

- **V_{DD}, V_{SS}**
  Supply voltage pins. V_{DD} should be 3.0 ~ 6.0V.
  V_{SS} is a ground pin (V_{SS} = OV)

- **V_{DD}, V_2, V_3, V_5**
  Bias supply voltage pins to drive the LCD. Bias voltage divided by the register is usually used as supply voltage source.
  Refer to the application circuit.

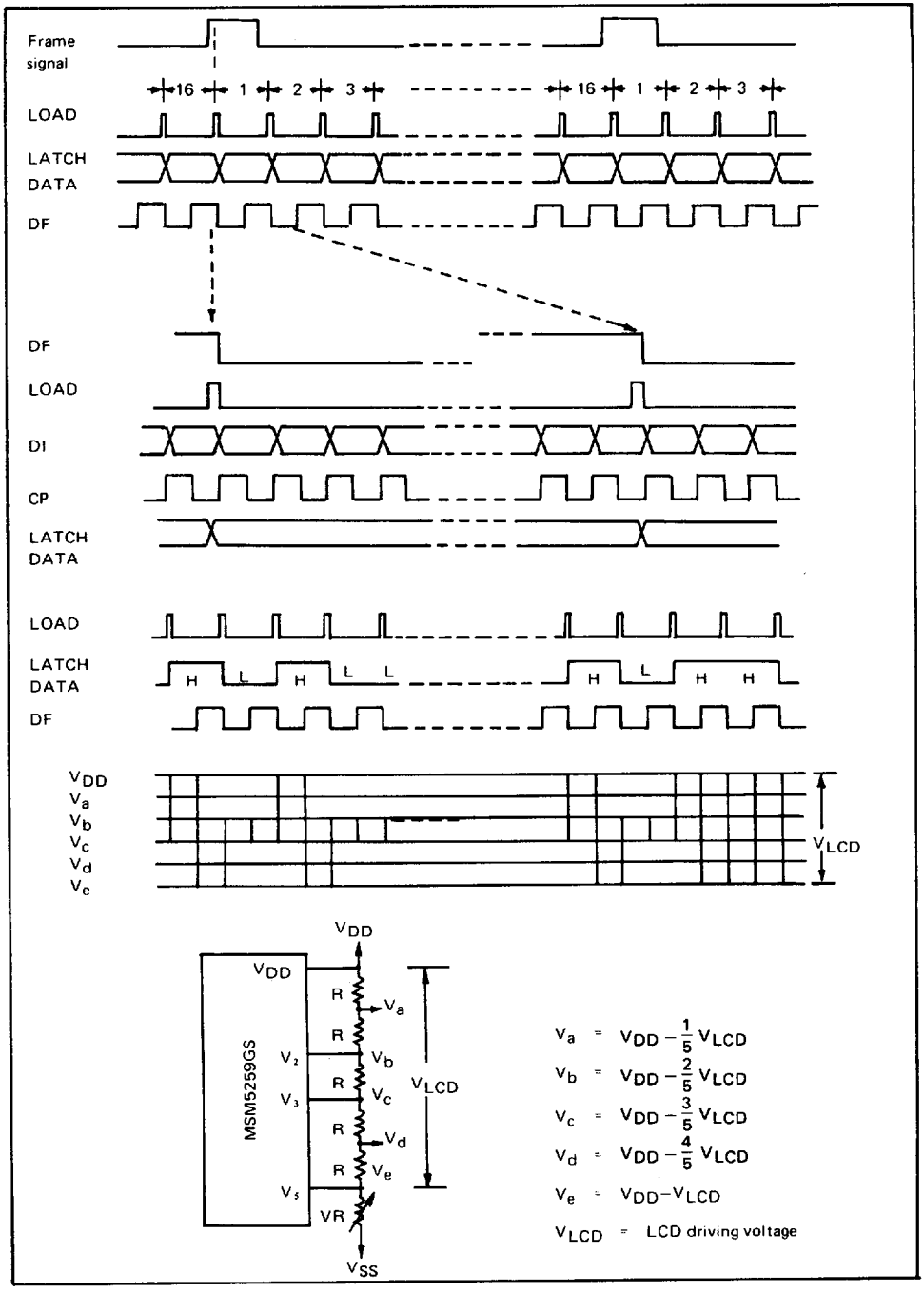
- **O_1 ~ O_{40}**
  Display data output pin which corresponds to each data bit in the latch.
  One of V_{DD}, V_2, V_3 and V_5 is selected as a display driving voltage source according to the combination of latched data level and DF signal.
  (Refer to the truth table below)

Latched data	DF	Display data output level
"H" (Selected)	H	V_5
	L	VDD
"L" (Non-selected)	H	V_3
	L	V_2

Truth Table

TIMING CHART

1/5 bias, 1/16 duty



$V_a = V_{DD} - \frac{1}{5} V_{LCD}$

$V_b = V_{DD} - \frac{2}{5} V_{LCD}$

$V_c = V_{DD} - \frac{3}{5} V_{LCD}$

$V_d = V_{DD} - \frac{4}{5} V_{LCD}$

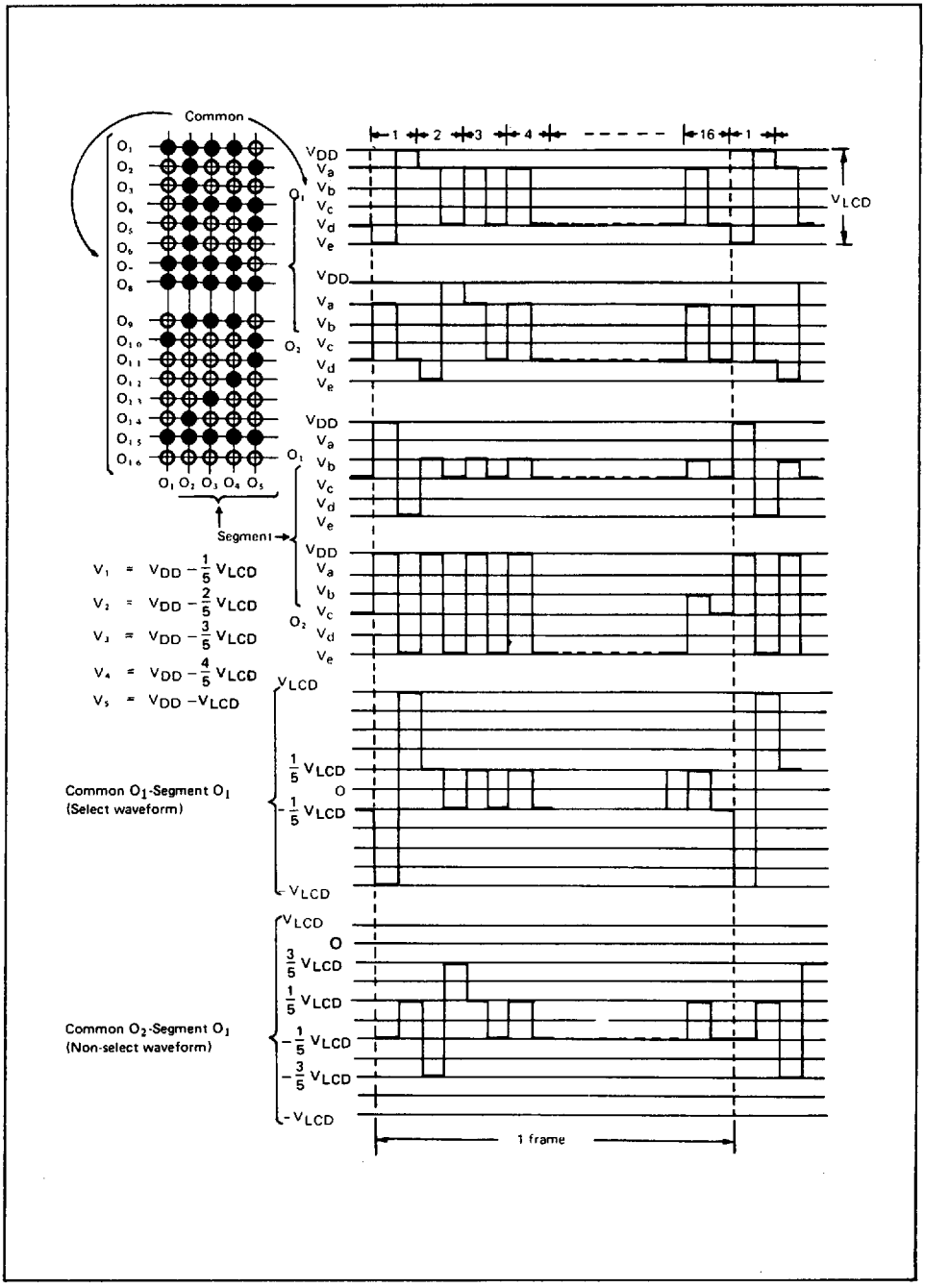
$V_e = V_{DD} - V_{LCD}$

V_{LCD} = LCD driving voltage

LCD DRIVING WAVEFORM

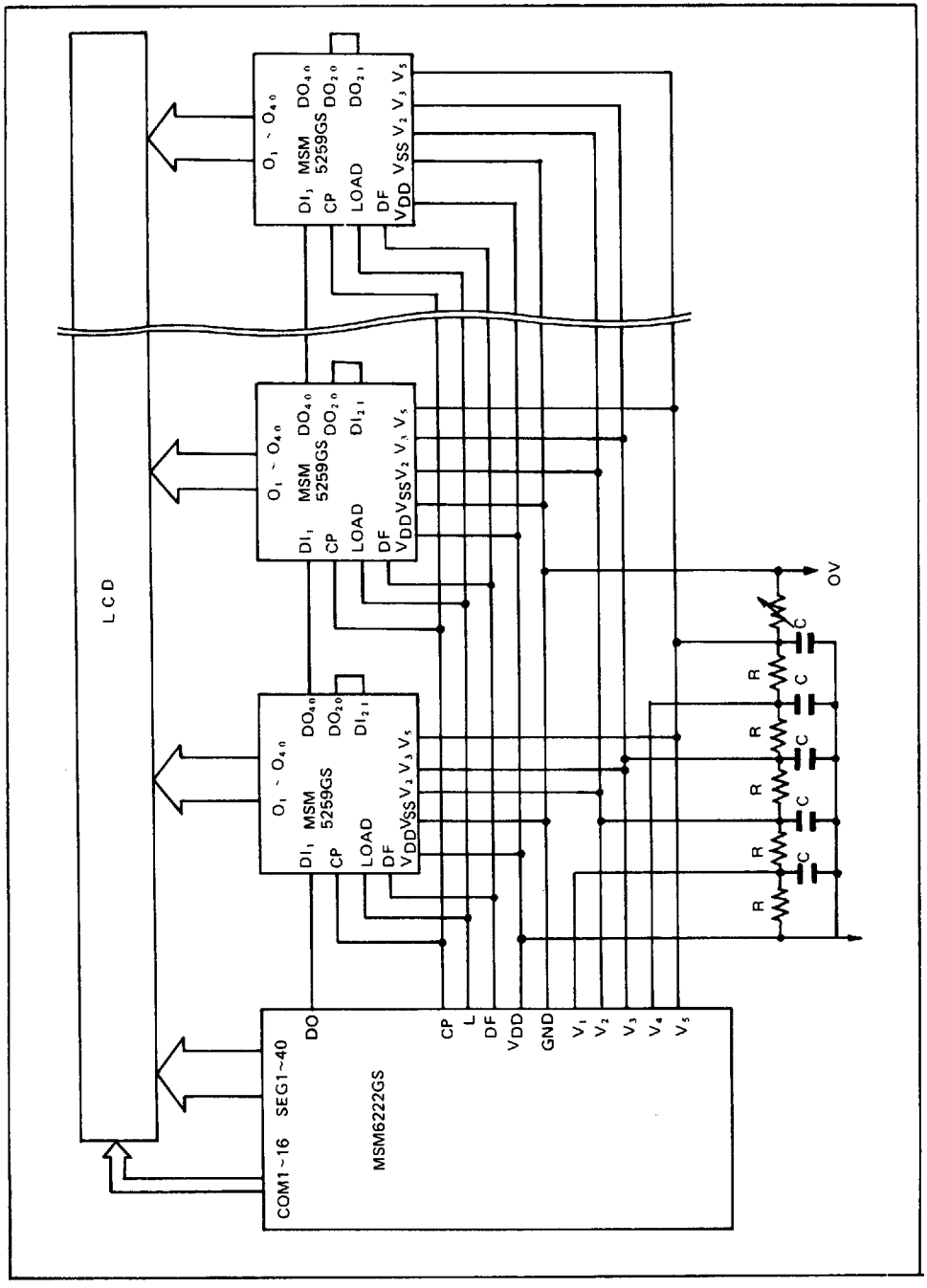
T-52-13-07

1/5 bias, 1/16 duty



TYPICAL APPLICATION CIRCUIT

(Connected to MSM6222GS LCD Controller)



TYPICAL APPLICATION CIRCUIT FOR STATIC DISPLAY

The MSM5259GS is applicable to a static LCD by setting V_2 and V_5 at ground level, connecting V_3 to V_{DD} and inputting COMMON SIGNAL to DF pin.

This sample application circuit below is the case when the MSM5259GS is applied to a 80-bit LCD panel by connecting two MSM5259GS in series.