QuadFALC

Quad E1/T1/J1 Framer and Line Interface Component for Long and Short Haul Applications

PEF 22554 HT Version 2.1

PEF 22554 E Version 2.1

Wired Communications

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Never stop thinking.

PEF 22554 HT/E

Revision History:	**2002-08-19**	DS1
Previous Version:	---	
Page	Subjects (major changes since last revision)	
	first version	

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Preface

The QuadFALC framer and line interface component is designed to fulfill all required interfacing between an analog E1/T1/J1 line and the digital PCM system highway/H.100 bus. The device contains four channels, which can be configured independently.

The digital functions as well as the analog characteristics are configured via a flexible microprocessor interface.

Organization of this Document

This Preliminary Data Sheet is organized as follows:

- **Chapter 1**, **Introduction**
  Gives a general description of the product and its family, lists the key features, and presents some typical applications.

- **Chapter 2**, **Pin Descriptions**
  Lists pin locations with associated signals, categorizes signals according to function, and describes signals.

- **Chapter 3** to **Chapter 5**, **Functional Description E1/T1/J1**
  These chapters describe the functional blocks and principle operation modes, organized into separate sections for E1 and T1/J1 operation

- **Chapter 6** and **Chapter 7**, **Operational Description E1/T1/J1**
  Shows the operation modes and how they are to be initialized (separately for E1 and T1/J1).

- **Chapter 8**, **Signaling Controller Operating Modes**
  Describes signaling controller functions for both E1 and T1/J1 operation.

- **Chapter 9** and **Chapter 10**, **E1 Registers** and **T1/J1 Registers**
  Gives a detailed description of all implemented registers and how to use them in different applications/configurations.

- **Chapter 11**, **Electrical Characteristics**
  Specifies maximum ratings, DC and AC characteristics.

- **Chapter 12**, **Package Outlines**
  Shows the mechanical values of the device package.

- **Chapter 13**, **Appendix**
  Gives an example for overvoltage protection and information about application notes and other support.

- **Chapter 14**, **Terminology**

- **Index**

Related Documentation

A detailed description of changes from version 1.3 to 2.1 is given in the PEF 22554 Version 2.1 Delta Sheet.

This document refers to the following international standards (in alphabetical/numerical order):

ANSI/EIA-656
ANSI T1.102
ANSI T1.403
AT&T PUB 43802
AT&T PUB 54016
AT&T PUB 62411
ESD Ass. Standard EOS/ESD-5.1-1993
ETSI ETS 300 011
ETSI ETS 300 166
ETSI ETS 300 233
ETSI ETS 300 324
ETSI ETS 300 347
ETSI TBR12
ETSI TBR13
FCC Part68
GR-253-CORE
GR-499-CORE
GR-1089-CORE
H.100
H-MVIP
IEEE 1149.1
ITU-T G.703
ITU-T G.704
ITU-T G.705
ITU-T G.706
ITU-T G.732
ITU-T G.735
ITU-T G.736
ITU-T G.737
ITU-T G.738
ITU-T G.739
ITU-T G.823
ITU-T G.824
ITU-T G.962
ITU-T G.963
ITU-T G.964
ITU-T I.431
ITU-Q.703
JT-G703
JT-G704
JT-G706
JT-I431
MIL-Std. 883D
TR-TSY-000009
UL 1459

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Please provide in the *subject* of your e-mail:
device name (QuadFALC), device number (PEF 22554 HT/E), device version (Version 2.1),

and in the *body* of your e-mail:
document type (Preliminary Data Sheet), issue date (2002-08-19) and document revision number
(DS1).

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1 Introduction

The QuadFALC framer and line interface component is designed to fulfill all required interfacing between four analog E1/T1/J1 lines and the digital PCM system highway, H.100/H.110 or H-MVIP bus for world market telecommunication systems.

Due to its multitude of implemented functions, it fits to a wide range of networking applications and fulfills the according international standards. An integrated signaling controller including Signaling System #7 support reduces software overhead.

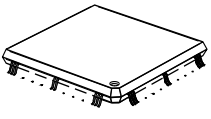
Crystal-less jitter attenuation with only one master clock source reduces the amount of required external components.

Equipped with a flexible microprocessor interface, it connects to any control processor environment. A standard boundary scan interface is provided to support board level testing. Flat pack or BGA device packaging, minimum number of external components and low power consumption lead to reduced overall system costs.

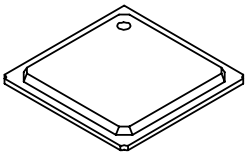
Other members of the FALC® family are the FALC®54 for short haul applications, the FALC®-LH for long haul and short haul applications as well as the FALC®56 supporting three HDLC channels on one single chip.

Version 2.1

1.1 Features



P-TQFP-144



P-BGA-160

Line Interface

- High density, generic interface for all E1/T1/J1 applications
- Four analog receive and transmit circuits for long/short haul applications
- E1 or T1/J1 mode selectable for each channel individually
- Data and clock recovery using an integrated digital phase locked loop
- Maximum line attenuation up to -43 dB at 1024 kHz (E1) and up to -36 dB at 772 kHz (T1/J1)
- Programmable transmit pulse shapes for E1 and T1/J1 pulse masks
- Programmable Line Build-Out for CSU signals according to ANSI T1. 403 and FCC68: 0 dB, -7.5 dB, -15 dB, -22.5 dB (T1/J1)
- Low transmitter output impedances for high transmit return loss
- Tristate function of the analog transmit line outputs
- Transmit line monitor protecting the device from damage
- Receive line monitor mode
- Jitter specifications of ITU-T I.431, G.703, G.736 (E1), G.823 (E1) and AT&T TR62411 (T1/J1) are met
- Crystal-less wander and jitter attenuation/compensation
- Common master clock reference for E1 and T1/J1 (any frequency within 1.02 and 20 MHz)
- Power down function per channel

Type	Package
PEF 22554 HT	P-TQFP-144
PEF 22554 E	P-BGA-160

- Support of automatic protection switching
- Dual rail or single rail digital inputs and outputs
- Unipolar NRZ or CMI for interfacing fibre optical transmission routes
- Selectable line codes (E1: HDB3, AMI/T1: B8ZS, AMI with ZCS)
- Loss of signal indication with programmable thresholds according to ITU-T G.775, ETS300233 (E1) and ANSI T1.403 (T1/J1)
- Optional data stream muting upon LOS detection
- Programmable receive slicer threshold
- Clock generator for jitter free system/transmit clocks per channel
- Local loop and remote loop for diagnostic purposes
- Low power device
- Single power supply (3.3 V) or dual power supply (3.3 V/1.8 V)
- Automatic Short Haul / Long Haul detection and adjustment by setting LIM0.EQON = 1
- 2048 kHz synchronization interface according o ITU-T G.703 Sec. 13 (E1). For more information refer to **Chapter 13.2** on **Page 455**

Frame Aligner

- Frame alignment/synthesis for 2048 kbit/s according to ITU-T G.704 (E1) and for 1544 kbit/s according to ITU-T G.704 and JT G.704 (T1/J1)
- Programmable frame formats:
  E1: Doubleframe
  CRC Multiframe
  T1: 4-Frame Multiframe (F4,FT)
  2-Frame Multiframe (F12, D3/4)
  Extended Superframe (F24, ESF)
  Remote Switch Mode (F72, SLC96)
- Selectable conditions for recover/loss of frame alignment
- CRC4 to Non-CRC4 Interworking according to ITU-T G. 706 Annex B (E1)
- Error checking via CRC4 procedures according to ITU-T G. 706 (E1)
- Error checking via CRC6 procedures according to ITU-T G. 706 and JT G.706 (T1/J1)
- Performs synchronization in ESF format according to NTT requirements (J1)
- Alarm and performance monitoring per second
  16 bit counter for CRC-, framing errors, code violations, error monitoring via E bit and SA6 bit (E1), errored blocks, PRBS bit errors
- Insertion and extraction of alarm indication signals (AIS, remote/yellow alarm,…)
- Remote Alarm generation/checking according to ITU JT-G.704 in ESF-format (J1)
- IDLE code insertion for selectable channels
- Single bit defect insertion
- Flexible system clock frequency for receiver and transmitter
- Supports programmable system data rates with independent receive/transmit shifts:
  E1: 2.048, 4.096, 8.192 and 16.384 Mbit/s (according to H.100/H.110 bus)
  T1/J1: 2.048, 4.096, 8.192, 16.384 Mbit/s and 1.544, 3.088, 6.176, 12.352 Mbit/s

- System interface multiplex mode; multiplexing of four channels into an 8.192 Mbit/s data stream and vice versa, bit- or byte-interleaved
- Elastic store for receive and transmit route clock wander and jitter compensation; controlled slip capability and slip indication
- Programmable elastic buffer size: 2 frames/1 frame/short buffer/bypass
- Provides different time slot mapping modes
- Supports fractional E1 or T1/J1 access
- Flexible transparent modes
- Programmable In-Band Loop Code detection and generation (TR62411)
- Channel loop back, line loop back or payload loop back capabilities (TR54016)
- Pseudo Random Bit Sequence (PRBS) generator and monitor (framed or unframed)
- Clear channel capabilities (T1/J1)
- Loop-timed mode

Signaling Controller

- HDLC controller
  Bit stuffing, CRC check and generation, flag generation, flag and address recognition, handling of bit oriented functions
- Supports Signaling System #7
  delimitation, alignment and error detection according to ITU-Q.703
  processing of fill in signaling units, processing of errored signaling units
- CAS/CAS-BR controller with last look capability, enhanced CAS- register access and freeze signaling indication
- DL-channel protocol for ESF format according to ANSI T1.403 specification or according to AT&T TR54016 (T1/J1)
- DL-bit access for F72 (SLC96) format (T1/J1)
- Generates periodical performance report according to ANSI T1. 403
- Provides access to serial signaling data streams
- Multiframe synchronization and synthesis according to ITU-T G.732
- Alarm insertion and detection (AIS and LOS in time slot 16)
- Transparent Mode
- FIFO buffers (64 bytes deep) for efficient transfer of data packets
- Time slot assignment
  Any combination of time slots selectable for data transfer independent of signaling mode (useful for fractional T1/J1 applications)
- Time-slot 0 S_a8...4-bit handling via FIFOs (E1)
- HDLC access to any S_a-bit combination (E1)

Microprocessor Interface

- 8/16-bit microprocessor bus interface (Intel or Motorola type)
- All registers directly accessible (byte or word access)
- Multiplexed and non-multiplexed address bus operations
- Hard/software reset options
- Extended interrupt capabilities
- One-second timer (internal or external timing reference)

General

- Boundary scan standard IEEE 1149.1
- P-TQFP-144 package; body size 20 mm × 20 mm; lead pitch 0.5 mm or
- P-BGA-160 package, body size 15 mm × 15 mm; ball pitch 1.0 mm
- 3.3 V or 3.3V/1.8V power supply
- Temperature range from -40 to +85 °C
- Typical power consumption 750 mW (four channels)

Applications

- Wireless Basestations
- E1/T1/J1 ATM Gateways, Multiplexer
- E1/T1/J1 Channel & Data Service Units (CSU, DSU)
- E1/T1/J1 Internet Access Equipment
- LAN/WAN Router
- ISDN PRI, PABX
- Digital Access Cross Connect Systems (DACS)
- SONET/SDH Add/Drop Multiplexer

1.2 Logic Symbol

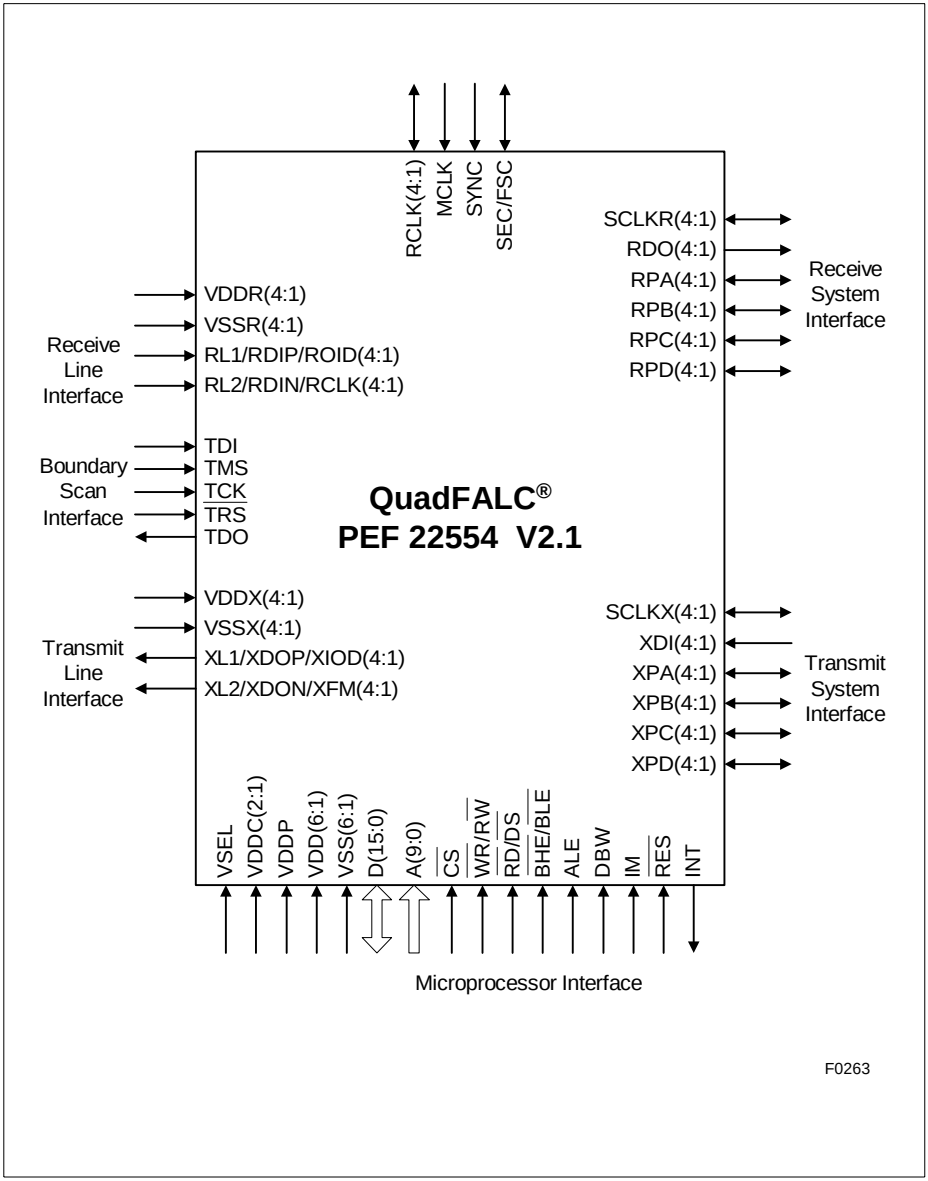


Figure 1 Logic Symbol

1.3 Typical Applications

The figures show a multiple link application for Frame Relay applications using the QuadFALC together with the 128 channel HDLC controller M128X and the Memory Timeswitch MTLS as well as an 8 channel interface to the ATM layer.

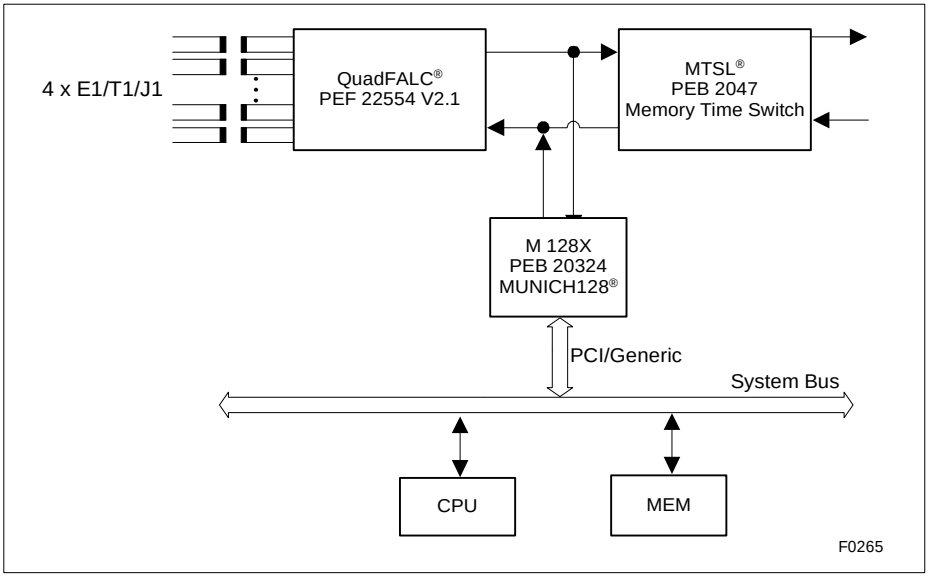


Figure 2 Multiple E1/T1/J1 Link over Frame Relay

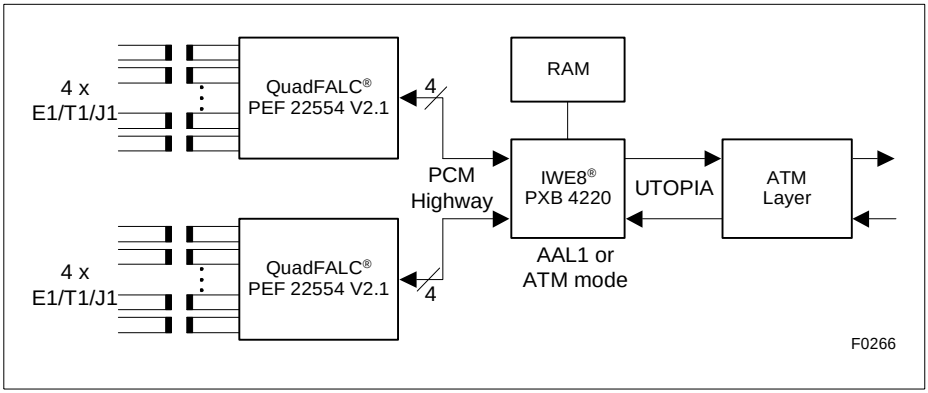


Figure 3 8 Channel E1/T1/J1 Interface to the ATM Layer

2 Pin Descriptions

2.1 Pin Diagram

(top view)

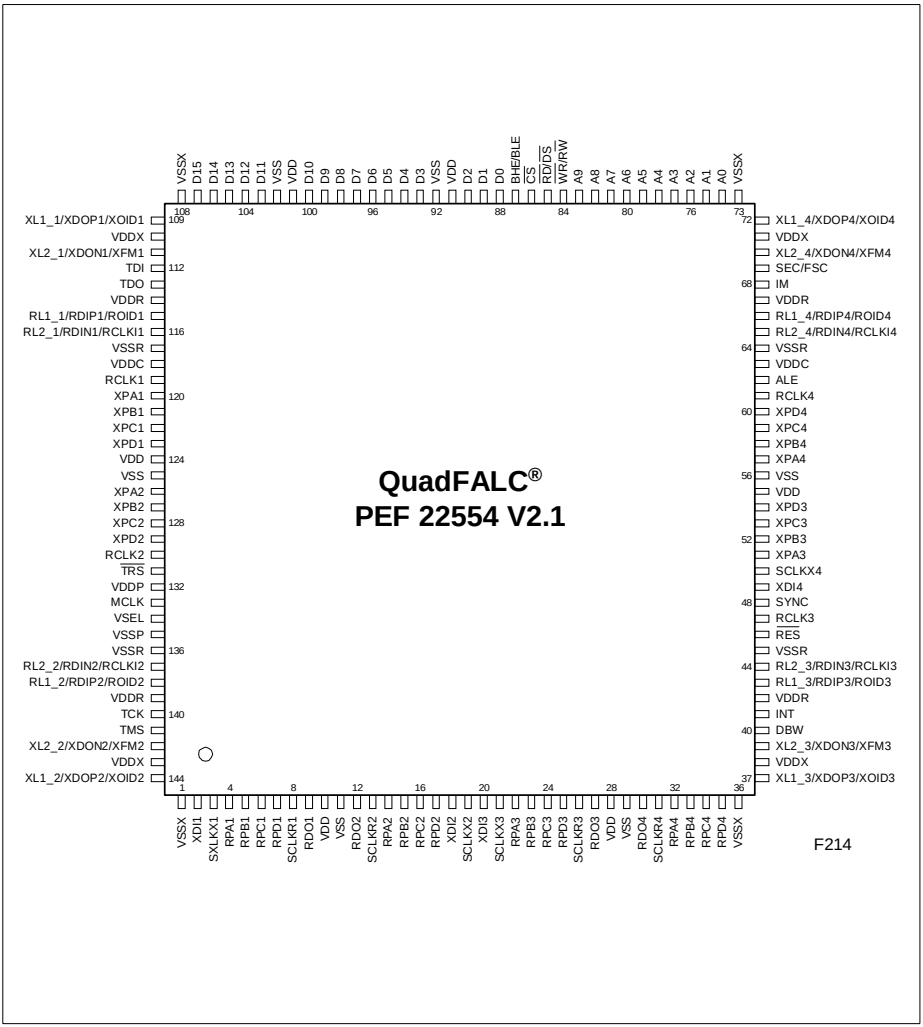


Figure 4 Pin Configuration P-TQFP-144

	1	2	3	4	5	6	7	8	9	10	11	12	13	14
A	●	XL1_2	XL2_2	VDDR	VSSR	RL1_2	RL2_2	RL2_1	RL1_1	VSSR	VDDR	XL2_1	XL1_1	
B	VSSX	VSSX	XDI1	MCLK	XPC2	$\overline{TRS}$	XPD2	VDD	XPA1	VDD	XPB1	D15	VSSX	VSSX
C	VDDX	VDDX	SCLKX 1	TCK	VSSP	VDDP	XPA2	XPB2	XPC1	VDDC	TDO	D14	VDDX	VDDX
D	RPC1	RPA1	RPB1	RPD1	TMS	VSEL	RCLK2	VSS	XPD1	RCLK1	TDI	D12	D13	D11
E	RDO1	SCLKR 1	VDD	VDD							VSS	VDD	VDD	D10
F	RDO2	VSS	SCLKR 2	RPA2							D9	D7	D8	D6
G	RPC2	RPB2	SCLKX 2	RPD2			VSS	VSS			D5	VDD	D4	D3
H	XDI3	SCLKX 3	XDI2	RPA3			VSS	VSS			D2	VSS	D0	D1
J	RPB3	RPD3	RPC3	SCLKR 3							$\overline{BHE}$/ $\overline{BLE}$	$\overline{CS}$	$\overline{WR}$/ $\overline{RW}$	$\overline{RD}$/$\overline{DS}$
K	RDO3	VSS	VDD	RDO4							A9	A8	A6	A7
L	SCLKR 4	RPB4	RPA4	DBW	RCLK3	XPA3	XPD3	XPB4	ALE	SEC/ FSC	A5	A3	A2	A4
M	VDDX	VDDX	RPC4	INT	$\overline{RES}$	SCLKX 4	VDD	VDD	XPD4	VDDC	IM	A1	VDDX	VDDX
N	VSSX	VSSX	RPD4	XDI4	XPC3	SYNC	XPB3	XPA4	RCLK4	VSS	XPC4	A0	VSSX	VSSX
P		XL1_3	XL2_3	VDDR	VSSR	RL1_3	RL2_3	RL2_4	RL1_4	VSSR	VDDR	XL2_4	XL1_4	

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Figure 5 Ball Layout P-BGA-160, Top View

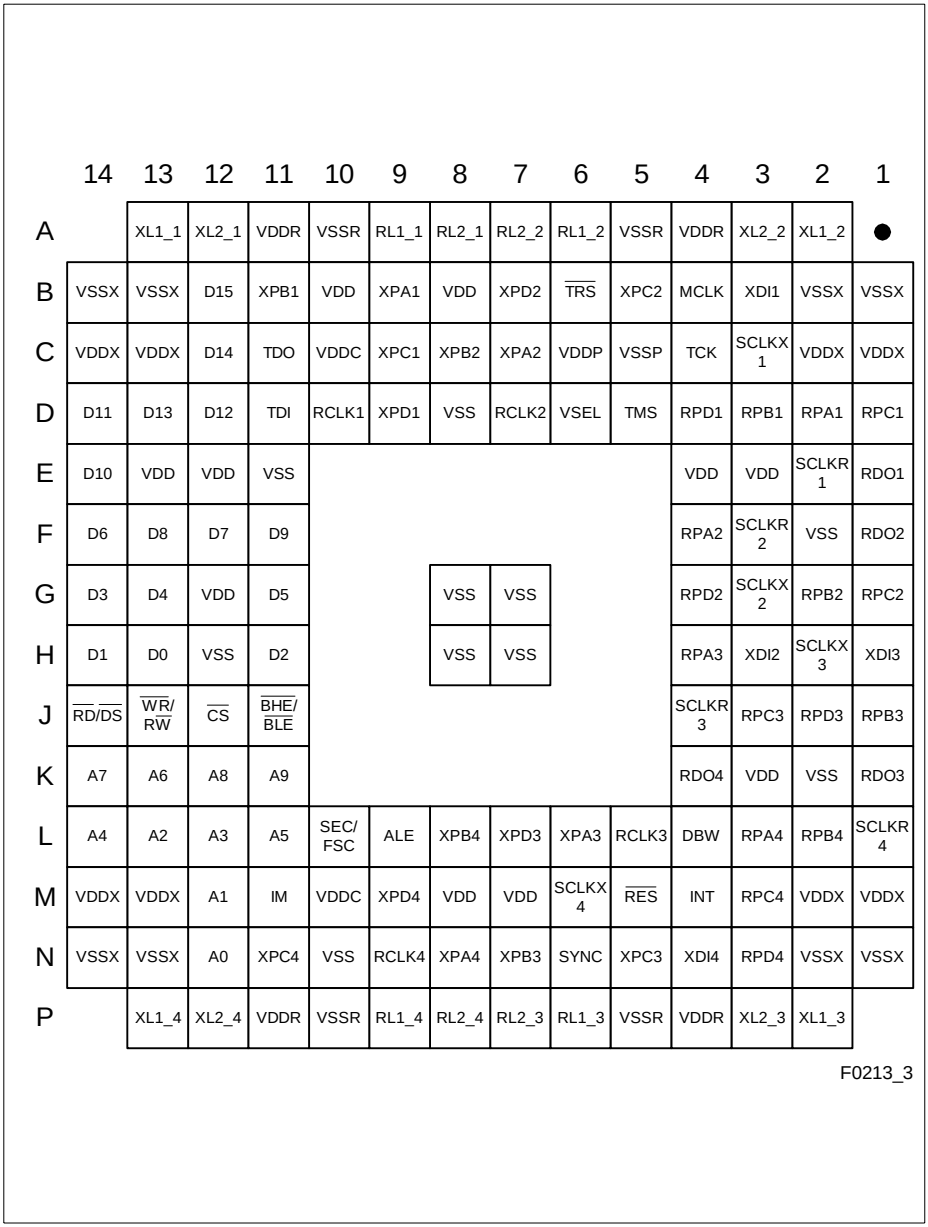


Figure 6 Ball Layout P-BGA-160, Bottom View

2.2 Pin Definitions and Functions

Table 1 Pin Definitions - Microprocessor Interface

Pin No.	Ball No.	Symbol	Input Output Supply	Function
83 82 81 80 79 78 77 76 75 74	K11 K12 K14 K13 L11 L14 L12 L13 M12 N12	A(9:0)	I + PU	**Address Bus** These inputs interface with ten bits of the system's address bus to select one of the internal registers for read or write.
107 106 105 104 103 100 99 98 97 96 95 94 93 90 89 88	B12 C12 D13 D12 D14 E14 F11 F13 F12 F14 G11 G13 G14 H11 H14 H13	D(15:0)	I/O + PU	**Data Bus** Bidirectional tristate data lines which interface with the system's data bus. Their configuration is controlled by the level of pin DBW: 8-bit mode (DBW = 0): D(7:0) are active. D(15:8) are internally pulled high. 16-bit mode (DBW = 1): D(15:0) are active. In case of byte transfers, the active half of the bus is determined by A0 and $\overline{BHE}$/$\overline{BLE}$ and the selected bus interface mode (via pin IM). The unused half is internally pulled high.

Table 1 Pin Definitions - Microprocessor Interface (cont'd)

Pin No.	Ball No.	Symbol	Input Output Supply	Function
62	L9	ALE	I + PU	**Address Latch Enable** A high on this line indicates an address on the external address/data bus. The address information provided on lines A(9:0) is internally latched with the falling edge of ALE. This function allows the QuadFALC to be connected to a multiplexed address/data bus directly. In this case, pins A(9:0) must be connected to the Data Bus pins externally. In case of demultiplexed mode this pin can be connected directly to V_{DD} or can be left open.
85	J14	$\overline{RD}$ $\overline{DS}$	I + PU	**Read Enable** (Intel bus mode) This signal indicates a read operation. When the QuadFALC is selected via $\overline{CS}$, the $\overline{RD}$ signal enables the bus drivers to output data from an internal register addressed by A(9:0) on to the Data Bus. **Data Strobe** (Motorola bus mode) This pin serves as input to control read/write operations.
84	J13	$\overline{WR}$ R$\overline{W}$	I + PU	**Write Enable** (Intel bus mode) This signal indicates a write operation. When $\overline{CS}$ is active the QuadFALC loads an internal register with data provided on the Data Bus. **Read/Write Enable** (Motorola bus mode) This signal distinguishes between read and write operation.

Table 1 Pin Definitions - Microprocessor Interface (cont'd)

Pin No.	Ball No.	Symbol	Input Output Supply	Function
40	L4	DBW	I + PU	**Data Bus Width** (Bus Interface Mode) A low signal on this input selects the 8-bit bus interface mode. A high signal on this input selects the 16-bit bus interface mode. In this case word transfer to/from the internal registers is enabled. Byte transfers are implemented by using A0 and $\overline{\text{BHE}}$/$\overline{\text{BLE}}$.
68	M11	IM	I + PU	**Interface Mode** The level at this pin defines the bus interface mode: A low signal on this input selects the Intel interface mode. A high signal on this input selects the Motorola interface mode.
86	J12	$\overline{\text{CS}}$	I + PU	**Chip Select** A low signal selects the QuadFALC for read and write operations.

Table 1 Pin Definitions - Microprocessor Interface (cont'd)

Pin No.	Ball No.	Symbol	Input Output Supply	Function
87	J11	$\overline{\text{BHE}}$	I + PU	**Bus High Enable** (Intel bus mode) If 16-bit bus interface mode is enabled, this signal indicates a data transfer on the upper byte of the data bus D(15:8). In 8-bit bus interface mode this signal has no function and should be tied to V_{DD} or left open.
		$\overline{\text{BLE}}$		**Bus Low Enable** (Motorola bus mode) If 16-bit bus interface mode is enabled, this signal indicates a data transfer on the lower byte of the data bus D(7:0). In 8-bit bus interface mode this signal has no function and should be tied to V_{DD} or left open.
41	M4	INT	O/oD	**Interrupt Request** INT serves as general interrupt request for all interrupt sources. These interrupt sources can be masked via registers IMR(4:0). Interrupt status is reported via registers GIS (Global Interrupt Status) and ISR(4:0). Output characteristics (push-pull active low/high, open drain) are determined by programming register IPC. (oD = open drain output)

Table 2 Pin Definitions - Line Interface

Pin No.	Ball No.	Symbol	Input Output Supply	Function
Line Interface Receive				
66 43 138 115	P9 P6 A6 A9	RL1 (4:1)	I (analog)	**Line Receiver 1** Analog Input from the external transformer. Selected, if LIM1.DRS = 0.
		RDIP (4:1)	I	**Receive Data Input Positive** Digital input for received dual rail PCM(+) route signal which will be latched with the internally generated receive route clock. An internal DPLL will extract the receive route clock from the incoming data pulse. The duty cycle of the received signal has to be close to 50%. The dual rail mode is selected if LIM1.DRS = 1 and FMR0.RC1 = 1. Input polarity is selected by bit RC0.RDIS (after reset: active low), line coding is selected by FMR0.RC(1:0).
		ROID (4:1)	I	**Receive Optical Interface Data** Unipolar data received from a fiber optical interface with 2048 kbit/s (E1) or 1544 kbit/s (T1/J1). Latching of data is done with the falling edge of RCLKI. Input polarity is selected by bit RC0.RDIS. The single rail mode is selected if LIM1.DRS = 1 and FMR0.RC1 = 0. If CMI coding is selected (FMR0.RC(1:0) = 01), an internal DPLL recovers clock an data; no clock signal on RCLKI is required.

Table 2 Pin Definitions - Line Interface (cont'd)

Pin No.	Ball No.	Symbol	Input Output Supply	Function
65 44, 137 116	P8 P7 A7 A8	RL2 (4:1)	I (analog)	**Line Receiver 2** Analog Input from the external transformer. Selected, if LIM1.DRS = 0.
		RDIN (4:1)	I	**Receive Data Input Negative** Input for received dual rail PCM(-) route signal which will be latched with the internally generated receive route clock. An internal DPLL will extract the receive route clock from the incoming data pulse. The duty cycle of the received signal has to be close to 50%. The dual rail mode is selected if LIM1.DRS = 1 and FMR0.RC1 = 1. Input polarity is selected by bit RC0.RDIS (after reset: active low), line coding is selected by FMR0.RC(1:0).
		RCLKI (4:1)	I	**Receive Clock Input** Receive clock input for the optical interface if LIM1.DRS = 1 and FMR0.RC(1:0) = 00. Clock frequency: 2.048 MHz (E1) or 1.544 MHz (T1/J1). RCLKI is ignored, if CMI coding is selected.

Table 2 Pin Definitions - Line Interface (cont'd)

Pin No.	Ball No.	Symbol	Input Output Supply	Function
Line Interface Transmit				
72 37 144 109	P13 P2 A2 A13	XL1 (4:1)	O (analog)	**Transmit Line 1** Analog output to the external transformer. Selected if LIM1.DRS is cleared. After reset this pin is in high impedance state until bit FMR0.XC1 is set and XPM2.XLT is cleared.
		XDOP (4:1)	O	**Transmit Data Output Positive** This digital output for transmitted dual rail PCM(+) route signals can provide - half bauded signals with 50% duty cycle (LIM0.XFB = 0) or - full bauded signals with 100% duty cycle (LIM0.XFB = 1) The data will be clocked off on the positive transitions of XCLK in both cases. Output polarity is selected by bit LIM0.XDOS (after reset: active low). The dual rail mode is selected if LIM1.DRS = 1 and FMR0.XC1 = 1. After reset this pin is in high impedance state until register LIM1.DRS is set and XPM2.XLT is cleared.

Table 2 Pin Definitions - Line Interface (cont'd)

Pin No.	Ball No.	Symbol	Input Output Supply	Function
72 37 144 109	P13 P2 A2 A13	XOID (4:1)	O	**Transmit Optical Interface Data** Unipolar data sent to a fiber optical interface with 2048 kbit/s (E1) or 1544 kbit/s (T1/J1) which will be clocked off on the positive transitions of XCLK. Clocking off data in NRZ code is done with 100% duty cycle. Data in CMI code are shifted out with 50% or 100% duty cycle on both transitions of XCLK according to the CMI coding. Output polarity is selected by bit LIM0.XDOS (after reset: data is sent active high). The single rail mode is selected if LIM1.DRS = 1 and FMR0.XC1 = 0. After reset this pin is in high impedance state until register LIM1.DRS is set and XPM2.XLT is cleared.

Table 2 Pin Definitions - Line Interface (cont'd)

Pin No.	Ball No.	Symbol	Input Output Supply	Function
70 39 142 111	P12 P3 A3 A12	XL2 (4:1)	O (analog)	**Transmit Line 2** Analog output for the external transformer. Selected if LIM1.DRS = 0. After reset this pin is in high impedance state until bit FMR0.XC1 is set and XPM2.XLT is cleared.
		XDON (4:1)	O	**Transmit Data Output Negative** This digital output for transmitted dual rail PCM(-) route signals can provide - half bauded signals with 50% duty cycle (LIM0.XFB = 0) or - full bauded signals with 100% duty cycle (LIM0.XFB = 1) The data will be clocked off on the positive transitions of XCLK in both cases. Output polarity is selected by bit LIM0.XDOS (after reset: active low). The dual rail mode is selected if LIM1.DRS = 1 and FMR0.XC1 = 1. After reset this pin is in high impedance state until register LIM1.DRS is set and XPM2.XLT is cleared.
		XFM (4:1)	O	**Transmit Frame Marker** This digital output marks the first bit of every frame transmitted on port XDOP. This function is only available in the optical interface mode (LIM1.DRS = 1 and FMR0.XC1 = 0). The data will be clocked off on the positive transitions of XCLK. After reset this pin is in high impedance state until register LIM1.DRS is set to one. In remote loop configuration the XFM marker is not valid. After reset this pin is in high impedance state until register LIM1.DRS is set and XPM2.XLT is cleared.

Table 3 Pin Definitions - Clock Generation

Pin No.	Ball No.	Symbol	Input Output Supply	Function
133	B4	MCLK	I	**Master Clock** A reference clock of better than ± 32 ppm accuracy in the range of 1.02 to 20 MHz must be provided at this pin. The QuadFALC will internally derive all necessary clocks from this master. (see registers GCM(8:1)).
48	N6	SYNC	I + PU	**Clock Synchronization of DCO-R** If a clock is detected on pin SYNC the DCO-R circuitry of the QuadFALC synchronizes to this 1.544/2.048-MHz clock (see LIM0.MAS, CMR1.DCS and CMR2.DCF). Additionally in master mode the QuadFALC is able to synchronize to an 8-kHz reference clock (IPC.SSYF = 1). If not connected, an internal pullup transistor ensures high input level.

Table 3 Pin Definitions - Clock Generation (cont'd)

Pin No.	Ball No.	Symbol	Input Output Supply	Function
69	L10	SEC	I + PU	**Second Timer Input** A pulse with logical high level for at least two 2.048-MHz cycles will trigger the internal second timer. After reset this pin is configured to be an input. If not connected, an internal pullup transistor ensures high input level (see register GPC1).
			O	**Second Timer Output** Activated high every second for two 2.048-MHz clock cycles.
		FSC	O	**8-kHz frame synchronization pulse** The synchronization pulse is active high/low for one 2.048-MHz cycle (pulse width = 488 ns).

Table 3 Pin Definitions - Clock Generation (cont'd)

Pin No.	Ball No.	Symbol	Input Output Supply	Function
61 47 130 119	N9 L5 D7 D10	RCLK (4:1)	O + PU	**Receive Clock** After reset this port is configured to be internally pulled up weakly. Setting of bit PC5.CRP will switch this port to be an active output. CMR1.RS(1:0) = 00: Receive clock extracted from the incoming data pulses. The clock frequency is 2.048 MHz (E1) or 1.544 MHz (T1/J1). In case of loss of signal (LOS) the RCLK is derived from the clock that is provided on MCLK. CMR1.RS(1:0) = 01: Receive clock extracted from the incoming data pulses. The clock frequency is 2.048 MHz (E1) or 1.544 MHz (T1/J1). RCLK is set high in case of loss of signal (indicated by FRS0.LOS = 1). CMR1.RS(1:0) = 10: Dejittered clock generated by the internal DCO-R circuit. The clock frequency is 2.048 MHz (E1 or T1/J1 and SIC2.SSC2 = 0) or 1.544 MHz (T1/J1 and SIC2.SSC2 = 1). CMR1.RS(1:0) = 11: Dejittered clock generated by the internal DCO-R circuit. The clock frequency is 8.192 MHz (E1 or T1/J1 and SIC2.SSC2 = 0) or 6.176 MHz (T1/J1 and SIC2.SSC2 = 1). Using GPC1.R1S(1:0), one of the four extracted route clocks RCLK(4:1) can be output on pin RCLK1.

Table 4 Pin Definitions - System Interface

Pin No.	Ball No.	Symbol	Input Output Supply	Function
System Interface Receive				
30 27 12 9	K4 K1 F1 E1	RDO (4:1)	O	**Receive Data Out** Received data which is sent to the system highway. Clocking off data is done with the rising or falling edge (SIC3.RESR) of SCLKR(4:1) or RCLK(4:1), if the receive elastic store is bypassed. The delay between the beginning of time slot 0 and the initial edge of SCLKR(4:1) (after $\overline{\text{SYPR}}$ goes active) is determined by the values of registers RC1 and RC0. If received data is shifted out with higher (more than 2.048/1.544 Mbit/s) data rates, the active channel phase is defined by bits SIC2.SICS(2:0). During inactive channel phases RDO is cleared (driven to low level, not tristate). In system interface multiplex mode all four received data streams are merged into a single data stream (byte- or bit-interleaved, selected by RDO1).

Table 4 Pin Definitions - System Interface (cont'd)

Pin No.	Ball No.	Symbol	Input Output Supply	Function
31 26 13 8	L1 J4 F3 E2	SCLKR (4:1)	I/O + PU	**System Clock Receive** Working clock for the receive system interface with a frequency of 16.384/8.192/4.096/2.048 MHz in E1 mode and 16.384/8.192/4.096/2.048 MHz (SIC2.SSC2 = 0) or 12.352/6.176/3.088/1.544 MHz (SIC2.SSC2 = 1) in T1/J1 mode. If the receive elastic store is bypassed, the clock supplied on this pin is ignored. If SCLKR is configured to be an output, the internal working clock of the receive system interface sourced by DCO-R or RCLK is output. In system interface multiplex mode a clock has to be provided on SCLKR1, which is common for all four receive system interfaces. Possible clock frequencies are 16.384 or 8.192 in E1 mode and 16.384, 12.352, 8.192 or 6.176 in T1/J1 mode.

Table 4 Pin Definitions - System Interface (cont'd)

Pin No.	Ball No.	Symbol	Input Output Supply	Function
4 14 22 32 5 15 23 33 6 16 24 34	D2 D3 D1 D4 F4 G2 G1 G4 H4 J1 J3 J2	RPA1 RPB1 RPC1 RPD1 RPA2 RPB2 RPC2 RPD2 RPA3 RPB3 RPC3 RPD3	I/O + PU	**Receive Multifunction Port A to D** Depending on programming of bits PC(4:1).RPC(2:0) these multifunction ports carry information to the system interface or from the system to the QuadFALC. After reset these ports are configured to be inputs. With the selection of the appropriate pin function, the corresponding input/output configuration is achieved automatically. Depending on bit SIC3.RESR latching/transmission of data is done with the rising or falling edge of SCLKR. If not connected, an internal pullup transistor ensures a 'high' input level.
7 17 25 35	L3 L2 M3 N3	RPA4 RPB4 RPC4 RPD4	I + PU	**Synchronous Pulse Receive ($\overline{\text{SYPR}}$)** PC(4:1).RPC(2:0) = 000 Defines the beginning of time slot 0 at system highway port RDO together with the values of registers RC(1:0). Only one multifunction port may be selected as $\overline{\text{SYPR}}$ input. After reset, $\overline{\text{SYPR}}$ of port A is used, the other lines are ignored. In system interface multiplex mode, $\overline{\text{SYPR}}$ has to be provided at port RPA1 for all four channels and defines the beginning of time slot 0 on port RDO1/RSIG1. The pulse cycle is an integer multiple of 125 µs.

Table 4 Pin Definitions - System Interface (cont'd)

Pin No.	Ball No.	Symbol	Input Output Supply	Function
4 14 22 32 5 15 23 33 6 16 24 34 7 17 25 35	D2 D3 D1 D4 F4 G2 G1 G4 H4 J1 J3 J2 L3 L2 M3 N3	RPA1 RPB1 RPC1 RPD1 RPA2 RPB2 RPC2 RPD2 RPA3 RPB3 RPC3 RPD3 RPA4 RPB4 RPC4 RPD4	O	**Receive Frame Marker (RFM)** PC(4:1).RPC(2:0) = 001 CMR2.IRSP = 0: The receive frame marker can be *active high* for a 2.048-MHz (E1) or 1.544-MHz (T1/J1) period during any bit position of the current frame. It is clocked off with the rising or falling edge of SCLKR or RCLK, depending on SIC3.RESR. Offset programming is done by using registers RC(1:0). CMR2.IRSP = 1: Frame synchronization pulse generated by the DCO-R circuitry internally. This pulse is *active low* for a 2.048-MHz (E1) or 1.544-MHz (T1/J1) period.
			O	**Receive Multiframe Begin (RMFB)** PC(4:1).RPC(2:0) = 010 In E1 mode RMFB marks the beginning of every received multiframe (RDO). Optionally the time slot 16 CAS multiframe begin can be marked (SIC3.CASMF). Active high for one 2048 kbit/s period. In T1/J1 mode the function depends on bit XC0.MFBS: MFBS = 1: RMFB marks the beginning of every received multiframe (RDO). MFBS = 0: RMFB marks the beginning of every received superframe. Additional pulses are provided every 12 frames when using ESF/F24 or F72 format.

Table 4 Pin Definitions - System Interface (cont'd)

Pin No.	Ball No.	Symbol	Input Output Supply	Function
4 14 22 32 5 15 23 33 6 16 24 34	D2 D3 D1 D4 F4 G2 G1 G4 H4 J1 J3 J2	RPA1 RPB1 RPC1 RPD1 RPA2 RPB2 RPC2 RPD2 RPA3 RPB3 RPC3 RPD3	O	**Receive Signaling Marker (RSIGM)** PC(4:1).RPC(2:0) = 011 E1: Marks the time slots which are defined by register RTR(4:1) of every received frame at port RDO. T1/J1: Marks the time slots which are defined by register RTR(4:1) of every received frame on port RDO, if CAS-BR is *not* used. When using the CAS-BR signaling scheme, the robbed bit of each channel every six frames is marked, if it is enabled by XC0.BRM = 1.
7 17 25 35	L3 L2 M3 N3	RPA4 RPB4 RPC4 RPD4	O	**Receive Signaling Data (RSIG)** PC(4:1).RPC(2:0) = 100 The received CAS signaling data is sourced by this pin. Time slots on RSIG correlate directly to the time slot assignment on RDO. In system interface multiplex mode all four received signaling data streams are merged into a single data stream which is transmitted on RPB1 (bit- or byte-interleaved).
			O	**Data Link Bit Receive (DLR)** PC(4:1).RPC(2:0) = 101 E1: Marks the SA(8:4) bits within the data stream on RDO. The SA(8:4) bit positions in time slot 0 of every frame not containing the frame alignment signal are selected by register XC0. T1/J1: Marks the DL-bit position within the data stream on RDO.

Table 4 Pin Definitions - System Interface (cont'd)

Pin No.	Ball No.	Symbol	Input Output Supply	Function
4 14 22 32 5 15 23 33	D2 D3 D1 D4 F4 G2 G1 G4	RPA1 RPB1 RPC1 RPD1 RPA2 RPB2 RPC2 RPD2	O	**Freeze Signaling (FREEZE)** PC(4:1).RPC(2:0) = 110 The freeze signaling status is set active high by detecting a loss of signal alarm, a loss of CAS frame alignment or a receive slip (positive or negative). It will stay high for at least one complete multiframe after the alarm disappears. Setting SIC2.FFS enforces a high on pin FREEZE.
6 16 24 34 7 17 25 35	H4 J1 J3 J2 L3 L2 M3 N3	RPA3 RPB3 RPC3 RPD3 RPA4 RPB4 RPC4 RPD4	O	**Frame Synchronous Pulse ($\overline{\text{RFSP}}$)** PC(4:1).RPC(2:0) = 111 Active low framing pulse derived from the received PCM route signal. During loss of synchronization (bit FRS0.LFA = 1), this pulse is suppressed (not influenced during alarm simulation). Pulse frequency: 8 kHz Pulse width: 488 ns (E1) or 648 ns (T1/J1).
System Interface Transmit				
49 20 18 2	N4 H1 H3 B3	XDI (4:0)	I	**Transmit Data In** Transmit data received from the system highway. Latching of data is done with rising or falling transitions of SCLKX according to bit SIC3.RESX. The delay between the beginning of time slot 0 and the initial edge of SCLKX (after $\overline{\text{SYPX}}$ goes active) is determined by the registers XC(1:0). In higher (more than 1.544/2.048 Mbit/s) data rates sampling of data is defined by bits SIC2.SICS(2:0).

Table 4 Pin Definitions - System Interface (cont'd)

Pin No.	Ball No.	Symbol	Input Output Supply	Function
50 21 19 3	M6 H2 G3 C3	SCLKX (4:1)	I/O + PU	**System Clock Transmit** Working clock for the transmit system interface with a frequency of 16.384/8.192/4.096/2.048 in E1 mode and 16.384/8.192/4.096/2.048 MHz (SIC2.SSC2 = 0) or 12.352/6.176/3.088/1.544 MHz (SIC2.SSC2 = 1) in T1/J1 mode.
120 126 51 57 121 127 52 58 122 128 53 59	B9 B11 C9 D9 C7 C8 B5 B7 L6 N7 N5 L7	XPA1 XPB1 XPC1 XPD1 XPA2 XPB2 XPC2 XPD2 XPA3 XPB3 XPC3 XPD3	I/O + PU	**Transmit Multifunction Port A to D** Depending on programming of bits PC(4:1).XPC(3:0) these multifunction ports carry information to the system interface or from the system to the QuadFALC. After reset the ports are configured to be inputs. With the selection of the appropriate pin function, the corresponding input/output configuration is achieved automatically. Depending on bit SIC3.RESX latching/transmission of data is done with the rising or falling edge of SCLKX. If not connected, an internal pullup transistor ensures a 'high' input level.
123 129 54 60	N8 L8 N11 M9	XPA4 XPB4 XPC4 XPD4	I + PU	**Synchronous Pulse Transmit ($\overline{\text{SYPX}}$)** PC(4:1).XPC(3:0) = 0000 Defines the beginning of time slot 0 at system highway port XDI together with the values of registers XC(1:0). In system interface multiplex mode $\overline{\text{SYPX}}$ has to be provided on port XPA1 for all four channels and defines the beginning of time slot 0 on port XDI1/XSIG1. The pulse cycle is an integer multiple of 125 µs.

Table 4 Pin Definitions - System Interface (cont'd)

Pin No.	Ball No.	Symbol	Input Output Supply	Function
120 126 51 57 121 127 52 58 122 128 53 59 123 129 54 60	B9 B11 C9 D9 C7 C8 B5 B7 L6 N7 N5 L7 N8 L8 N11 M9	XPA1 XPB1 XPC1 XPD1 XPA2 XPB2 XPC2 XPD2 XPA3 XPB3 XPC3 XPD3 XPA4 XPB4 XPC4 XPD4	I + PU	**Transmit Multiframe Synchronization (XMFS)** PC(4:1).XPC(3:0) = 0001 This port defines the frame and multiframe begin on the transmit system interface ports XDI and XSIG. Depending on PC5.CXMFS the signal on XMFS is active high or low. In system interface multiplex mode XMFS has to be provided on port XPA1. *Note: A new multiframe position has settled at least one multiframe after pulse XMFS has been supplied.*
			I + PU	**Transmit Signaling Data (XSIG)** PC(4:1).XPC(3:0) = 0010 Input for transmit signaling data received from the signaling highway. Optionally (SIC3.TTRF = 1) sampling of XSIG data is controlled by the active high XSIGM marker. At higher data rates sampling of data is defined by bits SIC2.SICS(2:0). In system interface multiplex mode all four signaling data streams are received on XPB1.
			I + PU	**Transmit Clock (TCLK)** PC(4:1).XPC(3:0) = 0011 A 2.048/8.192-MHz (E1) or 1.544/6.176-MHz (T1/J1) clock has to be sourced by the system if the internal generated transmit clock (generated by DCO-X) shall not be used. Optionally this input is used as a synchronization clock for the DCO-X circuitry with a frequency of 2.048 (E1) or 1.544 MHz (T1/J1).

Table 4 Pin Definitions - System Interface (cont'd)

Pin No.	Ball No.	Symbol	Input Output Supply	Function
120 126 51 57 121 127 52 58 122 128 53 59 123 129 54 60	B9 B11 C9 D9 C7 C8 B5 B7 L6 N7 N5 L7 N8 L8 N11 M9	XPA1 XPB1 XPC1 XPD1 XPA2 XPB2 XPC2 XPD2 XPA3 XPB3 XPC3 XPD3 XPA4 XPB4 XPC4 XPD4	O	**Transmit Multiframe Begin (XMFB)** PC(4:1).XPC(3:0) = 0100 XMFB marks the beginning of every transmitted multiframe on XDI. The signal is active high for one 2048- or 1.544-kbit/s period.
			O	**Transmit Signaling Marker (XSIGM)** PC(4:1).XPC(3:0) = 0101 E1: Marks the transmit time slots of every frame which are defined by register TTR(4:1) transmitted on port XDI. T1/J1: Marks the transmit time slots of every frame which are defined by register TTR(4:1) transmitted on port XDI (if not CAS-BR is used). When using the CAS-BR signaling scheme the robbed bit of each channel every six frames is marked.
			O	**Data Link Bit Transmit (DLX)** PC(4:1).XPC(3:0) = 0110 E1: Marks the S_A(8:4) bits within the data stream on XDI. The S_A(8:4) bit positions in time slot 0 of every frame not containing the frame alignment signal are selected by register XC0.SA(8:4)E. T1/J1: This output provides a 4-kHz signal which marks the DL-bit position within the data stream on XDI (in ESF mode only).

Table 4 Pin Definitions - System Interface (cont'd)

Pin No.	Ball No.	Symbol	Input Output Supply	Function
120 126 51 57 121 127 52 58 122 128 53 59 123 129 54 60	B9 B11 C9 D9 C7 C8 B5 B7 L6 N7 N5 L7 N8 L8 N11 M9	XPA1 XPB1 XPC1 XPD1 XPA2 XPB2 XPC2 XPD2 XPA3 XPB3 XPC3 XPD3 XPA4 XPB4 XPC4 XPD4	O I + PU	**Transmit Clock (XCLK)** PC(4:1).XPC(3:0) = 0111 Transmit line clock of 2.048 MHz (E1) or 1.544 MHz (T1/J1) derived from SCLKX/R, RCLK or generated internally by DCO circuitries. **Transmit Line Tristate (XLT)** PC(4:1).XPC(3:0) = 1000 A high level on this port sets the transmit lines XL1/2 or XDOP/N into tristate mode. This pin function is logically ored with register XPM2.XLT.

Table 5 Pin Definitions - Miscellaneous

Pin No.	Ball No.	Symbol	Input Output Supply	Function
Power Supply				
42 67 114 139	P4 P11 A11 A4	V_{DDR}	S	**Positive Power Supply** for the analog receiver (3.3 V)
45 64 117 136	P5 P10 A10 A5	V_{SSR}	S	**Power Supply Ground** for the analog receiver
38 71 110 143	M1 M2 M13 M14 C13 C14 C1 C2	V_{DDX}	S	**Positive Power Supply** for the analog transmitter (3.3 V)
1 36 73 108	B1 B2 N1 N2 N13 N14 B13 B14	V_{SSX}	S	**Power Supply Ground** for the analog transmitter
11 29 56 92 102 125 135	F2 K2 N10 H12 E11 D8 C5 G7 G8 H7 H8	V_{SS}	S	**Power Supply Ground** for digital sub circuits (0 V) For correct operation, all seven pins have to be connected to ground.

Table 5 Pin Definitions - Miscellaneous (cont'd)

Pin No.	Ball No.	Symbol	Input Output Supply	Function
10 28 55 91 101	E3 E4 K3 M7 M8 G12 E12 E13 B8	V_{DD}	S	**Positive Power Supply** for the digital pads (3.3 V) For correct operation, all seven pins have to be connected to positive power supply.
135	C5	V_{SSP}	S	**Power Supply Ground** for the analog PLL (0 V)
124 132	B10 C6	V_{DDP}	S	**Positive Power Supply** for the analog PLL (3.3 V)
63 118	M10 C10	V_{DDC}	S	**Positive Power Supply** for the digital core (1.8 V) This pin can either be a positive power supply input or output depending on the VSEL input condition. If the VSEL pin is connected to VSS, these pins are inputs and must both be connected to the same 1.8V power supply and require decoupling. If the VSEL pin is connected to VDD (3.3 V), these pins will both be 1.8 V power supply outputs and must be decoupled to VSS. ***Attention: These pins must not be used to supply external devices.***
Power Supply Configuration				
134	D6	VSEL	I + PU	**Voltage Select** Enables the internal voltage regulator for 3.3 V-only operation mode if connected to VDD (recommended) or left open. Disables the internal voltage regulator for dual power supply mode if connected to VSS.

Table 5 Pin Definitions - Miscellaneous (cont'd)

Pin No.	Ball No.	Symbol	Input Output Supply	Function
Device Reset				
46	M5	$\overline{RES}$	I	**Reset** A low signal on this pin forces the QuadFALC into reset state. During reset the QuadFALC needs an active clock on pin MCLK. During reset all bidirectional output stages are in input mode, if signal $\overline{RD}$ is "high".
Boundary Scan/Joint Test Access Group (JTAG)				
131		$\overline{TRS}$	I + PU	**Test Reset** for Boundary Scan (active low). If not connected, an internal pullup transistor ensures high input level. If the JTAG boundary scan is not used, this pin must be connected to $\overline{RES}$ or V_{SS}.
112		TDI	I + PU	**Test Data Input** for Boundary Scan If not connected an internal pullup transistor ensures high input level.
141		TMS	I + PU	**Test Mode Select** for Boundary Scan If not connected an internal pullup transistor ensures high input level.
140		TCK	I + PU	**Test Clock** for Boundary Scan If not connected an internal pullup transistor ensures high input level.
113		TDO	O	**Test Data Output** for Boundary Scan

Note: oD = open drain output
PU = input or input/output comprising an internal pullup device
To override the internal pullup by an external pulldown, a resistor value of 22 kΩ is recommended.

The pullup devices are activated during reset, this means their state is undefined until the reset signal has been applied.

Unused pins containing pullups can be left open. Unused receive channels have to be connected to a fixed level (V_{DDR} or V_{SSR}).

3 Functional Description E1/T1/J1

3.1 Functional Overview

The QuadFALC device contains analog and digital function blocks, which are configured and controlled by an external microprocessor or micro controller.

The main interfaces are

- Receive and Transmit Line Interface
- PCM System Highway Interface/H.100/H.110 bus (including channel multiplex mode)
- Microprocessor Interface
- Boundary Scan Interface

as well as several control lines for reset and clocking purpose.

The main internal functional blocks are

- Analog line receiver with equalizer network and clock/data recovery
- Analog line driver with programmable pulse shaper and line build out
- Central clock generation module
- Elastic buffers for receive and transmit direction
- Receive Framer, receive line decoding, alarm detection, PRBS and performance monitoring
- Transmit framer, receive line encoding, alarm and PRBS generation
- Receive jitter attenuator
- Transmit jitter attenuator
- HDLC controller (including SS7 and BOM support) and CAS signaling controller
- Test functions (loop switching local - remote - payload - single channel)
- Register access interface
- Boundary scan control

3.2 Block Diagram

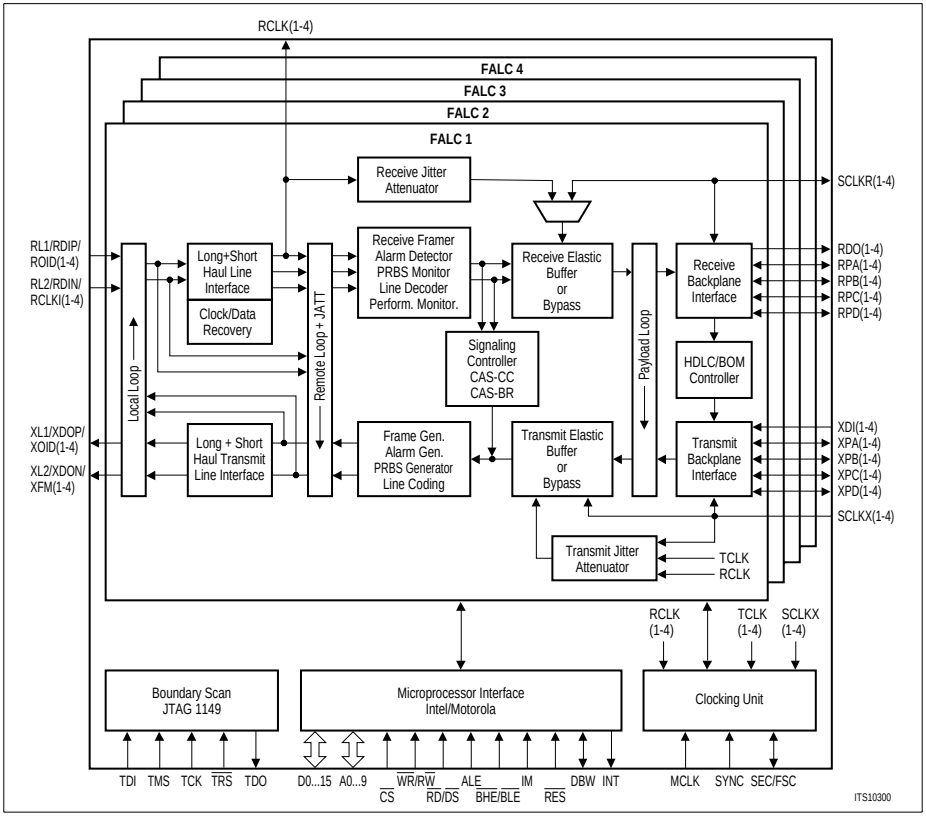


Figure 7 Block Diagram

3.3 Power Supply

3.3.1 Power Supply Options

The device requires two supply voltages, 3.3 V and 1.8 V. For compatibility reasons, it is possible to operate the device off a single 3.3 V supply, with the 1.8 V supply being generated internally using an on-chip regulator. In order to minimize power consumption, it is recommended to operate the device using separate external 3.3 V and 1.8 V supplies. Please note that the 1.8 V supply requires de-coupling whether generated on-chip or externally. Supply voltage selection is done by using pin VSEL.

See **Figure 8** and **Figure 9**.

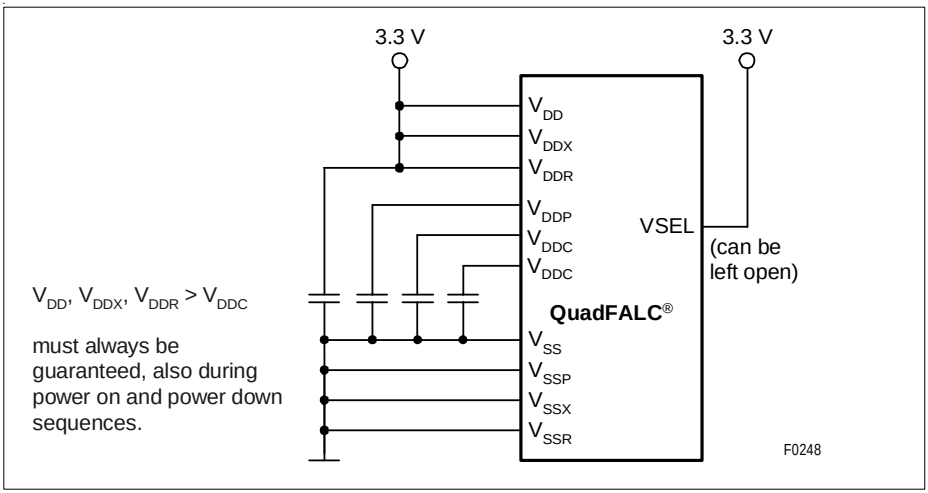


Figure 8 Single Voltage Supply

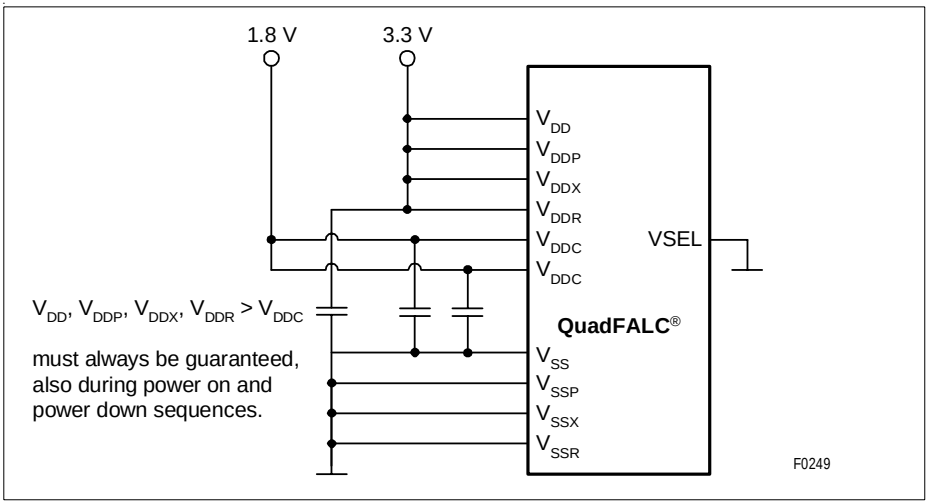


Figure 9 Dual Voltage Supply

3.3.2 Power Supply Decoupling

To gain best performance, the following values are recommended for the external decoupling capacitors between V_{DDC} and V_{SS}. There is one decoupling capacitor required on each V_{DDC} pin.

Table 6 Decoupling Capacitor Parameters

Parameter	Value
Capacitance	470 nF ± 20%, alternatively: 2 x 220 nF ± 20%
Capacitor material	ceramic, type X7R or compatible
ESR	< 30 mΩ
Loop inductance (L_L) between V_{DDC}, capacitor and next V_{SS} pin	< 10nH

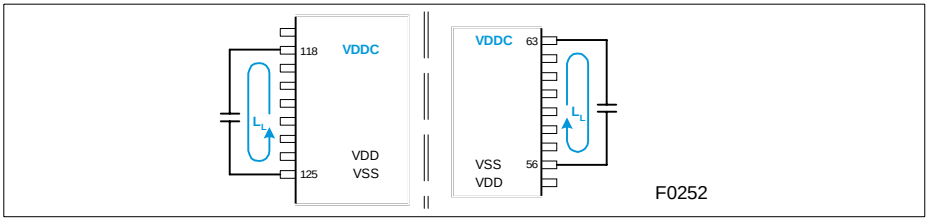


Figure 10 Decoupling Capacitor Placement

3.4 Functional Blocks

3.4.1 Microprocessor Interface

The communication between the CPU and the QuadFALC is done using a set of directly accessible registers. The interface can be configured as Intel or Motorola type with a selectable data bus width of 8 or 16 bits.

The CPU transfers data to/from the QuadFALC (through 64-byte deep FIFOs per direction), sets the operating modes, controls function sequences, and gets status information by writing or reading control/status registers. All accesses can be done as byte or word accesses if enabled. If 16-bit bus width is selected, access to lower/upper part of the data bus is determined by address line A0 and signal $\overline{BHE}$/$\overline{BLE}$ as shown in **Table 7** and **Table 8**.

Table 9 shows how the ALE (address latch enable) line is used to control the bus structure and interface type. The switching of ALE allows the QuadFALC to be directly connected to a multiplexed address/data bus.

3.4.1.1 Mixed Byte/Word Access to the FIFOs

Reading from or writing to the internal FIFOs (RFIFO and XFIFO) can be done using a 8-bit (byte) or 16-bit (word) access depending on the selected bus interface mode. Randomly mixed byte/word access to the FIFOs is allowed without any restrictions.

Table 7 Data Bus Access (16-Bit Intel Mode)

BHE	A0	Register Access	QuadFALC Data Pins Used
0	0	FIFO word access Register word access (even addresses)	D(15:0)
0	1	Register byte access (odd addresses)	D(15:8)
1	0	Register byte access (even addresses)	D(7:0)
1	1	No transfer performed	None

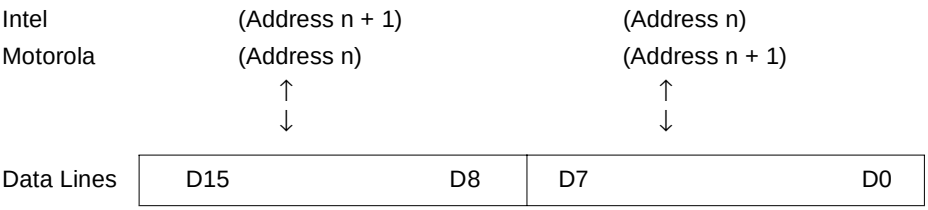
Table 8 Data Bus Access (16-Bit Motorola Mode)

BLE	A0	Register Access	QuadFALC Data Pins Used
0	0	FIFO word access Register word access (even addresses)	D(15:0)
0	1	Register byte access (odd addresses)	D(7:0)
1	0	Register byte access (even addresses)	D(15:8)
1	1	No transfer performed	None

Table 9 Selectable Bus and Microprocessor Interface Configuration

ALE	IM	Microprocessor interface	Bus Structure
GND/VDD	1	Motorola	demultiplexed
GND/VDD	0	Intel	demultiplexed
switching	0	Intel	multiplexed

The assignment of registers with even/odd addresses to the data lines in case of 16-bit register access depends on the selected microprocessor interface mode:



n: even address

3.4.1.2 FIFO Structure

In transmit and receive direction of the signaling controller 64-byte deep FIFOs are provided for the intermediate storage of data between the system internal highway and the CPU interface. The FIFOs are divided into two halves of 32 bytes. Only one half is accessible to the CPU at any time.

In case 16-bit data bus width is selected by fixing pin DBW to logical 1 word access to the FIFOs is enabled. Data output to bus lines D(15:0) as a function of the selected interface mode is shown in **Figure 11** and **Figure 12**. Of course, byte access is also allowed. The effective length of the accessible part of RFIFO can be changed from 32 bytes (RESET value) down to 2 bytes.

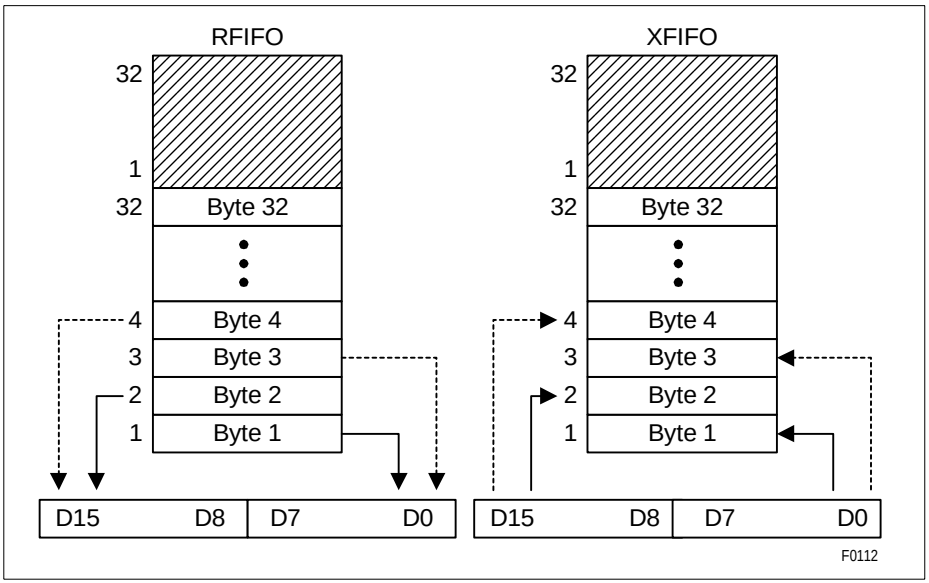


Figure 11 FIFO Word Access (Intel Mode)

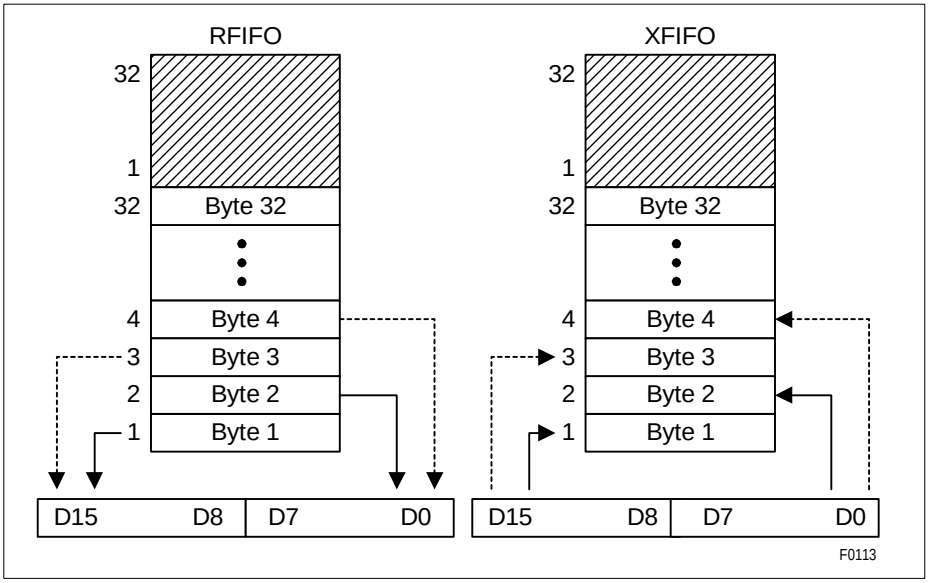


Figure 12 FIFO Word Access (Motorola Mode)

3.4.1.3 Interrupt Interface

Special events in the QuadFALC are indicated by means of a single interrupt output with programmable characteristics (open drain or push-pull, defined by register IPC), which requests the CPU to read status information from the QuadFALC, or to transfer data from/to the QuadFALC.

Since only one INT request output is provided, the cause of an interrupt must be determined by the CPU by reading the QuadFALC's interrupt status registers (GIS, ISR(4:0)). The interrupt at pin INT and the interrupt status bits are reset by reading the interrupt status registers. Register ISR(4:0) are of type "Clear on Read".

The structure of the interrupt status registers is shown in **Figure 13**.

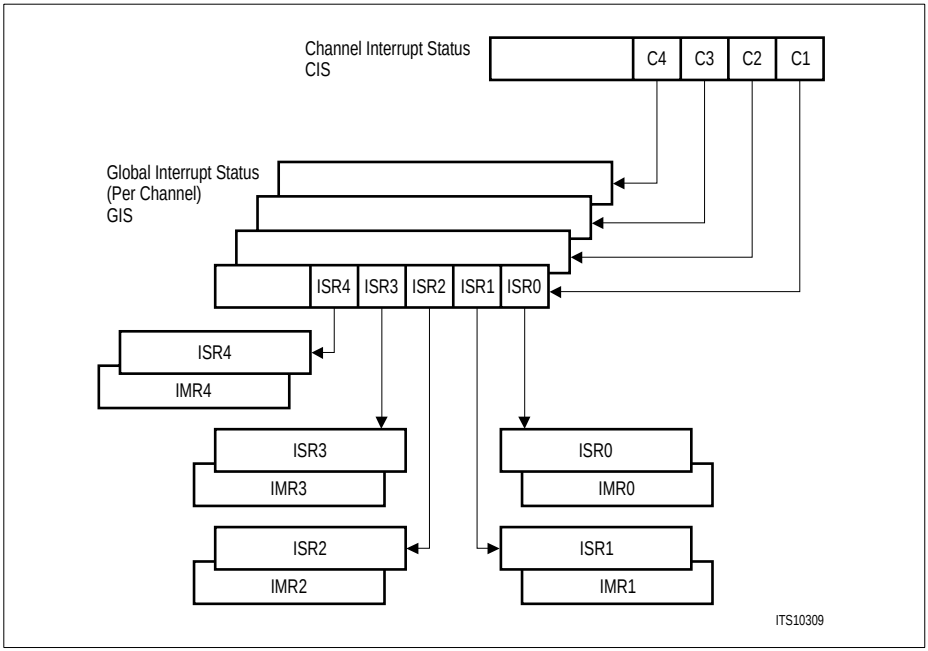


Figure 13 Interrupt Status Registers

Each interrupt indication of registers ISR(4:0) can be selectively masked by setting the corresponding bit in the corresponding mask registers IMR(4:0). If the interrupt status bits are masked they neither generate an interrupt at INT nor are they visible in ISR(4:0).

GIS, the non-maskable Global Interrupt Status Register, serves as pointer to pending interrupts. After the QuadFALC has requested an interrupt by activating its INT pin, the CPU should first read the Global Interrupt Status register GIS to identify the requesting interrupt source register. After reading the assigned interrupt status registers ISR(4:0), the pointer in register GIS is cleared or updated if another interrupt requires service.

If **all** pending interrupts are acknowledged by reading (GIS is reset), pin INT goes inactive.

Updating of interrupt status registers ISR(4:0) and GIS is only prohibited during read access.

Masked Interrupts Visible in Status Registers

- The Global Interrupt Status register (GIS) indicates those interrupt status registers with active interrupt indications (GIS.ISR(4:0)).
- An additional mode can be selected by bit GCR.VIS.

- In this mode, masked interrupt status bits neither generate an interrupt at pin INT nor are they visible in GIS, **but are displayed in the corresponding interrupt status register(s) ISR(4:0)**.

This mode is useful when some interrupt status bits are to be polled in the individual interrupt status registers.

Note: In the visible mode, all active interrupt status bits, whether the corresponding actual interrupt is masked or not, are reset when the interrupt status register is read. Thus, when polling of some interrupt status bits is desired, care must be taken that unmasked interrupts are not lost in the process.

Note: All unmasked interrupt statuses are treated as before.

Please note that whenever polling is used, all interrupt status registers concerned have to be polled individually (no “hierarchical” polling possible), since GIS only contains information on actually generated, i.e. unmasked interrupts.

3.4.2 Boundary Scan Interface

In the QuadFALC a **T**est **A**ccess **P**ort (TAP) controller is implemented. The essential part of the TAP is a finite state machine (16 states) controlling the different operational modes of the boundary scan. Both, TAP controller and boundary scan, meet the requirements given by the JTAG standard IEEE 1149.1. **Figure 14** gives an overview.

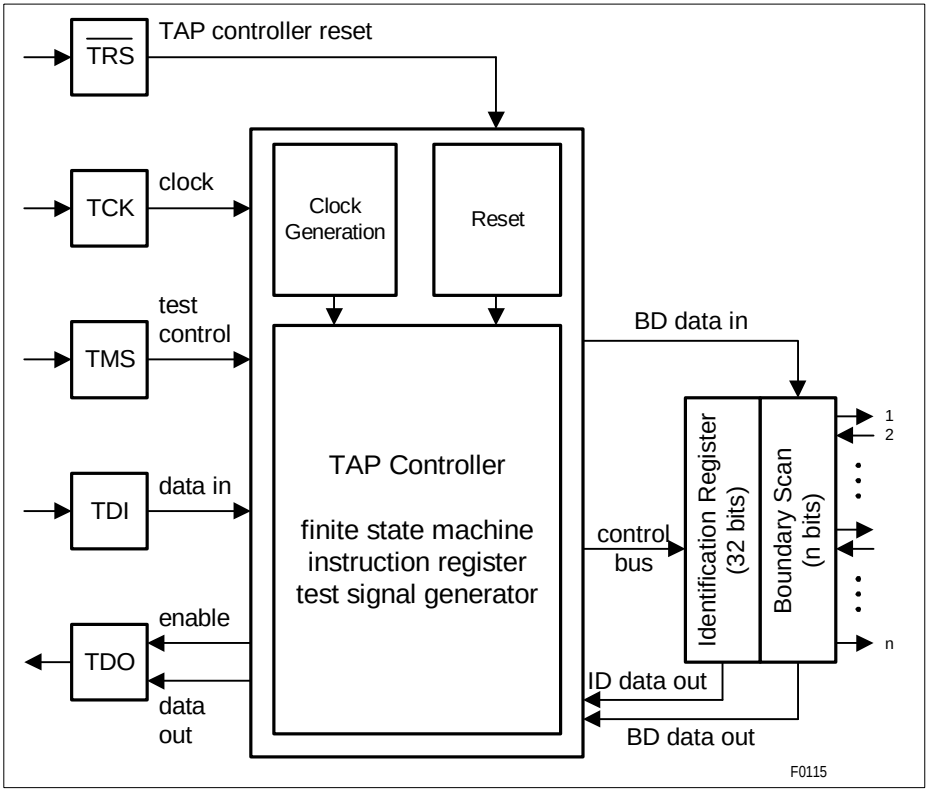


Figure 14 Block Diagram of Test Access Port and Boundary Scan

After switching on the device (power-on), a reset signal has to be applied to $\overline{\text{TRS}}$, which forces the TAP controller into test logic reset state.

For normal operation without boundary scan access, the boundary reset pin $\overline{\text{TRS}}$ can be tied to the device reset pin $\overline{\text{RES}}$.

The boundary length is 272.

If no boundary scan operation is used, $\overline{TRS}$ has to be connected to $\overline{RST}$ or V_{SS}. TMS, TCK and TDI do not need to be connected since pull-up transistors ensure high input levels in this case.

Test handling (boundary scan operation) is performed using the pins TCK (Test Clock), TMS (Test Mode Select), TDI (Test Data Input) and TDO (Test Data Output) when the TAP controller is not in its reset state, that means $\overline{TRS}$ is connected to V_{DD} or it remains unconnected due to its internal pull up. Test data at TDI is loaded with a clock signal connected to TCK. ‘1’ or ‘0’ on TMS causes a transition from one controller state to another; constant ‘1’ on TMS leads to normal operation of the chip.

An input pin (I) uses one boundary scan cell (data in), an output pin (O) uses two cells (data out and enable) and an I/O-pin (I/O) uses three cells (data in, data out and enable). Note that most functional output and input pins of the QuadFALC are tested as I/O pins in boundary scan, hence using three cells. The desired test mode is selected by serially loading a 8-bit instruction code into the instruction register through TDI (LSB first).

EXTEST is used to examine the interconnection of the devices on the board. In this test mode at first all input pins capture the current level on the corresponding external interconnection line, whereas all output pins are held at constant values (‘0’ or ‘1’). Then the contents of the boundary scan is shifted to TDO. At the same time the next scan vector is loaded from TDI. Subsequently all output pins are updated according to the new boundary scan contents and all input pins again capture the current external level afterwards, and so on.

SAMPLE is a test mode which provides a snapshot of pin levels during normal operation.

IDCODE: A 32-bit identification register is serially read out on pin TDO. It contains the version number (4 bits), the device code (16 bits) and the manufacturer code (11 bits). The LSB is fixed to ‘1’.

The ID code field is set to: 0011 0000 0000 0100 1101 0000 1000 0011

Version = $3_{H,}$ Part Number = $004D_H$, Manufacturer = 083_H (including LSB, fixed to ’1’)

BYPASS: A bit entering TDI is shifted to TDO after one TCK clock cycle.

An alphabetical overview of all TAP controller operation codes is given in **Table 10**.

Table 10 TAP Controller Instruction Codes

TAP Instruction	Instruction Code
BYPASS	11111111
EXTEST	00000000
IDCODE	00000100
SAMPLE	00000001
reserved for device test	01010011

3.4.3 Master Clocking Unit

The QuadFALC provides a flexible clocking unit, which references to any clock in the range of 1.02 to 20 MHz supplied on pin MCLK.

The clocking unit has to be tuned to the selected reference frequency by setting the global clock mode registers (GCM(8:1)) accordingly.

The calculation formulas for the appropriate register settings can be found in **Chapter 9.2** on **page 220** or **Chapter 10.2** on **page 320**. A calculation tool is available to evaluate the required register settings automatically (see **Chapter 13.3** on **page 456**).

All required clocks for E1 or T1/J1 operation are generated by this circuit internally. The global setting depends only on the selected master clock frequency and is the same for E1 and T1/J1 because both clock rates are provided simultaneously.

Each of the four channels can be selected for E1 or T1/J1 mode individually.

To meet the E1 requirements the MCLK reference clock must have an accuracy of better than ± 32 ppm. The synthesized clock can be controlled on pins RCLK, SCLKR and XCLK.

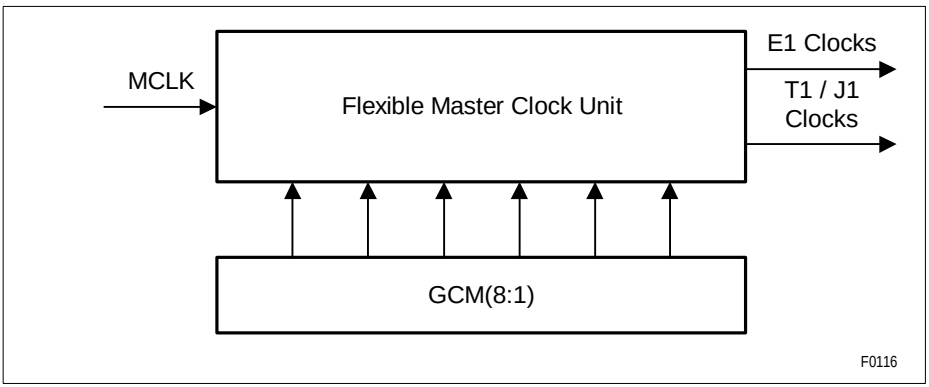


Figure 15 Flexible Master Clock Unit

4 Functional Description E1

4.1 Receive Path in E1 Mode

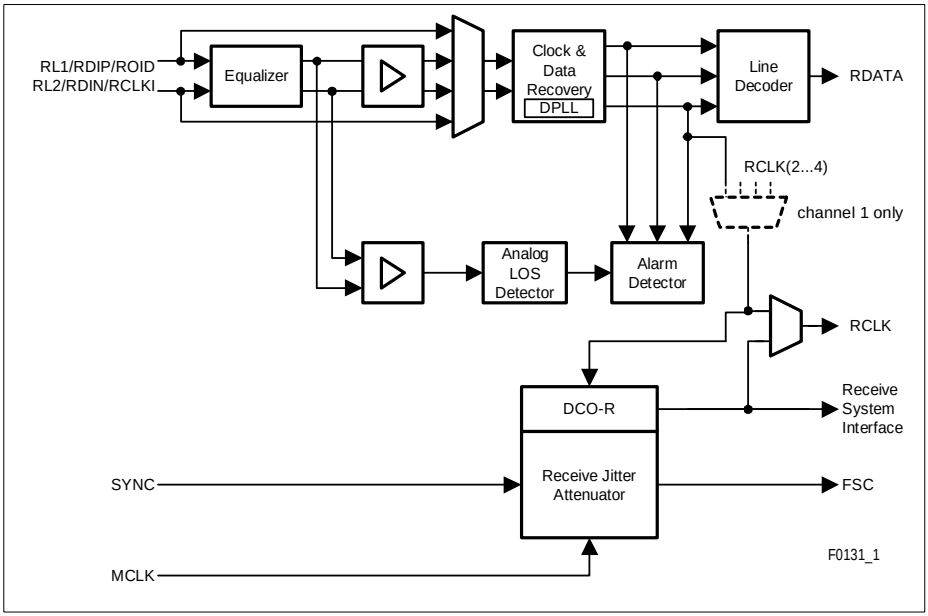


Figure 16 Receive Clock System (E1)

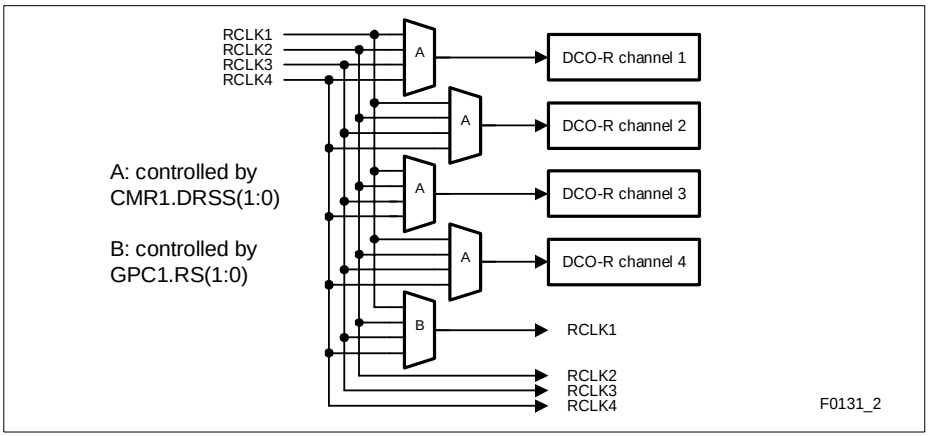


Figure 17 Receive Clock Selection (E1)

4.1.1 Receive Line Interface

For data input, three different data types are supported:

- Ternary coded signals received at multifunction ports RL1 and RL2 from a -10 dB (short haul, LIM0.EQON = 0) or -43 dB (long haul, LIM0.EQON = 1) ternary interface. The ternary interface is selected if LIM1.DRS is reset.
- Digital dual rail signals received on ports RDIP and RDIN. The dual rail interface is selected if LIM1.DRS and FMR0.RC1 is set.
- Unipolar data on port ROID received from a fibre optical interface. The optical interface is selected if LIM1.DRS is set and FMR0.RC1 is reset.

4.1.2 Receive Short and Long Haul Interface

The QuadFALC has an integrated short haul and long haul line interface, including a receive equalization network and noise filtering.

4.1.3 Receive Equalization Network (E1)

The QuadFALC automatically recovers the signals received on pins RL1/2 in a range of up to -43 dB. The maximum reachable length with a 22 AWG twisted pair cable is 1500 m. After reset the QuadFALC is in short haul mode, received signals are recovered up to -10 dB of cable attenuation. Automatic short haul/long haul detection and adjustment is done by setting of bit LIM0.EQON.
The integrated receive equalization network recovers signals with up to -43 dB of cable attenuation. Noise filters eliminate the higher frequency part of the received signals. The incoming data is peak detected and sliced to produce the digital data stream. The slicing level is software selectable in four steps (45%, 50%, 55%, 67%). For typical E1 applications, a level of 50% is used. The received data is then forwarded to the clock & data recovery unit.

In long-haul mode, the current equalizer status is indicated by register RES (Receive Equalizer Status).

4.1.4 Receive Line Attenuation Indication (E1)

Status register RES reports the current receive line attenuation in a range from 0 to -43 dB in 25 steps of approximately 1.7 dB each. The least significant 5 bits of this register indicate the cable attenuation in dB. These 5 bits are only valid in combination with the most significant two bits (RES.EV1/0 = 01).

4.1.5 Receive Clock and Data Recovery (E1)

The analog received signal on port RL1/2 is equalized and then peak-detected to produce a digital signal. The digital received signal on port RDIP/N is directly forwarded to the DPLL. The receive clock and data recovery extracts the route clock from the data stream received at the RL1/2, RDIP/RDIN or ROID lines and converts the data stream into a single rail, unipolar bit stream. The clock and data recovery uses an internally generated high frequency clock based on MCLK.

The recovered route clock or a dejittered clock can be output on pin RCLK as shown in **Table 11**. Additionally, RCLK1 can output the receive clocks of channels 2, 3 or 4 (RCLK(4:2), selected by CMR1.DRSS(1:0)).

See also **Table 14** on page **72** for details of master/slave clocking.

Table 11 RCLK Output Selection (E1)

Clock Source	RCLK Frequency	CMR1. RS1/0
Receive Data (2.048 Mbit/s on RL1/RL2, RDIP/RDIN or ROID)	2.048 MHz (recovered clock)	00
Receive Data (2.048 Mbit/s on RL1/RL2, RDIP/RDIN or ROID) in case of LOS	constant high	01
DCO-R	2.048 MHz	10
	8.192 MHz	11

The intrinsic jitter generated in the absence of any input jitter is not more than 0.035 UI. In digital bipolar line interface mode the clock and data recovery requires HDB3 coded signals with 50% duty cycle.

4.1.6 Receive Line Coding (E1)

The HDB3 line code or the AMI coding is provided for the data received from the ternary or the dual rail interface. In case of the optical interface a selection between the NRZ code and the CMI Code (1T2B) with HDB3 or AMI postprocessing is provided. If CMI code is selected the receive route clock is recovered from the data stream. The CMI decoder does not correct any errors. In case of NRZ coding data is latched with the falling edge of signal RCLKI. The HDB3 code is used along with double violation detection or extended code violation detection (selectable by FMR0.EXZE)). In AMI code all code violations are detected. The detected errors increment the code violation counter (16 bits length).

When using the optical interface with NRZ coding, the decoder is bypassed and no code violations are detected.

The signal at the ternary interface is received at both ends of a transformer.

The E1 operating modes 75 Ω or 120 Ω are selectable by switching resistors in parallel or using special transformers with different transfer ratios in one package (using center tap). This selection does not require changing transformers.

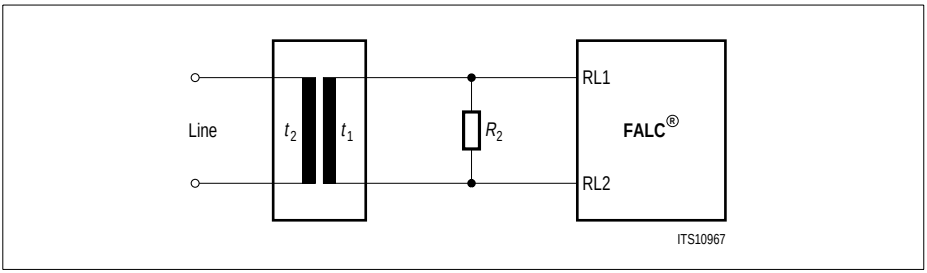


Figure 18 Receiver Configuration (E1)

Table 12 Recommended Receiver Configuration Values (E1)

Parameter[1)]	Characteristic Impedance [Ω]	
	120	**75**
R_2 (± 1%) [Ω]	120	75
$t_2 : t_1$	1 : 1	1 : 1

1) This includes all parasitic effects caused by circuit board design.

4.1.7 Receive Line Monitoring Mode

For short haul applications like shown in **Figure 19**, the receive equalizer can be switched into receive line monitoring mode (LIM0.RLM = 1). One device is used as a short haul receiver while the other is used as a short haul monitor. In this mode the receiver sensitivity is increased to detect an incoming signal of -20 dB resistive attenuation. The required resistor values are given in **Table 13**.

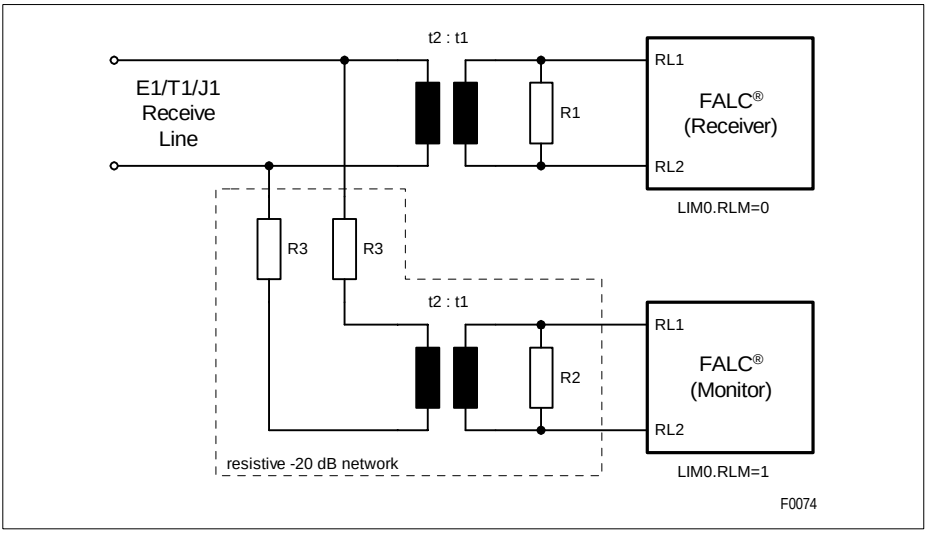


Figure 19 Receive Line Monitoring

Table 13 External Component Recommendations (Monitoring)

Parameter[1)]	Characteristic Impedance [Ω]	
	E1	
	75	120
R_1 (± 1 %) [Ω]	75	120
R_2 (± 1 %) [Ω]	75	120
R_3 (± 1 %) [Ω]	330	510
$t_2 : t_1$	1 : 1	1 : 1

1) This includes all parasitic effects caused by circuit board design.

Using the receive line monitor mode and the hardware tristate function of transmit lines XL1/2, the QuadFALC now supports applications connecting two devices to one receive

and transmission line. In these kind of applications both devices are working in parallel for redundancy purpose (see **Figure 20**). While one of them is driving the line, the other one must be switched into transmit line tristate mode. If both channels are configured identically and supplied with the same system data and clocks, the transmit path can be switched from one channel to the other without causing a synchronization loss at the remote end.

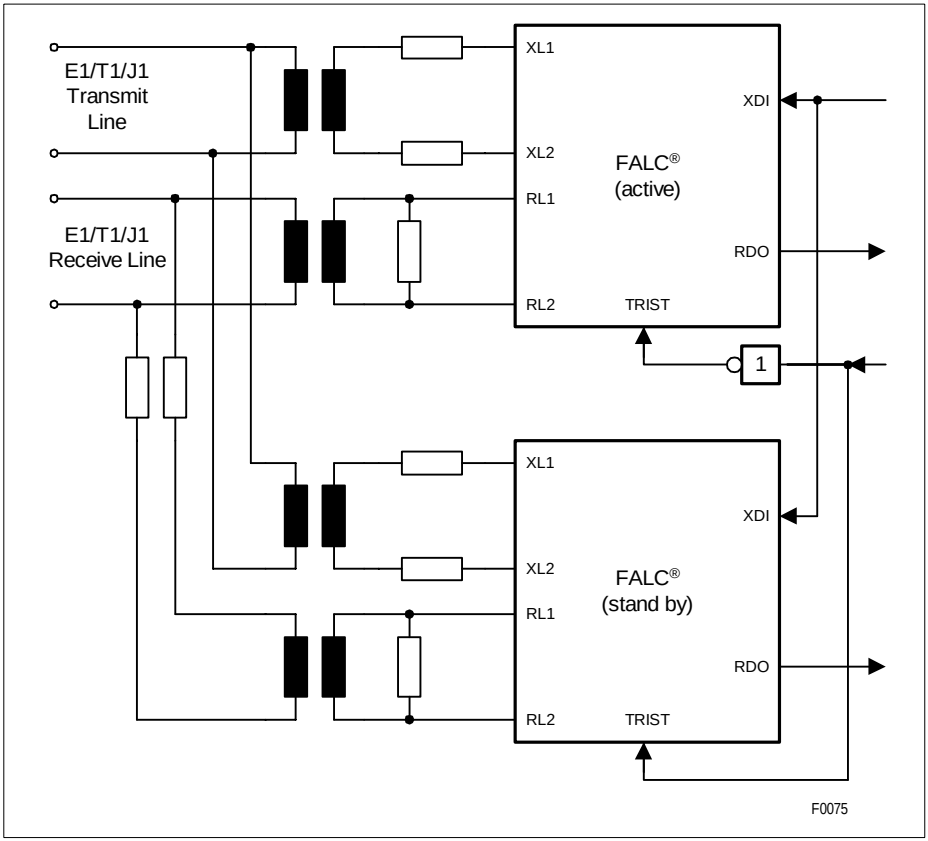


Figure 20 Protection Switching Application

4.1.8 Loss of Signal Detection (E1)

There are different definitions for detecting Loss of Signal (LOS) alarms in the ITU-T G.775 and ETS 300233. The QuadFALC covers all these standards. The LOS indication is performed by generating an interrupt (if not masked) and activating a status bit. Additionally a LOS status change interrupt is programmable by using register GCR.SCI.

- Detection:
  An alarm is generated if the incoming data stream has no pulses (no transitions) for a certain number (N) of consecutive pulse periods. “No pulse” in the digital receive interface means a logical zero on pins RDIP/RDIN/ROID. A pulse with an amplitude less than P dB below nominal is the criteria for “no pulse” in the analog receive interface (LIM1.DRS = 0). The receive signal level P is programmable by three control bits LIM1.RIL(2:0) (see **Chapter 11.3** on page **422**). The number N can be set by an 8-bit register (PCD). The contents of the PCD register is multiplied by 16, which results in the number of pulse periods, i.e. the time which has to suspend until the alarm has to be detected. The programmable range is 16 to 4096 pulse periods. ETS300233 requires detection intervals of at least 1 ms. This time period results always in a LFA (Loss of Frame Alignment) before a LOS is detected.
- Recovery:
  In general the recovery procedure starts after detecting a logical one (digital receive interface) or a pulse (analog receive interface) with an amplitude more than P dB (defined by LIM1.RIL(2:0)) of the nominal pulse. The value in the 8-bit register PCR defines the number of pulses (1 to 255) to clear the LOS alarm.

If a loss of signal condition is detected in long-haul mode, the data stream can optionally be cleared automatically to avoid bit errors before LOS is indicated. The selection is done by LIM1.CLOS = 1.

4.1.9 Receive Jitter Attenuator (E1)

The receive jitter attenuator is placed in the receive path. The working clock is an internally generated high frequency clock based on the clock provided on pin MCLK. The jitter attenuator meets the requirements of ITU-T I.431, G. 736 to 739, G.823 and ETSI TBR12/13.

The internal PLL circuitry DCO-R generates a ’jitter free’ output clock which is directly dependent on the phase difference of the incoming clock and the jitter attenuated clock.The receive jitter attenuator can be synchronized either on the extracted receive clock RCLK or on a 2.048-MHz/8-kHz clock provided on pin SYNC (8 kHz in master mode only). The received data is written into the receive elastic buffer with RCLK and are read out with the dejittered clock sourced by DCO-R. The jitter attenuated clock can be output on pins RCLK or SCLKR. Optionally an 8-kHz clock is provided on pin SEC/FSC.

The DCO-R circuitry attenuates the incoming jittered clock starting at 2-Hz jitter frequency with 20 dB per decade fall off. Wander with a jitter frequency below 2 Hz is passed unattenuated. The intrinsic jitter in the absence of any input jitter is < 0.02 UI.

For some applications it might be useful starting of jitter attenuation at lower frequencies. Therefore the corner frequency is switchable by the factor of ten downto 0.2 Hz (LIM2.SCF).

The DCO-R circuitry is automatically centered to the nominal bit rate if the reference clock on pin SYNC/RCLK is missed for 2 to 4 2.048-MHz clock periods (only if 2.048 MHz clock is used). This center function of DCO-R can be disabled (CMR2.DCF = 1) in order to accept a gapped reference clock. In analog line interface mode RCLK is always running. Only in digital line interface mode with single rail data a gapped clock can occur.

The receive jitter attenuator works in two different modes:

- Slave mode
  In slave mode (LIM0.MAS = 0) the DCO-R is synchronized on the recovered route clock. In case of LOS the DCO-R switches automatically to Master mode. If bit CMR1.DCS is set automatic switching from RCLK to SYNC is disabled.
- Master mode
  In master mode (LIM0.MAS = 1) the jitter attenuator is in free running mode if no clock is supplied on pin SYNC. If an external clock on the SYNC input is applied, the DCO-R synchronizes to this input. The external frequency can be 2.048 MHz (IPC.SSYF = 0) or 8.0 kHz (IPC.SSYF = 1).

The following table shows the clock modes with the corresponding synchronization sources.

Table 14 System Clocking (E1)

Mode	Internal LOS Active	SYNC Input	System Clocks generated by DCO-R
Master	independent	Fixed to VDD	DCO-R centered, if CMR2.DCF = 0. (CMR2.DCF should not be set)
Master	independent	2.048 MHz	Synchronized to SYNC input (external 2.048 MHz, IPC.SSYF = 0)
Master	independent	8.0 kHz	Synchronized to SYNC input (external 8.0 kHz, IPC.SSYF = 1, CMR2.DCF = 0)
Slave	no	Fixed to VDD	Synchronized to line RCLK
Slave	no	2.048 MHz	Synchronized to line RCLK

Table 14 System Clocking (E1) (cont'd)

Mode	Internal LOS Active	SYNC Input	System Clocks generated by DCO-R
Slave	yes	Fixed to VDD	CMR1.DCS = 0: DCO-R is centered, if CMR2.DCF = 0. (CMR2.DCF should not be set)
			CMR1.DCS = 1: Synchronized on line RCLK
Slave	yes	2.048 MHz	CMR1.DCS = 0: Synchronized to SYNC input (external 2.048 MHz)
			CMR1.DCS = 1: Synchronized on line clock RCLK(4:1), channel selected by CMR1.DRSS(1:0)

The jitter attenuator meets the jitter transfer requirements of the ITU-T I.431 and G.735 to 739 (refer to **Figure 21**)

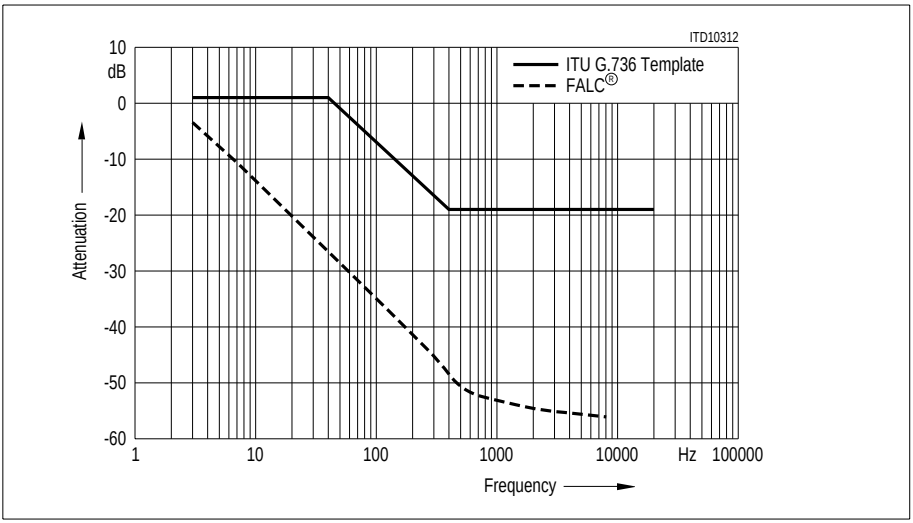


Figure 21 Jitter Attenuation Performance (E1)

Also the requirements of ETSI TBR12/13 are satisfied. Insuring adequate margin against TBR12/13 output jitter limit with 15 UI input at 20 Hz the DCO-R circuitry starts jitter attenuation at about 2 Hz.

4.1.10 Jitter Tolerance (E1)

The QuadFALC receiver's tolerance to input jitter complies to ITU for CEPT application.

Figure 22 shows the curves of different input jitter specifications stated below as well as the QuadFALC performance.

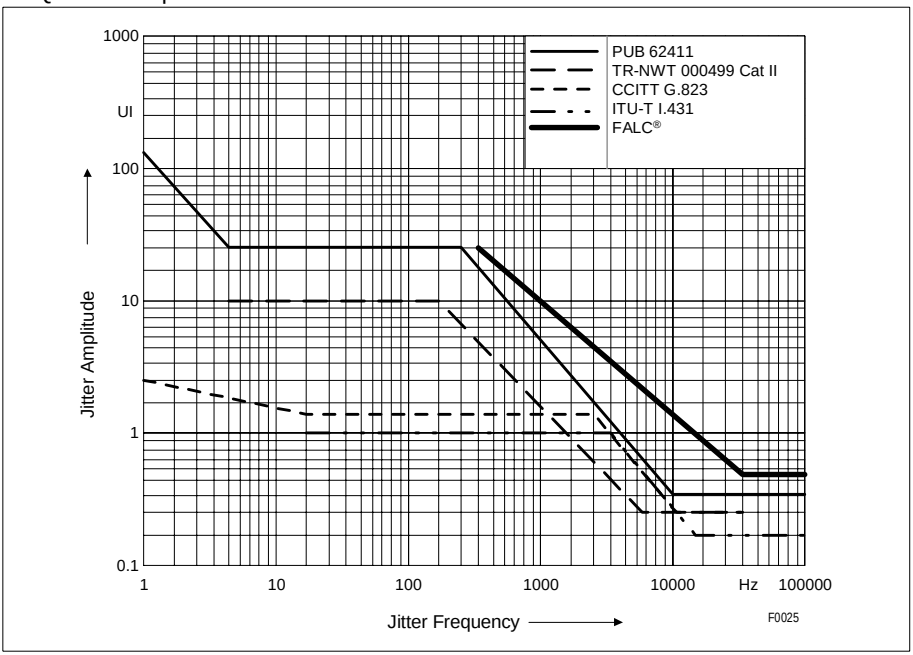


Figure 22 Jitter Tolerance (E1)

4.1.11 Output Jitter (E1)

In the absence of any input jitter the QuadFALC generates the output jitter, which is specified in the**Table 15** below.

Table 15 Output Jitter (E1)

Specification	Measurement Filter Bandwidth		Output Jitter (UI peak to peak)
	Lower Cutoff	Upper Cutoff	
ITU-T I.431	20 Hz	100 kHz	< 0.015
	700 Hz	100 kHz	< 0.015
ETSI TBR 12	40 Hz	100 kHz	< 0.11

4.1.12 Framer/Synchronizer (E1)

The following functions are performed:

- Synchronization on pulse frame and multiframe
- Error indication when synchronization is lost. In this case, AIS is sent automatically to the system side and remote alarm is sent to the remote end if enabled.
- Initiating and controlling of resynchronization after reaching the asynchronous state. This can be done automatically by the QuadFALC or user controlled using the microprocessor interface.
- Detection of remote alarm indication from the incoming data stream.
- Separation of service bits and data link bits. This information is stored in status registers.
- Generation of various maskable interrupt statuses of the receiver functions.
- Generation of control signals to synchronize the CRC checker, and the receive elastic buffer.

If programmed and applicable to the selected multiframe format, CRC checking of the incoming data stream is done by generating check bits for a CRC submultiframe according to the CRC4 procedure (refer to ITU-T G.704). These bits are compared with those check bits that are received during the next CRC submultiframe. If there is at least one mismatch, the CRC error counter (16 bit) is incremented.

4.1.13 Receive Elastic Buffer (E1)

The received bit stream is stored in the receive elastic buffer. The memory is organized as a two-frame elastic buffer with a maximum size of 64 $\times$ 8 bit. The size of the elastic buffer can be configured independently for the receive and transmit direction. Programming of the receive buffer size is done by SIC1.RBS1/0:

- RBS1/0 = 00: two frame buffer or 512 bits
  Maximum of wander amplitude (peak-to-peak): 190 UI (1 UI = 488 ns)
  average delay after performing a slip: 1 frame or 256 bits
- RBS1/0 = 01: one frame buffer or 256 bits
  Maximum of wander amplitude: 100 UI
  average delay after performing a slip: 128 bits, (RFM)
- RBS1/0 = 10: short buffer or 96 bits
  Maximum of wander amplitude: 38 UI
  average delay after performing a slip: 48 bits, (RFM)
- RBS1/0 = 11: bypass of the receive elastic buffer

The functions are:

- Clock adaptation between system clock (SCLKR) and internally generated route clock (RCLK).
- Compensation of input wander and jitter.
- Frame alignment between system frame and receive route frame
- Reporting and controlling of slips

Controlled by special signals generated by the receiver, the unipolar bit stream is converted into bit-parallel data which is circularly written to the elastic buffer using internally generated receive route clock (RCLK).

Reading of stored data is controlled by the system clock sourced by SCLKR or by the receive jitter attenuator and the synchronization pulse ($\overline{\text{SYPR}}$) together with the programmed offset values for the receive time slot/clock slot counters. After conversion into a serial data stream, the data is given out on port RDO. If the receive buffer is bypassed programming of the time slot offset is disabled and data is clocked off with RCLK instead of SCLKR.

In one frame or short buffer mode the delay through the receive buffer is reduced to an average delay of 128 or 46 bits. In bypass mode the time slot assigner is disabled. In this case $\overline{\text{SYPR}}$ programmed as input is ignored. Slips are performed in all buffer modes except the bypass mode. After a slip is detected the read pointer is adjusted to one half of the current buffer size.

The following table gives an overview of the receive buffer operating mode.

Table 16 Receive Buffer Operating Modes (E1)

Buffer Size (SIC1.RBS1/0)	**TS Offset programming (RC1/0) + $\overline{\text{SYPR}}$ = input**	**Slip performance**
bypass[1)]	disabled recommended: RFM	no
short buffer	not recommended, recommended: RFM	yes
1 frame	not recommended, recommended: RFM	yes
2 frames	enabled	yes

1) In bypass mode the clock provided on pin SCLKR is ignored. Clocking is done with RCLK.

In single frame mode (SIC1.RBS), values of receive time slot offset (RC1/0) have to be specified great enough to prevent too great approach of frame begin of line side and frame begin of system side.

Figure 23 gives an idea of operation of the receive elastic buffer:
A slip condition is detected when the write pointer (W) and the read pointer (R) of the memory are nearly coincident, i.e. the read pointer is within the slip limits (S +, S –). If a slip condition is detected, a negative slip (one frame or one half of the current buffer size is skipped) or a positive slip (one frame or one half of the current buffer size is read out twice) is performed at the system interface, depending on the difference between RCLK and the current working clock of the receive backplane interface. I.e. on the position of pointer R and W within the memory. A positive/negative slip is indicated in the interrupt status bits ISR3.RSP and ISR3.RSN.

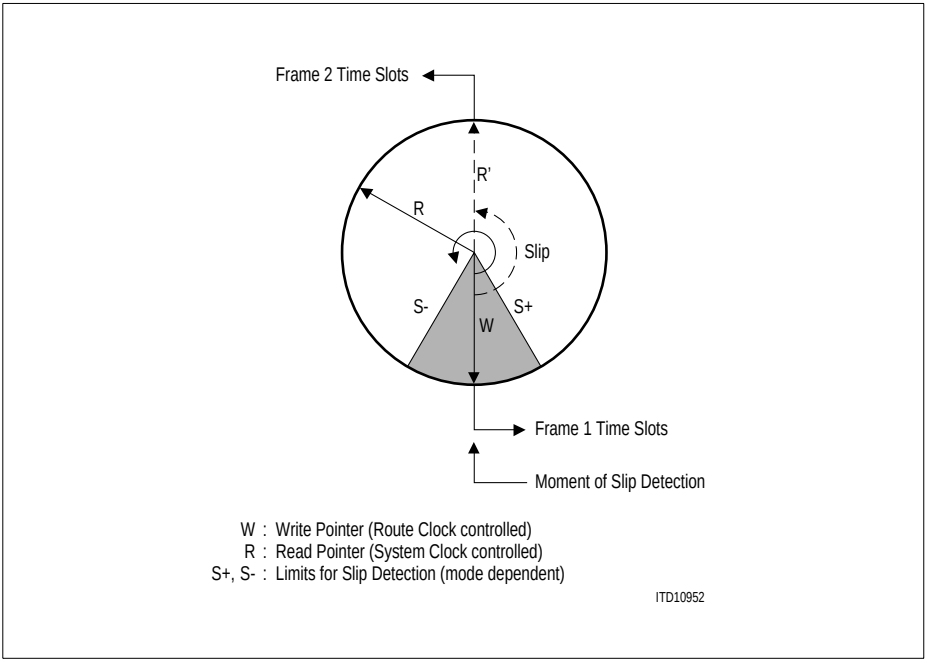


Figure 23 The Receive Elastic Buffer as Circularly Organized Memory

4.1.14 Receive Signaling Controller (E1)

The signaling controller can be programmed to operate in various signaling modes. The QuadFALC performs the following signaling and data link methods.

4.1.14.1 HDLC or LAPD access

The QuadFALC offers one HDLC controller for each channel. All of them provide the following features:

- 64 byte receive FIFO for each channel
- 64 byte transmit FIFO for each channel
- transmission in up to 32 time slots
  (time slot number programmable for each channel individually)
- transmission in even frames only, odd frames only or both
  (programmable for each channel individually)
- bit positions to be used in selected time slots are maskable
  (any bit position can be enabled for each channel individually)
- HDLC or transparent mode
- flag detection
- CRC checking
- bit-stuffing
- flexible address recognition (1 byte, 2 bytes)
- C/R-bit processing (according to LAPD protocol)
- SS7 support
- BOM (bit oriented message) support
- use of time slot 0
- use of S_a-bits
- flexibility to insert and extract data during certain time slots, any combination of time slots can be programmed independently for the receive and transmit direction

In case of common channel signaling the signaling procedure HDLC/SDLC or LAPD according to Q.921 is supported. The signaling controller of the QuadFALC performs the flag detection, CRC checking, address comparison and zero-bit removing. The received data flow and the address recognition features can be performed in very flexible way, to satisfy almost any practical requirements. Depending on the selected address mode, the QuadFALC performs a 1 or 2-byte address recognition. If a 2-byte address field is selected, the high address byte is compared with the fixed value FEH or FCH (group address) as well as with two individually programmable values in RAH1 and RAH2 registers. According to the ISDN LAPD protocol, bit 1 of the high byte address is interpreted as command/response bit (C/R) and is excluded from the address comparison. Buffering of receive data is done in a 64 byte deep RFIFO.
In signaling controller transparent mode, fully transparent data reception without HDLC framing is performed, i.e. without flag recognition, CRC checking or bit stuffing. This allows user specific protocol variations.

4.1.14.2 Support of Signaling System #7

The HDLC controller supports the signaling system #7 (SS7) which is described in ITU-Q.703. The following description assumes, that the reader is familiar with the SS7 protocol definition.

SS7 support must be activated by setting the MODE register. The SS7 protocol is supported by the following hardware features in receive mode:

- all Signaling Units (SU) are stored in the receive FIFO (RFIFO)
- detecting of flags from the incoming data stream
- bit stuffing (zero deletion)
- checking of seven or more consecutive ones in the receive data stream (octet counting mode handling according to ITU-T Q.703)
- checking if the received Signaling Unit is a multiple of eight bits and at least six octets including the opening flag
- calculation of the CRC16 checksum:
  In receive direction the calculated checksum is compared to the received one; errors are reported in register RSIS.
- checking if the signal information field of a received signaling unit consists of more than 272 octets, in this case the current signaling unit is discarded.

In order to reduce the microprocessor load, fill in signaling units (FISUs) are processed automatically. By examining the length indicator of a received signal unit the QuadFALC decides whether a FISU has been received. Consecutively received FISUs are compared and not stored in the receive FIFO (RFIFO, 2×32 bytes), if the contents is equal to the previous one. The same applies to link status signaling units, if bit CCR5.CSF is set. The different types of signaling units as message signaling unit (MSU), link status signaling unit (LSSU) and fill in signaling units (FISU) are indicated in the RSIS register, which is automatically added to the RFIFO with each received signaling unit. The complete signaling unit except start and end flags is stored in the receive FIFO. The functions of bits CCR1.RCRC and CCR1.RADD are still valid in SS7 mode. Errored signaling units are handled automatically according to ITU-T Q.703 as shown in **Figure 24**. SU counter (su) and errored SU counter (C_s) are reset by setting CMDR2.RSUC. The error threshold T can be selected to be 64 (default) or 32 by setting/clearing bit CCR5.SUET. If the defined error limit is exceeded, an interrupt (ISR1.SUEX) is generated, if not masked by IMR1.SUEX = 1.

Note: If SUEX is caused by an aborted/invalid frame, the interrupt will be issued regularly until a valid frame is received (e.g. a FISU).

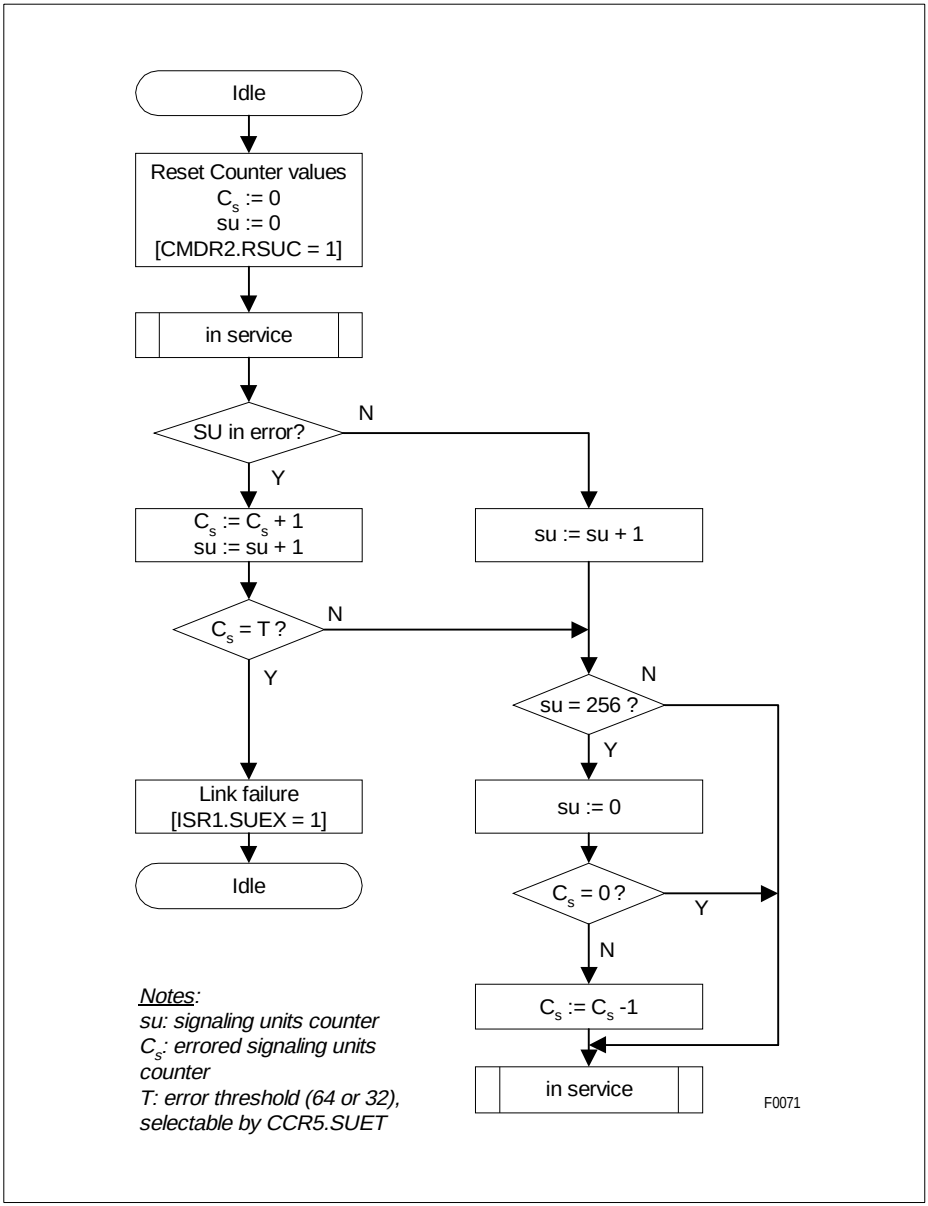


Figure 24 Automatic Handling of Errored Signaling Units

4.1.14.3 S_a-Bit Access (E1)

The QuadFALC supports the S_a-bit signaling of time slot 0 of every other frame as follows:

- the access through register RSW
- the access through registers RSA(8:4), capable of storing the information for a complete multiframe
- the access through the 64 byte deep receive FIFO of the signaling controller. This S_a-bit access gives the opportunity to receive a transparent bit stream as well as HDLC frames where the signaling controller automatically processes the HDLC protocol. Any combination of S_a-bits which shall be extracted and stored in the RFIFO is selected by XC0.SA(8:4). The access to the RFIFO is supported by ISR0.RME/RPF.

4.1.14.4 Channel Associated Signaling CAS (E1, serial mode)

The signaling information is carried in time slot 16 (TS16). The signaling controller samples the bit stream either on the receive line side or if external signaling is enabled on the receive system side. External signaling is enabled by selecting the RSIG pin function in registers PC(4:1) and setting XSP.CASEN = 1.

Optionally the complete CAS multiframe can be transmitted on pin RSIG. The signaling data is clocked with the working clock of the receive highway (SCLKR) together with the receive synchronization pulse ($\overline{\text{SYPR}}$). Data on RSIG is transmitted in the last 4 bits per time slot and is aligned to the data on RDO. The first 4 bits per time slot can be optionally fixed high or low (SIC2.SSF), except for time slot 0 and 16 (bit 1 to 4 are always ’0000’ in TS16). In time slot 0 the FAS/NFAS word is transmitted, in time slot 16 the CAS multiframe pattern ’0000XYXX’. Data on RSIG is only valid if the freeze signaling status is inactive. With FMR1.SAIS an all-ones data stream can be transmitted on RDO and RSIG.
The signaling procedure is done as it is described in ITU-T G.704 and G.732.
The main functions are:

- Synchronization to a CAS multiframe
- Detection of AIS and remote alarm in CAS multiframes
- Separation of CAS service bits X1 to X3

Updating of the received signaling information is controlled by the freeze signaling status. The freeze signaling status is automatically activated if a loss of signal (FRS0.LOS = 1), or a loss of CAS multiframe alignment (FRS1.TSL16LFA = 1) or a receive slip occurs. The current freeze status is output on port FREEZE (RPA to D) and indicated by register SIS.SFS. Optionally automatic freeze signaling can be disabled by setting bit SIC3.DAF.

After CAS resynchronization an interrupt is generated. Because at this time the signaling is still frozen, CAS data is not valid yet. Readout of CAS data has to be delayed until the next CAS multiframe is received.

Because the CAS controller is working on the PCM highway side of the receive buffer, slips disturb the CAS data.

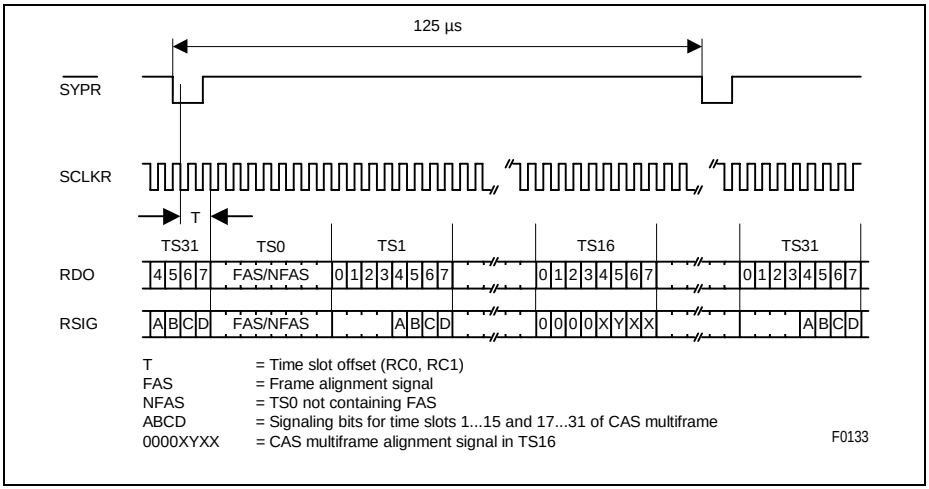


Figure 25 2.048 MHz Receive Signaling Highway (E1)

4.1.14.5 Channel Associated Signaling CAS (E1, µP access mode)

The signaling information is carried in time slot 16 (TS16). Receive data is stored in registers RS(16:1) aligned to the CAS multiframe boundary. The signaling controller samples the bit stream either on the receive line side or if external signaling is enabled on the receive system side.

The signaling procedure is done as it is described in ITU-T G.704 and G.732.
The main functions are:

- Synchronization to a CAS multiframe
- Detection of AIS and remote alarm in CAS multiframes
- Separation of CAS service bits X1 to X3
- Storing of received signaling data in registers RS(16:1) with last look capability

Updating of the received signaling information is controlled by the freeze signaling status. The freeze signaling status is automatically activated if a loss of signal (FRS0.LOS = 1), or a loss of CAS multiframe alignment (FRS1.TSL16LFA = 1) or a receive slip occurs. The current freeze status is output on port FREEZE (RPA to D) and indicated by register SIS.SFS. Optionally automatic freeze signaling can be disabled by setting bit SIC3.DAF. If SIS.SFS is active, updating of the registers RS(16:1) is disabled.

To relieve the microprocessor load from always reading the complete RS(16:1) buffer every 2 ms the QuadFALC notifies the microprocessor through interrupt ISR0.CASC only when signaling changes from one multiframe to the next. Additionally the QuadFALC generates a receive signaling data change pointer (RSP1/2) which directly points to the updated RS(16:1) register.

Because the CAS controller is working on the PCM highway side of the receive buffer, slips disturb the CAS data.

4.2 Framer Operating Modes (E1)

4.2.1 General

Bit: FMR1.PMOD = 0

PCM line bit rate	:	2.048 Mbit/s
Single frame length	:	256 bit, No. 1 to 256
Framing frequency	:	8 kHz
HDLC controller	:	nx64 kbit/s, n = 1 to 32 or n×4 kbit/s, n = 1 to 5
Organization	:	32 time slots, No. 0 to 31 with 8 bits each, No. 1 to 8

The operating mode of the QuadFALC is selected by programming the carrier data rate and characteristics, line code, multiframe structure, and signaling scheme.

The QuadFALC implements all of the standard framing structures for E1 or PCM 30 (CEPT, 2.048 Mbit/s) carriers. The internal HDLC or CAS controller supports all signaling procedures including signaling frame synchronization/synthesis and signaling alarm detection in all framing formats. The time slot assignment from the PCM line to the system highway and vice versa is performed without any changes of numbering (TS0 ↔ TS0, …, TS31 ↔ TS31).

Summary of E1 Framing Modes

- Doubleframe format according to ITU-T G. 704
- Multiframe format according to ITU-T G. 704
- CRC4 processing according to ITU-T G. 706
- Multiframe format with CRC4 to non CRC4 interworking according to ITU-T G. 706
- Multiframe format with modified CRC4 to non CRC4 interworking
- Multiframe format with CRC4 performance monitoring

After RESET, the QuadFALC is switched into doubleframe format automatically. Switching between the framing formats is done by programming bits FMR2.RFS1/0 and FMR3.EXTIW for the receiver and FMR1.XFS for the transmitter.

4.2.2 Doubleframe Format (E1)

The framing structure is defined by the contents of time slot 0 (refer to **Table 17**).

Table 17 Allocation of Bits 1 to 8 of Time Slot 0 (E1)

Bit AlternateNumber Frames	1	2	3	4	5	6	7	8
Frame Containing the Frame Alignment Signal	S_i	0	0	1	1	0	1	1
	Note [1]	Frame Alignment Signal						
Frame not Containing the Frame Alignment Signal or Service Word	S_i	1	A	S_{a4}	S_{a5}	S_{a6}	S_{a7}	S_{a8}
	Note [1]	Note [2]	Note [3]	Note [4]				

[1] S_i-bits: reserved for international use. If not used, these bits should be fixed to '1'. Access to received information trough bits RSW.RSI and RSP.RSIF. Transmission is enabled by bits XSW.XSIS and XSP.XSIF.

[2] Fixed to '1'. Used for synchronization.

[3] Remote alarm indication: In undisturbed operation '0'; in alarm condition '1'.

[4] S_a-bits: Reserved for national use. If not used, they should be fixed at '1'. Access to received information trough bits RSW.RY(4:0). Transmission is enabled by bits XSW.XY(4:0). HDLC signaling in bits S_a(8:4) is selectable. As a special extension for double frame format, the S_a-bit registers RSA(8:4)/XSA(8:4) can be used optionally.

4.2.2.1 Transmit Transparent Modes

In transmit direction, contents of time slot 0 frame alignment signal of the outgoing PCM frame are normally generated by the QuadFALC. However, transparency for the complete time slot 0 can be achieved by selecting the transparent mode XSP.TT0. With the Transparent Service Word Mask register TSWM the S_i-bits, A-bit and the S_a(8:4)-bits can be selectively switched through transparently.

Table 18 Transmit Transparent Mode (Doubleframe E1)

Transmit Transparent Source for				
Enabled by	**Framing**	**A-Bit**	**S_a-Bits**	**S_i-Bits**
–	(int. gen.)	XSW.XRA[2)]	XSW.XY(4:0)[3)]	XSW.XSIS, XSP.XSIF
XSP.TT0	via pin XDI[1)]	via pin XDI	via pin XDI	via pin XDI
TSWM.TSIF	(int. gen.)	XSW.XRA	XSW.XY(4:0)	via pin XDI
TSWM.TSIS	(int. gen.)	XSW.XRA	XSW.XY(4:0)	via pin XDI
TSWM.TRA	(int. gen.)	via pin XDI	XSW.XY(4:0)	XSW.XSIS, XSP.XSIF
TSWM.TSA (8:4)	(int. gen.)	XSW.XRA	via pin XDI	XSW.XSIS, XSP.XSIF

1) pin XDI or XSIG or XFIFO buffer (signaling controller)

2) Additionally, automatic transmission of the A-bit is selectable.

3) As a special extension for double frame format, the S_a-bit register can be used optionally.

4.2.2.2 Synchronization Procedure

Synchronization status is reported by bit FRS0.LFA. Framing errors are counted by the Framing Error Counter (FEC). Asynchronous state is reached after detecting 3 or 4 consecutive incorrect FAS words or 3 or 4 consecutive incorrect service words (bit 2 = 0 in time slot 0 of every other frame not containing the frame alignment word), the selection is done by bit RC0.ASY4. Additionally, the service word condition can be disabled. When the framer lost its synchronization an interrupt status bit ISR2.LFA is generated.

In asynchronous state, counting of framing errors and detection of remote alarm is stopped. AIS is automatically sent to the backplane interface (can be disabled by bit FMR2.DAIS).

Further on the updating of the registers RSW, RSP, RSA(8:4), RSA6S and RS(16:1) is halted (remote alarm indication, S_a/S_i-Bit access).

The resynchronization procedure starts automatically after reaching the asynchronous state. Additionally, it can be invoked user controlled by bit FMR0.FRS (force resynchronization, the FAS word detection is interrupted until the framer is in the asynchronous state. After that, resynchronization starts automatically).

Synchronous state is established after detecting:

- a correct FAS word in frame n,
- the presence of the correct service word (bit 2 = 1) in frame n + 1,
- a correct FAS word in frame n + 2.

If the service word in frame n + 1 or the FAS word in frame n + 2 or both are not found searching for the next FAS word starts in frame n + 2 just after the previous frame alignment signal.

Reaching the synchronous state causes a frame alignment recovery interrupt status ISR2.FAR if enabled. Undisturbed operation starts with the beginning of the next doubleframe.

4.2.2.3 A-Bit Access

If the QuadFALC detects a remote alarm indication in the received data stream the interrupt status bit ISR2.RA is set. With setting of bit XSW.XRA a remote alarm (RAI) is sent to the far end.

By setting FMR2.AXRA the QuadFALC automatically transmit the remote alarm bit = 1 in the outgoing data stream if the receiver detects a loss of frame alignment FRS0.LFA = 1. If the receiver is in synchronous state FRS0.LFA = 0 the remote alarm bit is reset.

*Note: The A-bit can be processed by the system interface. Setting bit TSWM.TRA enables transparency for the A-bit in transmit direction (refer to **Table 17**).*

4.2.2.4 S_a-Bit Access

As an extension for access to the S_a-bits through registers RSA(8:4)/XSA(8:4) an option is implemented to allow the usage of internal S_a-bit registers RSA(8:4)/XSA(8:4) in doubleframe format.

This function is enabled by setting FMR1.ENSA = 1 for the transmitter and FMR1.RFS(1:0) = 01 for the receiver. In this case the QuadFALC internally works with a 16-frame structure but no CRC multiframe alignment/generation is performed.

4.2.3 CRC-Multiframe (E1)

The multiframe structure shown in **Table 19** is enabled by setting bit: FMR2.RFS1/0 for the receiver and FMR1.XFS for the transmitter.

Multiframe	:	2 submultiframes = 2 × 8 frames
Frame alignment	:	refer to section Doubleframe Format
Multiframe alignment	:	bit 1 of frames 1, 3, 5, 7, 9, 11 with the pattern ’001011’
CRC bits	:	bit 1 of frames 0, 2, 4, 6, 8, 10, 12, 14
CRC block size	:	2048 bit (length of a submultiframe)
CRC procedure	:	CRC4, according to ITU-T G.704 and G.706

Table 19 CRC-Multiframe Structure (E1)

	Sub-Multiframe	Frame Number	Bits 1 to 8 of the Frame							
			1	**2**	**3**	**4**	**5**	**6**	**7**	**8**
Multiframe	I	0	C_1	0	0	1	1	0	1	1
		1	0	1	A	S_{a4}	S_{a5}	S_{a61}	S_{a7}	S_{a8}
		2	C_2	0	0	1	1	0	1	1
		3	0	1	A	S_{a4}	S_{a5}	S_{a62}	S_{a7}	S_{a8}
		4	C_3	0	0	1	1	0	1	1
		5	1	1	A	S_{a4}	S_{a5}	S_{a63}	S_{a7}	S_{a8}
		6	C_4	0	0	1	1	0	1	1
		7	0	1	A	S_{a4}	S_{a5}	S_{a64}	S_{a7}	S_{a8}
	II	8	C_1	0	0	1	1	0	1	1
		9	1	1	A	S_{a4}	S_{a5}	S_{a61}	S_{a7}	S_{a8}
		10	C_2	0	0	1	1	0	1	1
		11	1	1	A	S_{a4}	S_{a5}	S_{a62}	S_{a7}	S_{a8}
		12	C_3	0	0	1	1	0	1	1
		13	E*	1	A	S_{a4}	S_{a5}	S_{a63}	S_{a7}	S_{a8}
		14	C_4	0	0	1	1	0	1	1
		15	E*	1	A	S_{a4}	S_{a5}	S_{a64}	S_{a7}	S_{a8}

E: Spare bits for international use. Access to received information through bits RSP.RS13 and RSP.RS15. Transmission is enabled by bits XSP.XS13 and XSP.XS15. Additionally, automatic transmission for submultiframe error indication is selectable.

S_a: Spare bits for national use. Additionally, S_a-bit access through registers RSA(8:4) and XSA(8:4) is provided. HDLC-signaling in bits S_a(8:4) is selectable.

C_1 ... C_4: Cyclic redundancy check bits.

A: Remote alarm indication. Additionally, automatic transmission of the A-bit is selectable.

For transmit direction, contents of time slot 0 are additionally determined by the selected transparent mode.

Table 20 Transmit Transparent Mode (CRC Multiframe E1)

	Transmit Transparent Source for			
Enabled by	**Framing + CRC**	**A-Bit**	**S_a-Bits**	**E-Bits**
–	(int. gen.)	XSW.XRA[2)]	XSW.XY(4:0)[3)]	XSP.XS13/XS15[4)]
XSP.TT0	via pin XDI[1)]	via pin XDI	via pin XDI	via pin XDI
TSWM.TSIF	via pin XDI	XSW.XRA[1)]	XSW.XY(4:0)[2)]	(int. generated)
TSWM.TSIS	via pin XDI	XSW.XRA[1)]	XSW.XY(4:0)[2)]	via pin XDI
TSWM.TRA	(int. gen.)	via pin XDI	XSW.XY(4:0)[2)]	XSP.XS13/XS15[3)]
TSWM.TSA(8:4)	(int. gen.)	XSW.XRA[1)]	via pin XDI	XSP.XS13/XS15[3)]

1) pin XDI or XSIG or XFIFO buffer (signaling controller)

2) Automatic transmission of the A-bit is selectable

3) The S_a-bit register XSA(8:4) can be used optionally

4) Additionally, automatic transmission of submultiframe error indication is selectable

The CRC procedure is automatically invoked when the multiframe structure is enabled. CRC errors in the received data stream are counted by the 16-bit CRC Error Counter CEC (one error per submultiframe, maximum).

Additionally a CRC4 error interrupt status ISR0.CRC4 is generated if enabled by IMR0.CRC4.

All CRC bits of one outgoing submultiframe are automatically inverted in case a CRC error is flagged for the previous received submultiframe. This function is enabled by bit RC0.CRCI. Setting of bit RC0.XCRCI inverts the CRC bits before transmission to the distant end. The function of RC0.XCRCI and RC0.CRCI are logically ored.

4.2.3.1 Synchronization Procedure

Multiframe alignment is assumed to have been lost if doubleframe alignment has been lost (flagged on status bit FRS0.LFA). The rising edge of this bit causes an interrupt.

The multiframe resynchronization procedure starts when Doubleframe alignment has been regained which is indicated by an interrupt status bit ISR2.FAR. For Doubleframe synchronization refer to section Doubleframe Format. It is also be invoked by the user by setting

- bit FMR0.FRS for complete doubleframe **and** multiframe resynchronization
- bit FMR1.MFCS for multiframe resynchronization only.

The CRC checking mechanism is enabled after the first correct multiframe pattern has been found. However, CRC errors are not counted in asynchronous state.

In doubleframe asynchronous state, counting of framing errors, CRC4 bit errors and detection of remote alarm is stopped. AIS is automatically sent to the backplane interface (can be disabled by bit FMR2.DAIS). Further on the updating of the registers RSW, RSP, RSA(8:4), RSA6S and RS(16:1) is halted (remote alarm indication, S_a/S_i-bit access).

The multiframe synchronous state is established after detecting two correct multiframe alignment signals at an interval of $n \times 2$ ms (n = 1, 2, 3 ...). The loss of multiframe alignment flag FRS0.LMFA is reset. Additionally an interrupt status multiframe alignment recovery bit ISR2.MFAR is generated with the falling edge of bit FRS0.LMFA.

4.2.3.2 Automatic Force Resynchronization (E1)

In addition, a search for Doubleframe alignment is automatically initiated if two multiframe pattern with a distance of $n \times 2$ ms have not been found within a time interval of 8 ms after doubleframe alignment has been regained (bit FMR1.AFR). A new search for frame alignment is started just after the previous frame alignment signal.

4.2.3.3 Floating Multiframe Alignment Window (E1)

After reaching doubleframe synchronization a 8 ms timer is started. If a multiframe alignment signal is found during the 8 ms time interval the internal timer is reset to remaining 6 ms in order to find the next multiframe signal within this time. If the multiframe signal is not found for a second time, the interrupt status bit ISR0.T8MS is set. This interrupt usually occurs every 8 ms until multiframe synchronization is achieved.

4.2.3.4 CRC4 Performance Monitoring (E1)

In the synchronous state checking of multiframe pattern is disabled. However, with bit FMR2.ALMF an automatic multiframe resynchronization mode can be activated. If 915 out of 1000 errored CRC submultiframes are found then a false frame alignment is assumed and a search for doubleframe and multiframe pattern is initiated. The new search for frame alignment is started just after the previous basic frame alignment signal. The internal CRC4 resynchronization counter is reset when the multiframe synchronization has been regained.

4.2.3.5 Modified CRC4 Multiframe Alignment Algorithm (E1)

The modified CRC4 multiframe alignment algorithm allows an automatic interworking between framers with and without a CRC4 capability. The interworking is realized as it is described in ITU-T G.706 Appendix B.

If doubleframe synchronization is consistently present but CRC4 multiframe alignment is not achieved within 400 ms it is assumed that the distant end is initialized to doubleframe format. The CRC4/non-CRC4 interworking is enabled by FMR2.RFS1/0 = 11 and is activated only if the receiver has lost its synchronization. If doubleframe alignment (basic frame alignment) is established, a 400 ms timer and searching for multiframe alignment are started. A research for basic frame alignment is initiated if the CRC4 multiframe synchronization can not be achieved within 8 ms and is started just after the previous frame alignment signal. The research of the basic frame alignment is done in parallel and is independent of the synchronization procedure of the primary basic frame alignment signal. During the parallel search all receiver functions are based on the primary frame alignment signal, like framing errors, S_a-, S_i-, A-bits, ...). All subsequent multiframe searches are associated with each basic framing sequence found during the parallel search.

If the CRC4 multiframe alignment sequence was not found within the time interval of 400 ms, the receiver is switched into a non-CRC4 mode indicated by setting the bit FRS0.NMF (No Multiframing Found) and ISR2.T400MS. In this mode checking of CRC bits is disabled and the received E-bits are forced to low. The transmitter framing format is not changed. Even if multiple basic FAS resynchronizations have been established during the parallel search, the receiver is maintained to the initially determined primary frame alignment signal location.

However, if the CRC4-multiframe alignment can be achieved within the 400 ms time interval assuming a CRC4-to-CRC4 interworking, then the basic frame alignment sequence associated to the CRC4 multiframe alignment signal is chosen. If necessary, the primary frame alignment signal location is adjusted according to the multiframe alignment signal. The CRC4 performance monitoring is started if enabled by FMR2.ALMF and the received E-bits are processed in accordance to ITU-T G.704.

Switching into the doubleframe format (non-CRC4) mode after 400 ms can be disabled by setting of FMR3.EXTIW. In this mode the QuadFALC continues to search for multiframing. In the interworking mode setting of bit FMR1.AFR is not allowed.

4.2.3.6 A-Bit Access (E1)

If the QuadFALC detects a remote alarm indication (bit 2 in TS0 not containing the FAS word) in the received data stream the interrupt status bit ISR2.RA is set. With the deactivation of the remote alarm the interrupt status bit ISR2.RAR is generated.

By setting FMR2.AXRA the QuadFALC automatically transmits the remote alarm bit = 1 in the outgoing data stream if the receiver detects a loss of frame alignment (FRS0.LFA = 1). If the receiver is in synchronous state (FRS0.LFA = 0), the remote alarm bit is reset in the outgoing data stream.

Additionally, if bit FMR3.EXTIW is set and the multiframe synchronous state can not be achieved within 400 ms after finding the primary basic framing, the A-bit is transmitted active high to the remote end until the multiframing is found.

*Note: The A-bit can be processed by the system interface. Setting bit TSWM.TRA enables transparency for the A-bit in transmit direction (refer to **Table 19**).*

4.2.3.7 S_a-Bit Access (E1)

Due to signaling procedures using the five S_a-bits (S_{a4} to S_{a8}) of every other frame of the CRC multiframe structure, three possibilities of access by the microprocessor are implemented.

- The standard procedure allows reading/writing the S_a-bit registers RSW, XSW without further support. The S_a-bit information is updated every other frame.
- The advanced procedure, enabled by bit FMR1.ENSA, allows reading/writing the S_a-bit registers RSA(8:4), XSA(8:4).

A transmit or receive multiframe begin interrupt (ISR0.RMB or ISR1.XMB) is provided.

Registers RSA(8:4) contains the service word information of the previously received CRC-multiframe or 8 doubleframes (bit slots 4 to 8 of every service word). These registers are updated with every multiframe begin interrupt ISR0.RMB.

With the transmit multiframe begin an interrupt ISR1.XMB is generated and the contents of these registers (XSA(8:4)) is copied into shadow registers. The contents is subsequently sent out in the service words of the next outgoing CRC multiframe (or every doubleframe) if none of the time slot 0 transparent modes is enabled. The transmit multiframe begin interrupt XMB request that these registers issue should be serviced. If requests for new information are ignored, the current contents is repeated.

- The extended access through the receive and transmit FIFOs of the signaling controller. In this mode it is possible to transmit/receive a HDLC frame or a transparent bit stream in any combination of the S_a-bits. Enabling is done by setting of bit CCR1.EITS and the corresponding bits XC0.SA(8:4)E/TSWM.TSA(8:4) and resetting of registers TTR(4:1), RTR(4:1) and FMR1.ENSA. The access to and from the FIFOs is supported by ISR0.RME,RPF and ISR1.XPR,ALS.

S_a6-Bit Detection according to ETS 300233

Four consecutive received S_a6-bits are checked for the combinations defined by ETS 300233. The QuadFALC detects the following fixed S_a6-bit combinations: SA61, SA62, SA63, SA64 = 1000, 1010, 1100, 1110, 1111. All other possible 4-bit combinations are grouped to status “X”.

A valid S_a6-bit combination must occur three times in a row. The corresponding status bit in register RSA6S is set. Register RSA6S is of type “clear on read”. Any status change of the S_a6-bit combinations causes an interrupt (ISR0.SA6SC).

During the basic frame asynchronous state update of register RSA6S and interrupt status ISR0.SA6SC is disabled. In multiframe format the detection of the S_a6-bit combinations can be done either synchronously or asynchronously to the submultiframe (FMR3.SA6SY). In synchronous detection mode updating of register RSA6S is done in the multiframe synchronous state (FRS0.LMFA = 0). In asynchronous detection mode updating is independent of the multiframe synchronous state.

S_a6-Bit Error Indication Counters

The S_a6-bit error indication counter CRC2L/H (16 bits) counts the received S_a6-bit sequence 0001 or 0011 in every CRC submultiframe. In the primary rate access digital section this counter option gives information about CRC errors reported from the TE by the S_a6 bit. Incrementing is only possible in the multiframe synchronous state. The S_a6-bit error indication counter CRC3L/H (16 bits) counts the received S_a6-bit sequence 0010 or 0011 in every CRC submultiframe. In the primary rate access digital section this counter option gives information about CRC errors detected at T-reference point and reporting them by the S_a6-bit. Incrementing is only possible in the multiframe synchronous state.

4.2.3.8 E-Bit Access (E1)

Due to signaling requirements, the E-bits of frame 13 and frame 15 of the CRC multiframe can be used to indicate received errored submultiframes:

Submultiframe I statusE-bit located in frame 13
Submultiframe II statusE-bit located in frame 15

no CRC error: E = 1; CRC error:E = 0

Standard Procedure

After reading the submultiframe error indication RSP.SI1 and RSP.SI2, the microprocessor has to update the contents of register XSP (XS13, XS15). Access to these registers has to be synchronized on transmit or receive multiframe begin interrupts (ISR0.RMB or ISR1.XMB).

Automatic Mode

In the multiframe synchronous state the E-bits are processed according to ITU-T G.704 independently of bit XSP.EBP (E-bit polarity selection).

By setting bit XSP.AXS status information of received submultiframes is automatically inserted in the E-bit position of the outgoing CRC multiframe without any further interventions of the microprocessor.

In the doubleframe and multiframe asynchronous state the E-bits are set or cleared, depending on the setting of bit XSP.EBP.

Submultiframe Error Indication Counter

The EBC (E-Bit) counter EBCL/H (16 bits) counts zeros in the E-bit position of frame 13 and 15 of every received CRC multiframe. This counter option gives information about the outgoing transmit PCM line if the E-bits are used by the remote end for submultiframe error indication. Incrementing is only possible in the multiframe synchronous state.

*Note: E-bits can be processed by the system interface. Setting bit TSWM.TSIS enables transparency for E-bits in transmit direction (refer to **Table 19**).*

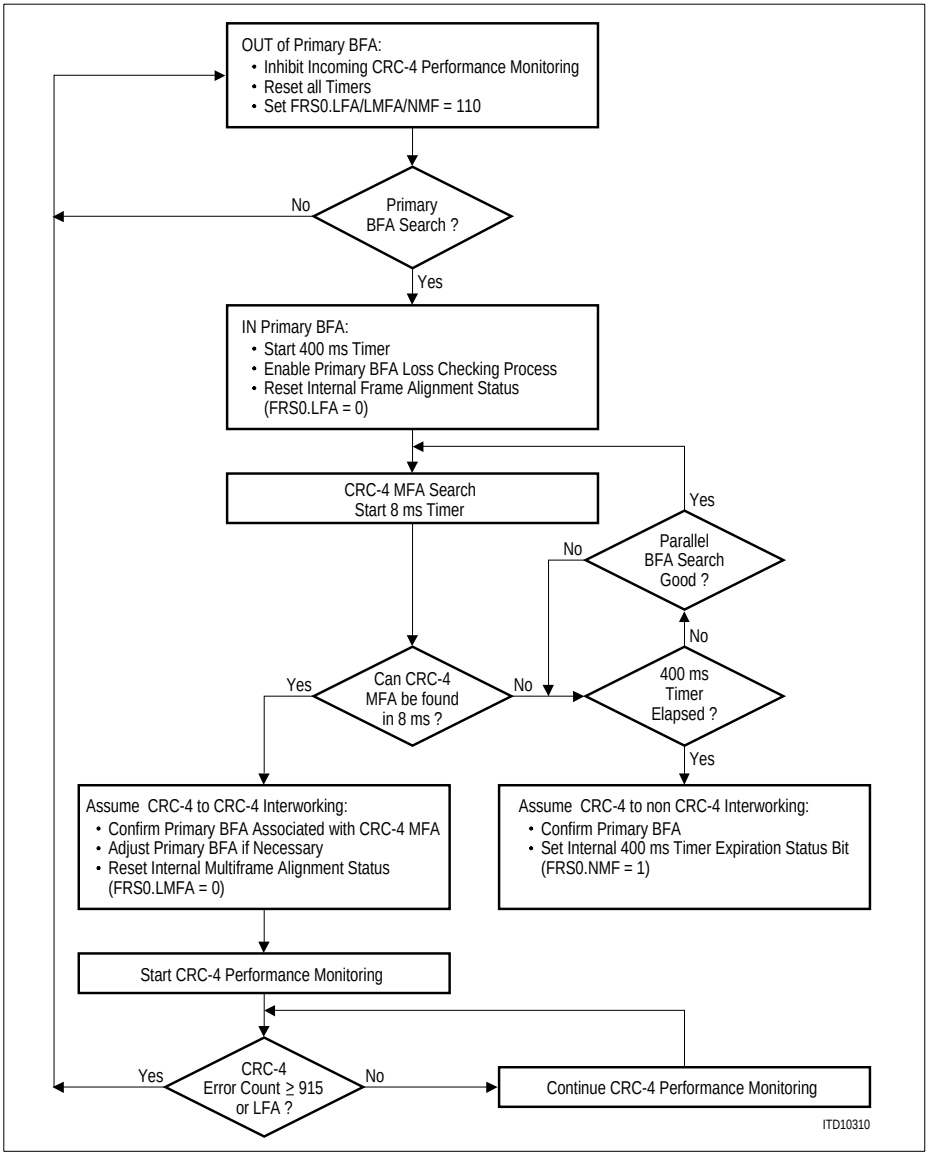


Figure 26 CRC4 Multiframe Alignment Recovery Algorithms (E1)

4.3 Additional Receive Framer Functions (E1)

4.3.1 Error Performance Monitoring and Alarm Handling

- Alarm Indication Signal: Detection and recovery is flagged by bit FRS0.AIS and ISR2.AIS. Transmission is enabled by bit FMR1.XAIS.
- Loss of Signal: Detection and recovery is flagged by bit FRS0.LOS and ISR2.LOS.
- Remote Alarm Indication: Detection and release is flagged by bit FRS0.RRA, RSW.RRA and ISR2.RA/RAR. Transmission is enabled by bit XSW.XRA.
- AIS in time slot 16: Detection and release is flagged by bit FRS1.TS16AIS and ISR3.AIS16. Transmission is enabled by writing all ones in registers XS(16:1).
- LOS in time slot 16: Detection and release is flagged by bit FRS1.TS16LOS. Transmission is enabled by writing all zeros in registers XS(16:1).
- Remote Alarm in time slot 16: Detection and release is flagged by bit FRS1.TS16RA and ISR3.RA16. Transmission is enabled by bit XS1.2.
- Transmit Line Shorted: Detection and release is flagged by bit FRS1.XLS and ISR1.XLSC.
- Transmit Ones Density: Detection and release is flagged by bit FRS1.XLO and ISR1.XLSC.

Table 21 Summary of Alarm Detection and Release (E1)

Alarm	Detection Condition	Clear Condition
Loss of Signal (LOS)	no transitions (logical zeros) in a programmable time interval of 16 to 4096 consecutive pulse periods. Programmable receive input signal threshold	programmable number of ones (1 to 256) in a programmable time interval of 16 to 4096 consecutive pulse periods. A one is a signal with a level above the programmed threshold.
Alarm Indication Signal (AIS)	FMR0.ALM = 0: less than 3 zeros in 250 µs and loss of frame alignment declared FMR0.ALM = 1: less than 3 zeros in each of two consecutive 250-µs periods	FMR0.ALM = 0: more than 2 zeros in 250 µs FMR0.ALM = 1: more than 2 zeros in each of two 500-µs periods
Remote Alarm (RRA)	bit 3 = 1 in time slot 0 not containing the FAS word	set conditions no longer detected.
Remote Alarm in time slot 16 (TS16RA)	Y-bit = 1 received in CAS multiframe alignment word	Y-bit = 0 received in CAS multiframe alignment word

Table 21 Summary of Alarm Detection and Release (E1) (cont'd)

Alarm	Detection Condition	Clear Condition
Loss of Signal in time slot 16 (TS16LOS)	all zeros for at least 16 consecutively received time slots 16	receiving a one in time slot 16
Alarm Indication Signal in time slot 16 (TS16AIS)	time slot 16 containing less than 4 zeros in each of two consecutive CAS multiframes periods	time slot 16 containing more than 3 zeros in one CAS multiframe
Transmit Line Short (XLS)	more than 3 pulse periods with highly increased transmit line current on XL1/2	transmit line current limiter inactive
Transmit Ones Density (XLO)	32 consecutive zeros in the transmit data stream on XL1/2	Cleared with each transmitted pulse

4.3.2 Auto Modes

- Automatic remote alarm access
  If the receiver has lost its synchronization a remote alarm can be sent automatically, if enabled by bit FMR2.AXRA to the distant end. The remote alarm bit is set automatically in the outgoing data stream, if the receiver is in asynchronous state (FRS0.LFA bit is set). In synchronous state the remote alarm bit is removed.
- Automatic E-bit access
  By setting bit XSP.AXS status information of received submultiframes is automatically inserted at the E-bit position of the outgoing CRC Multiframe without any further interventions of the microprocessor.
- Automatic AIS to system interface
  In asynchronous state the synchronizer enforces an AIS to the receive system interface automatically. However, received data can be switched through transparently, if bit FMR2.DAIS is set.
- Automatic clock source switching
  In slave mode (LIM0.MAS = 0) the DCO-R synchronizes to the recovered route clock. In case of loss of signal (LOS) the DCO-R switches to Master mode automatically. If bit CMR1.DCS is set, automatic switching from RCLK to SYNC is disabled.
- Automatic freeze signaling:
  Updating of the received signaling information is controlled by the freeze signaling status. The freeze signaling status is automatically activated if a loss of signal or a loss of CAS multiframe alignment or a receive slip occurs. The internal signaling buffer

RS(16:1) is frozen. Optionally automatic freeze signaling is disabled by setting bit SIC3.DAF.

4.3.3 Error Counter

The QuadFALC offers six error counters where each of them has a length of 16 bit. They record code violations, framing bit errors, CRC4-bit errors and CRC4 error events which are flagged in the different S_a6-bit combinations or the number of received multiframes in asynchronous state or the change of frame alignment (COFA). Counting of the multiframes in the asynchronous state and the COFA parameter is done in a 6/2 bit counter and is shared with CEC3L/H. Each of the error counters is buffered. Buffer updating is done in two modes:

- one second accumulation
- on demand by handshake with writing to the DEC register

In the one second mode an internal/external one second timer updates these buffers and resets the counter to accumulate the error events in the next one-second period. The error counter can not overflow. Error events occurring during an error counter reset are not lost.

4.3.4 Errored Second

The QuadFALC supports the error performance monitoring by detecting the following alarms or error events in the received data:
framing errors, CRC errors, code violations, loss of frame alignment, loss of signal, alarm indication signal, E-bit error, receive and transmit slips.
With a programmable interrupt mask register ESM all these alarms or error events can generate an errored second interrupt (ISR3.ES) if enabled.

4.3.5 Second Timer

Additionally a one second timer interrupt can be generated internally to indicate that the enabled alarm status bits or the error counters have to be checked. The one second timer signal is output on port SEC/FSC (GPC1.CSFP1/0). Optionally synchronization to an external second timer is possible which has to be provided at pin SEC/FSC. Selecting the external second timer is done with GCR.SES. Refer also to register GPC1 for input/output selection.

4.3.6 In-Band Loop Generation and Detection

The QuadFALC generates and detects a framed or unframed in-band loop up/activate and down/deactivate pattern with bit error rates up to 10^{-2}. Framed or unframed in-band loop code is selected by LCR1.FLLB. Replacing transmit data with the in-band loop codes is done by programming FMR3.XLD/XLU.
The QuadFALC also offers the ability to generate and detect a flexible in-band loop up

and loop down pattern (LCR1.LLBP = 1). The loop up and loop down pattern is individually programmable from 2 to 8 bit in length (LCR1.LAC1/0 and LCR1.LDC1/0). Programming of loop codes is done in registers LCR2 and LCR3.
Status and interrupt status bits inform the user whether loop up or loop down code has been detected.

4.3.7 Time Slot 0 Transparent Mode

The transparent modes are useful for loopbacks or for routing data unchanged through the QuadFALC.

In receive direction, transparency for ternary or dual/single rail unipolar data is always achieved if the receiver is in the synchronous state. In asynchronous state data is transparently switched through if bit FMR2.DAIS is set. However, correct time slot assignment can not be guaranteed due to missing frame alignment between line and system side.
Setting of bit LOOP.RTM disconnects control of the internal elastic store from the receiver. The elastic buffer is now in a “free running” mode without any possibility to update the time slot assignment to a new frame position in case of resynchronization of the receiver. Together with FMR2.DAIS this function can be used to realize undisturbed transparent reception.

Transparency in transmit direction can be achieved by activating the time slot 0 transparent mode (bit XSP.TT0 or TSWM.(7:0)). If XSP.TT0 = 1 all internal information of the QuadFALC (framing, CRC, S_a/S_i-bit signaling, remote alarm) is ignored. With register TSWM the S_i-bits, A-bit or the S_a(8:4) bits can be enabled selectively to send data transparently from port XDI to the far end. For complete transparency the internal signaling controller, idle code generation and AIS alarm generation, single channel and payload loop back have to be disabled.

4.4 Transmit Path in E1 Mode

4.4.1 Transmitter (E1)

The serial bit stream is processed by the transmitter which has the following functions:

- Frame/multiframe synthesis of one of the two selectable framing formats
- Insertion of service and data link information
- AIS generation (Alarm indication signal)
- Remote alarm generation
- CRC generation and insertion of CRC bits
- CRC bits inversion in case of a previously received CRC error
- Idle code generation per DS0

The frame/multiframe boundaries of the transmitter can be externally synchronized by using the $\overline{\text{SYPX}}$/XMFS pin. Any change of the transmit time slot assignment

subsequently produces a change in the framing bit positions on the line side. This feature is required if signaling and service bits are routed through the switching network and are inserted in transmit direction by the system interface.

In loop-timed configuration (LIM2.ELT = 1) disconnecting the control of the transmit system highway from the transmitter is done by setting XSW.XTM. The transmitter is now in a free running mode without any possibility to update the multiframe position in case of changing the transmit time slot assignment. The framing bits are generated independently of the transmit system interface. For proper operation the transmit elastic buffer size should be programmed to 2 frames.

The contents of selectable time slots can be overwritten by the pattern defined by register IDLE. The selection of “idle channels” is done by programming the four-byte registers ICB(4:1).

4.4.2 Transmit Line Interface (E1)

The analog transmitter transforms the unipolar bit stream to ternary (alternate bipolar) return to zero signals of the appropriate programmable shape. The unipolar data is provided by the digital transmitter.

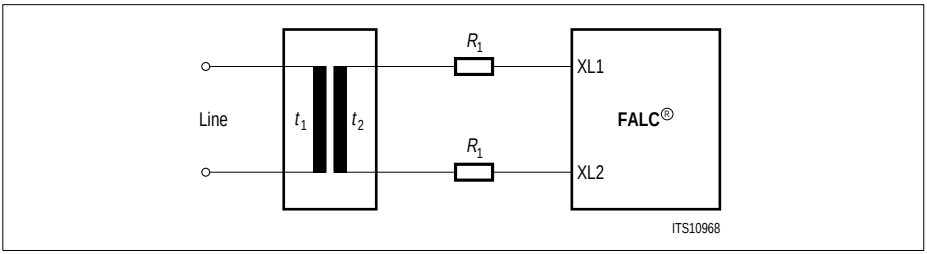


Figure 27 Transmitter Configuration (E1)

Table 22 Recommended Transmitter Configuration Values (E1)

Parameter	Characteristic Impedance [Ω]	
	120	75
R_1 (± 1%) [Ω]	7.5[1)]	7.5[1)]
t2 : t1	1 : 2.4	1 : 2.4

[1)] This value refers to an ideal transformer without any parasitics. Any transformer resistance or other parasitic resistances have to be taken into account when calculating the final value of the output serial resistors.

Similar to the receive line interface three different data types are supported:

- Ternary Signal
  Single rail data is converted into a ternary signal which is output on pins XL1 and XL2. The HDB3 and AMI line code is employed. Selected by FMR0.XC1/0 and LIM1.DRS = 0.
- Dual rail data PCM(+), PCM(–) at multifunction ports XDOP/XDON with 50% or 100% duty cycle and with programmable polarity. Line coding is done in the same way as in ternary interface mode. Selected by FMR0.XC1/0 and LIM1.DRS = 1.
- Unipolar data on port XOID is transmitted either in NRZ (Non Return to Zero) with 100% duty cycle or in CMI (Code Mark Inversion or known as 1T2B) Code with or without (FMR3.CMI) preprocessed HDB3 coding to a fibre optical interface. Clocking off data is done with the rising edge of the transmit clock XCLK (2048 kHz) and with a programmable polarity. Selection is done by FMR0.XC1 = 0 and LIM1.DRS = 1.

4.4.3 Transmit Jitter Attenuator (E1)

The transmit jitter attenuator DCO-X circuitry generates a 'jitter free' transmit clock and meets the following requirements: ITU-T I.431, G. 703, G. 736 to 739, G.823 and ETSI TBR12/13. The DCO-X circuitry works internally with the same high frequency clock as the receive jitter attenuator. It synchronizes either to the working clock of the transmit backplane interface or the clock provided on pin TCLK or the receive clock RCLK (remote loop/loop-timed). The DCO-X attenuates the incoming clock jitter starting at 2 Hz with 20 dB per decade fall off. With the jitter attenuated clock, which is directly depending on the phase difference of the incoming clock and the jitter attenuated clock, data is read from the transmit elastic buffer (2 frames) or from the JATT buffer (2 frames, remote loop). Wander with a jitter frequency below 2 Hz is passed transparently.

The DCO-X accepts gapped clocks which are used in ATM or SDH/SONET applications. The jitter attenuated clock is output by pin XCLK.

In case of missing clock on pin SCLKX the DCO-X centers automatically, if selected by bit CMR2.DCOXC = 1.

The transmit jitter attenuator can be disabled. In that case data is read from the transmit elastic buffer with the clock sourced by pin TCLK (2.048 or 8.192 MHz). Synchronization between SCLKX and TCLK has to be done externally.

In the loop-timed clock configuration (LIM2.ELT) the DCO-X circuitry generates a transmit clock which is frequency synchronized on RCLK. In this configuration the transmit elastic buffer has to be enabled.

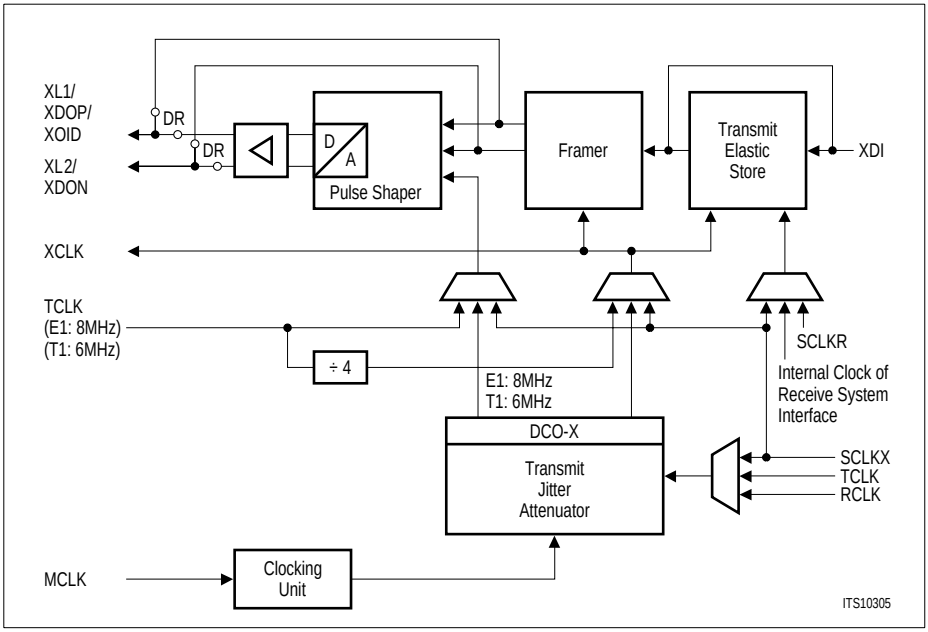


Figure 28 Transmit Clock System (E1)

Note: DR = Dual Rail Interface
DCO-X Digital Controlled Oscillator Transmit

4.4.4 Transmit Elastic Buffer (E1)

The received bit stream from pin XDI is optionally stored in the transmit elastic buffer. The memory is organized as the receive elastic buffer. The functions are also equal to the receive side. Programming of the transmit buffer size is done by SIC1.XBS1/0:

- XBS1/0 = 00: Bypass of the transmit elastic buffer
- XBS1/0 = 01: one frame buffer or 256 bits
  Maximum of wander amplitude (peak-to-peak): 100 UI (1 UI = 488 ns)
  average delay after performing a slip: 128 bits
- XBS1/0 = 10: two frame buffer or 512 bits
  Maximum of wander amplitude: 190 UI
  average delay after performing a slip: 1 frame or 256 bits
- XBS1/0 = 11: short buffer or 92 bits:
  Maximum of wander amplitude: 18 µs
  average delay after performing a slip: 46 bits

The functions of the transmit buffer are:

- Clock adaptation between system clock (SCLKX) and internally generated transmit route clock (XCLK).
- Compensation of input wander and jitter.
- Frame alignment between system frame and transmit route frame
- Reporting and controlling of slips

Writing of received data from XDI is controlled by SCLKX/R and $\overline{\text{SYPX}}$/XMFS in combination with the programmed offset values for the transmit time slot/clock slot counters. Reading of stored data is controlled by the clock generated by DCO-X circuitry or the externally generated TCLK and the transmit framer. With the dejittered clock data is read from the transmit elastic buffer and are forwarded to the transmitter. Reporting and controlling of slips is done according to the receive direction. Positive/negative slips are reported in interrupt status bits ISR4.XSP and ISR4.XSN. If the transmit buffer is bypassed data is directly transferred to the transmitter.

The following table gives an overview of the transmit buffer operating modes.

Table 23 Transmit Buffer Operating Modes (E1)

SIC1.XBS(1:0)	Buffer Size	TS Offset programming	Slip performance
00	bypass	enabled	no
11	short buffer	enabled	yes
01	1 frame	enabled	yes
10	2 frames	enabled	yes

4.4.5 Programmable Pulse Shaper (E1)

The analog transmitter includes a programmable pulse shaper to satisfy the requirements of ITU-T I.431. The amplitude and shape of the transmit pulses are completely programmable by registers XPM(2:0). For mote details refer to transmit pulse mask programming on **Page 245**.

The transmitter requires an external step up transformer to drive the line.

4.4.6 Transmit Line Monitor (E1)

The transmit line monitor compares the transmit line current on XL1 and XL2 with an on-chip transmit line current limiter. The monitor detects faults on the primary side of the transformer indicated by a highly increased transmit line current (more than 120 mA for at least 3 consecutive pulses sourced by V_{DDX}[1)]) and protects the device from damage by setting the transmit line driver XL1/2 into high impedance state automatically (if enabled by XPM2.DAXLT = 0). The current limiter checks the actual current value of

1) shorts between XL1 or XL2 and V_{DDX} are not detected

XL1/2 and if the transmit line current drops below the detection limit the high impedance state is cleared.

Two conditions are detected by the monitor: transmit line ones density (more than 31 consecutive zeros) indicated by FRS1.XLO and transmit line high current indicated by FRS1.XLS. In both cases a transmit line monitor status change interrupt is provided.

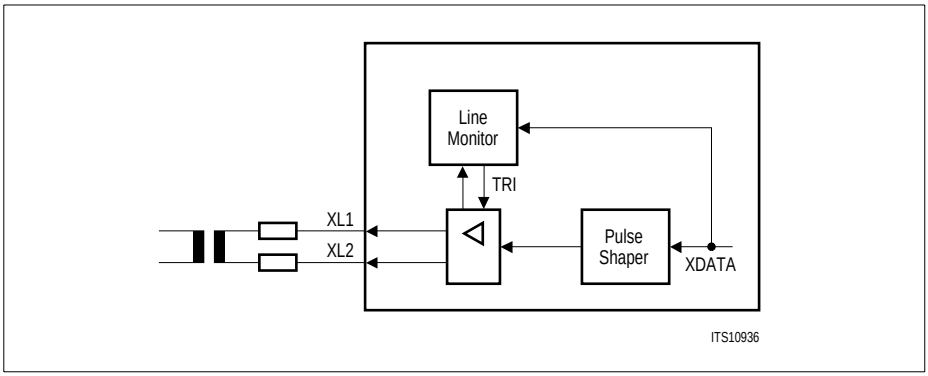


Figure 29 Transmit Line Monitor Configuration (E1)

4.4.7 Transmit Signaling Controller (E1)

Similar to the receive signaling controller the same signaling methods and the same time slot assignment is provided. The QuadFALC performs the following signaling and data link methods.

4.4.7.1 HDLC or LAPD access

The transmit signaling controller of the QuadFALC performs the flag generation, CRC generation, zero-bit stuffing and programmable idle code generation. Buffering of transmit data is done in the 64 byte deep XFIFO. The signaling information is internally multiplexed with the data applied to port XDI or XSIG.
In signaling controller transparent mode, fully transparent data transmission without HDLC framing is performed. Optionally the QuadFALC supports the continuous transmission of the XFIFO contents.
The QuadFALC offers the flexibility to insert data during certain time slots. Any combinations of time slots can be programmed separately for the receive and transmit direction.

4.4.7.2 Support of Signaling System #7

The HDLC controller supports the signaling system #7 (SS7) which is described in ITU-Q.703. The following description assumes, that the reader is familiar with the SS7 protocol definition.

SS7 support must be activated by setting the MODE register. Data stored in the transmit FIFO (XFIFO) is sent automatically. The SS7 protocol is supported by the following hardware features in transmit direction:

- transmission of flags at the beginning of each Signaling Unit
- bit stuffing (zero insertion)
- calculation of the CRC16 checksum:
  The transmitter adds the checksum to each Signaling Unit.

Each Signaling Unit written to the transmit FIFO (XFIFO, 2×32 bytes) is sent once or repeatedly including flags, CRC checksum and stuffed bits. After e.g. an MSU has been transmitted completely, the QuadFALC optionally starts sending of FISUs containing the forward sequence number (FSN) and the backward sequence number (BSN) of the previously transmitted Signaling Unit. Setting bit CCR5.AFX causes Fill In Signaling Units (FISUs) to be sent continuously, if no HDLC or Signaling Unit (SU) is to be transmitted from XFIFO. During update of XFIFO, automatic transmission is interrupted and resumed after update is completed. The internally generated FISUs contain FSN and BSN of the last transmitted Signaling Unit written to XFIFO.

Using CMDR.XREP = 1, the contents of XFIFO can be sent continuously. Clearing of CMDR.XRES/SRES stops the automatic repetition of transmission. This function is also available for HDLC frames, so no flag generation, CRC byte generation and bit stuffing is necessary.
Example: After an MSU has been sent repetitively and XREP has been cleared, FISUs are sent automatically.

4.4.7.3 S_a-Bit Access (E1)

The QuadFALC supports the S_a-bit signaling of time slot 0 of every other frame as follows:

- the access through register XSW
- the access through registers XSA(8:4), capable of storing the information for a complete multiframe
- the access through the 64 byte deep XFIFO of the signaling controller

This S_a-bit access gives the opportunity to transparent a bit stream as well as HDLC frames where the signaling controller automatically processes the HDLC protocol. Any combination of S_a-bits which shall be inserted in the outgoing data stream can be selected by XC0.SA(8:4).

4.4.7.4 Channel Associated Signaling CAS (E1, serial mode)

In external signaling mode (serial mode) the signaling data received on port XSIG is sampled with the working clock of the transmit system interface (SCLKX) in combination with the transmit synchronization pulse ($\overline{SYPX}$). Data on XSIG is latched in the bit positions 5 to 8 per time slot, bits 1 to 4 are ignored. Time slots 0 and 16 are sampled completely (bit 1 to 8). The received CAS multiframe is inserted frame aligned into the data stream on XDI and must be valid during the last frame of a multiframe if CRC4/multiframe mode is selected. The CAS multiframe is aligned to the CRC4-multiframe; other frames are ignored. Data sourced by the internal signaling controller (microprocessor access mode) overwrites the external signaling data.

If the QuadFALC is configured for no signaling, the system interface data stream passes the QuadFALC undisturbedly.

Note: CAS data on XSIG is read in the last frame of a multiframe only and ignored in all other frames.

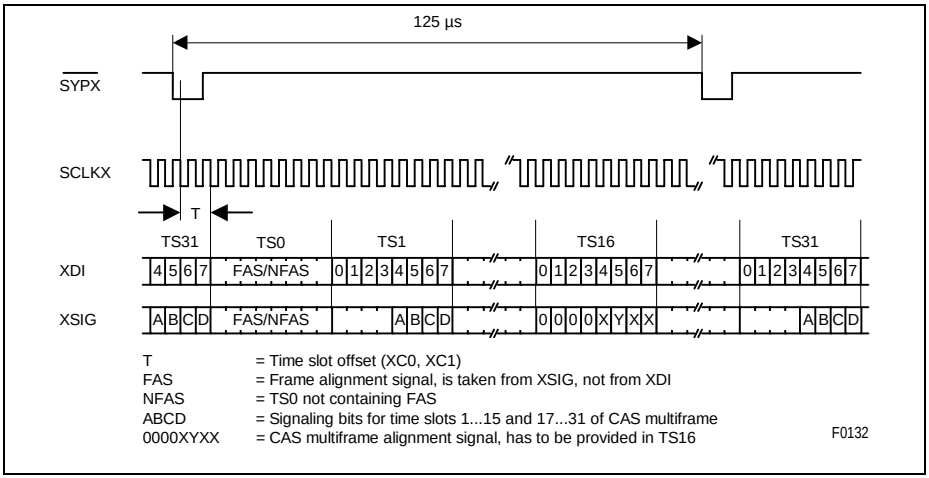


Figure 30 2.048 MHz Transmit Signaling Highway (E1)

4.4.7.5 Channel Associated Signaling CAS (E1, µP access mode)

Transmit data stored in registers XS(16:1) is transmitted on a multiframe boundary in time slot 16. The signaling controller inserts the bit stream either on the transmit line side or, if external signaling is enabled, on the transmit system side using pin function XSIG. Data sourced by the internal signaling controller overwrites the external signaling data.

If the QuadFALC is configured for no signaling, the system interface data stream passes the QuadFALC undisturbedly.

4.5 System Interface in E1 Mode

The QuadFALC offers a flexible feature for system designers where for transmit and receive direction different system clocks and system pulses are necessary. The interface to the receive system highway is realized by two data buses, one for the data RDO and one for the signaling data RSIG. The receive highway is clocked by pin SCLKR, while the interface to the transmit system highway is independently clocked by pin SCLKX. The frequency of these working clocks and the data rate of 2.048/4.096/8.192/16.384 Mbit/s for the receive and transmit system interface is programmable by SIC1.SSC1/0, and SIC1.SSD1, FMR1.SSD0. Selectable system clock and data rates and their valid combinations are shown in the table below

Table 24 System Clocking and Data Rates (E1)

System Data Rate	Clock Rate 2.048 MHz	Clock Rate 4.096 MHz	Clock Rate 8.192 MHz	Clock Rate 16.384 MHz
2.048 Mbit/s	x	x	x	x
4.096 Mbit/s	--	x	x	x
8.192 Mbit/s	--	--	x	x
16.384 Mbit/s	--	--	--	x

x = valid, -- = invalid

Generally the data or marker on the system interface are clocked off or latched on the rising or falling edge (SIC3.RESR/X) of the SCLKR/X clock. Some clocking rates allow transmission of time slots in different channel phases. Each channel phase which shall be active on ports RDO, XDI, RP(A to D) and XP(A to D) is programmable by SIC2.SICS(2:0), the remaining channel phases are cleared or ignored.
The signals on pin $\overline{\text{SYPR}}$ together with the assigned time slot offset in register RC0 and RC1 define the beginning of a frame on the receive system highway.The signal on pin $\overline{\text{SYPX}}$ or XMFS together with the assigned time slot offset in register XC0 and XC1 define the beginning of a frame on the transmit system highway.

Adjusting the frame begin (time slot 0, bit 0) relative to $\overline{\text{SYPR/X}}$ or XMFS is possible in the range of 0 to 125 µs. The minimum shift of varying the time slot 0 begin can be programmed between 1 bit and 1/8 bit depending of the system clocking and data rate, e.g. with a clocking/data rate of 2.048 MHz shifting is done bit by bit, while running the QuadFALC with 16.384 MHz and 2.048 Mbit/s data rate it is done by 1/8 bit.

A receive frame marker RFM can be activated during any bit position of the entire frame. Programming is done with registers RC1/0. The pin function RFM is selected by PC(4:1).RPC(2:0) = 001. The RFM selection disables the internal time slot assigner, no offset programming is performed. The receive frame marker is active high for one

2.048 MHz cycle and is clocked off with the rising or falling edge of the clock which is in/output on port SCLKR (see SIC3.RESR/X).

Compared to the receive path the inverse functions are performed for the transmit direction.

The interface to the transmit system highway is realized by two data buses, one for the data XDI and one for the signaling data XSIG. The time slot assignment is equivalent to the receive direction.

Latching of data is controlled by the system clock (SCLKX) and the synchronization pulse ($\overline{\text{SYPX}}$/XMFS) in combination with the programmed offset values for the transmit time slot/clock slot counters XC1/0. The frequency of the working clock of 2.048/4.096/8.192/16.384 MHz for the transmit system interface is programmable by SIC1.SSC1/0. Refer also to**Table 24**.

The received bit stream on ports XDI and XSIG can be multiplexed internally on a time slot basis, if enabled by SIC3.TTRF = 1. The data received on port XSIG can be sampled if the transmit signaling marker XSIGM is active high. Data on port XDI is sampled if XSIGM is low for the corresponding time slot. Programming the XSIGM marker is done with registers TTR(4:1).

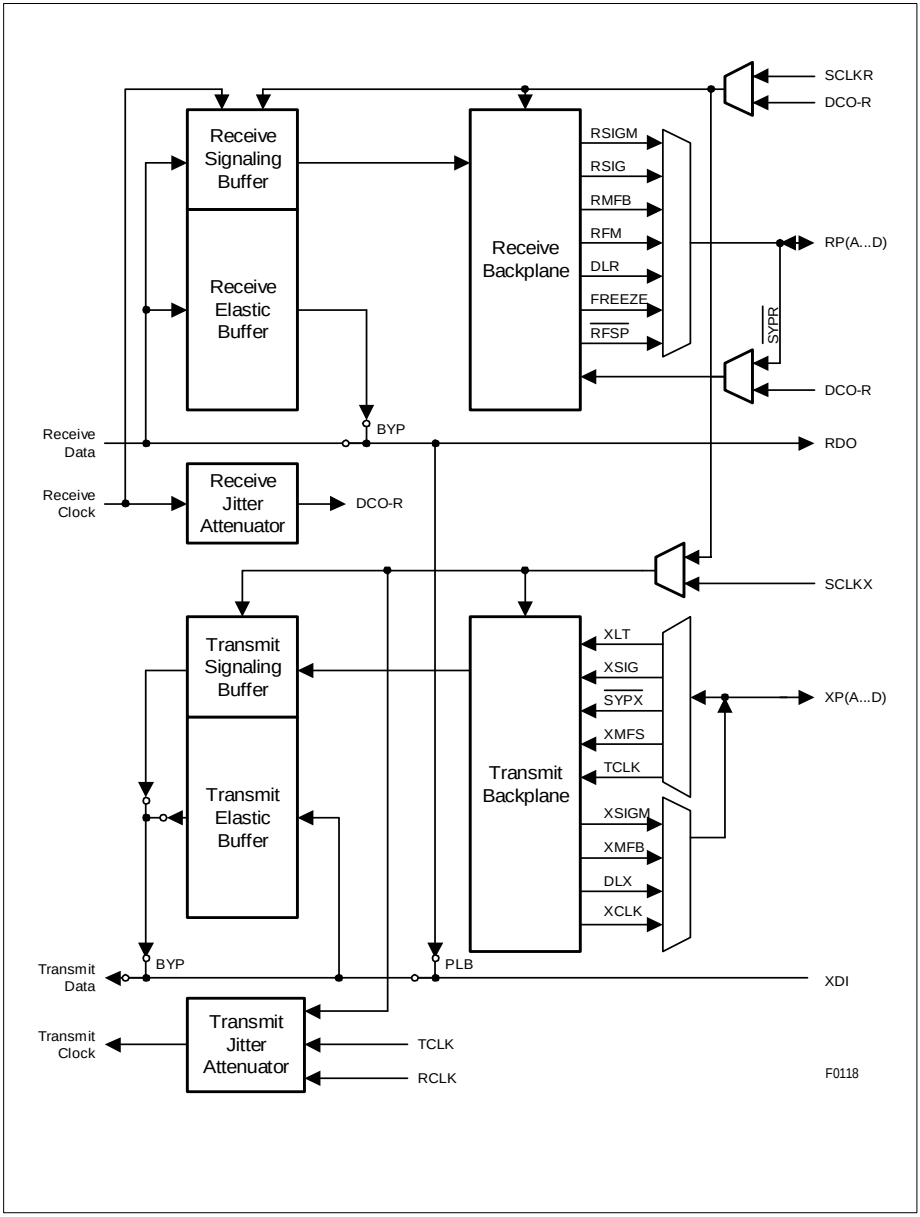


Figure 31 System Interface (E1)

4.5.1 Receive System Interface (E1)

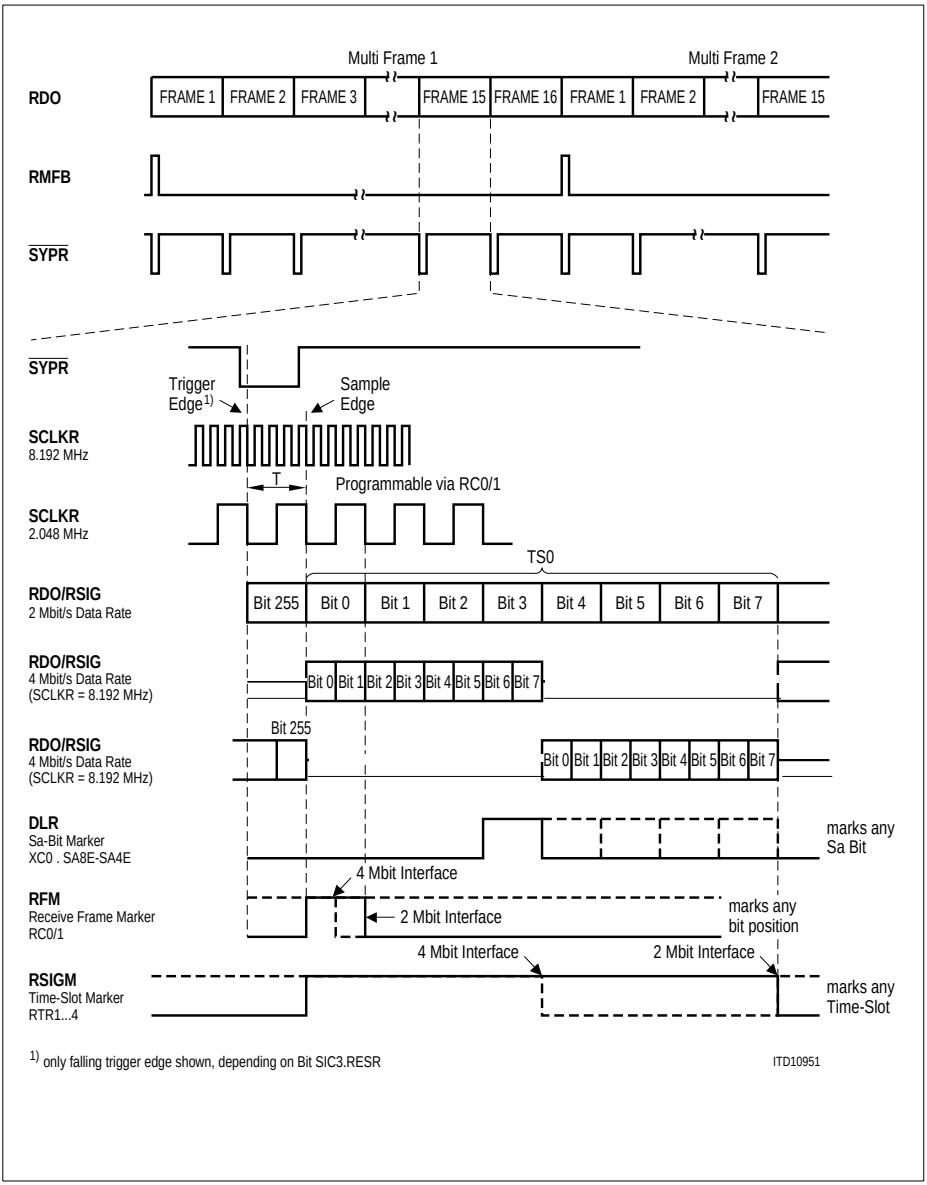


Figure 32 Receive System Interface Clocking (E1)

4.5.1.1 Receive Offset Programming

Depending on the selection of the synchronization signals ($\overline{\text{SYPR}}$ or RFM), different calculation formulas are used to define the position of the synchronization pulses. These formulas are given below, see **Figure 33** to **Figure 36** for explanation. The pulse length of $\overline{\text{SYPR}}$ and RFM is always the basic E1 bit width (488 ns), independent of the selected system highway clock and data frequency.

$\overline{\text{SYPR}}$ Offset Calculation

T: Time between beginning of $\overline{\text{SYPR}}$ pulse and beginning of next frame (time slot 0, bit 0), measured in number of SCLKR clock intervals
maximum delay: $T_{max} = (256 \times SC/SD) - 1$

SD: Basic data rate, 2.048 Mbit/s

SC: System clock rate; 2.048, 4.096, 8.192, or 16.384 MHz

X: Programming value to be written to registers RC0 and RC1 (see **Page 243**).

$0 \le T \le 4$: $X = 4 - T$
$5 \le T \le T_{max}$: $X = 2052 - T$

RFM Offset Calculation

MP: Marker position of RFM, counting in SCLKR clock cycles (0 = bit 1, time slot 0, channel phase 0)

SC = 2.048 MHz: $0 \le MP \le 255$
SC = 4.096 MHz: $0 \le MP \le 511$
SC = 8.192 MHz: $0 \le MP \le 1023$
SC = 16.384 MHz: $0 \le MP \le 2047$

SD: Basic data rate, 2.048 Mbit/s

SC: System clock rate; 2.048, 4.096, 8.192, or 16.384 MHz

X: Programming value to be written to registers RC0 and RC1 (see **Page 243**).

$0 \le MP \le 2045$: $X = MP + 2$
$2046 \le MP \le 2047$: $X = MP - 2046$

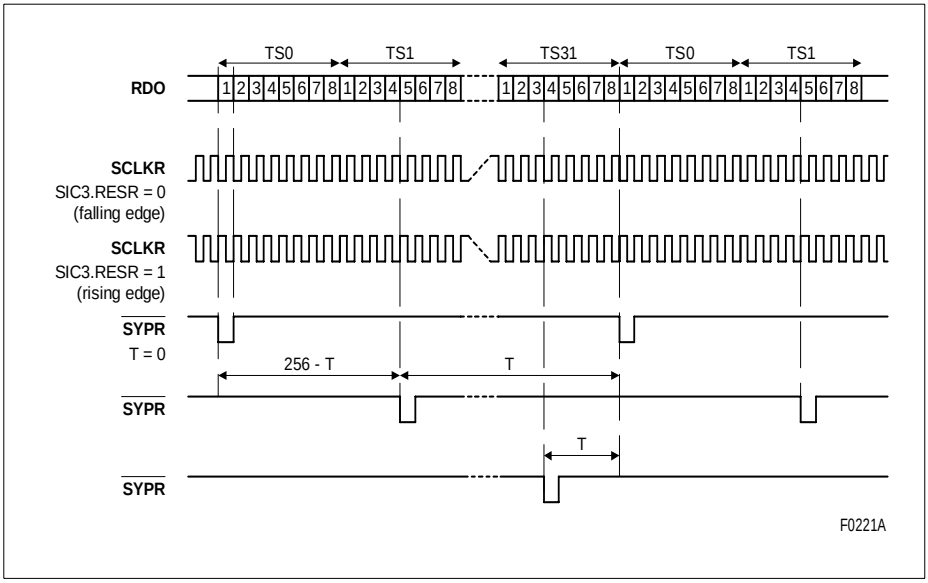


Figure 33 $\overline{\text{SYPR}}$ Offset Programming (2.048 Mbit/s, 2.048 MHz)

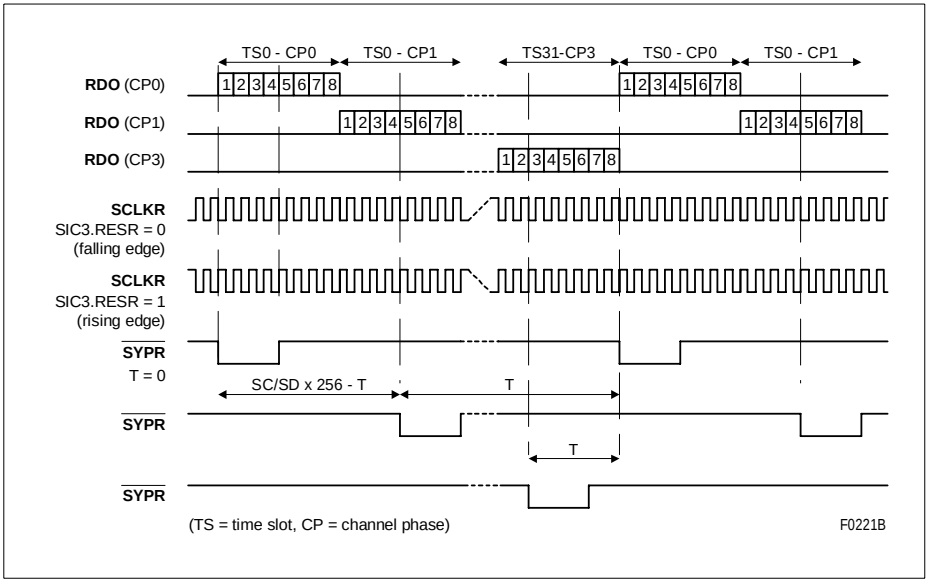


Figure 34 $\overline{\text{SYPR}}$ Offset Programming (8.192 Mbit/s, 8.192 MHz)

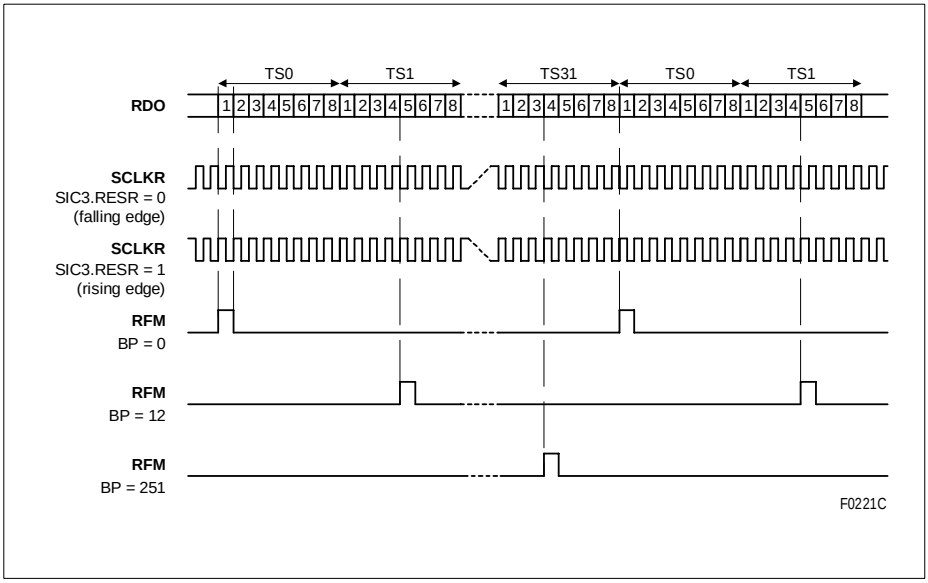


Figure 35 RFM Offset Programming (2.048 Mbit/s, 2.048 MHz)

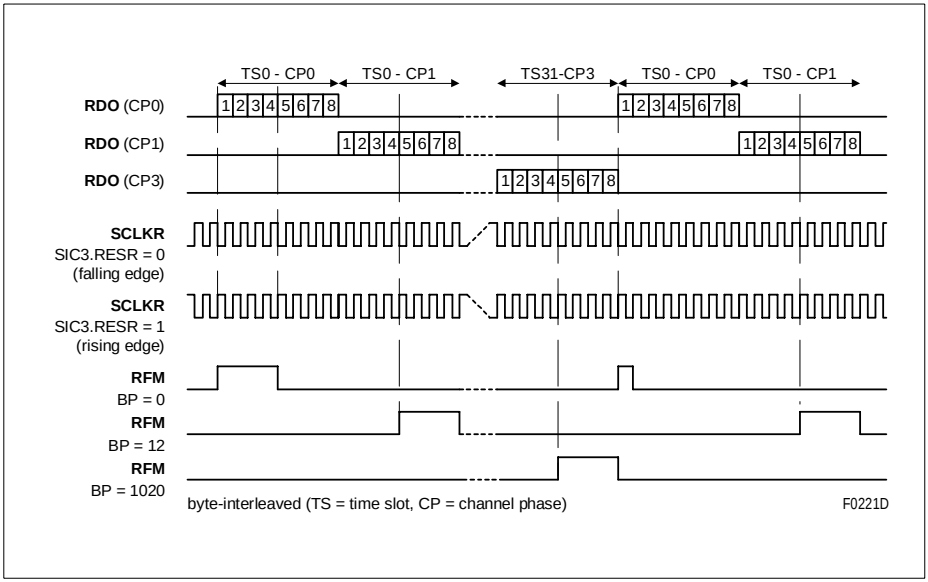


Figure 36 RFM Offset Programming (8.192 Mbit/s, 8.192 MHz)

4.5.2 Transmit System Interface (E1)

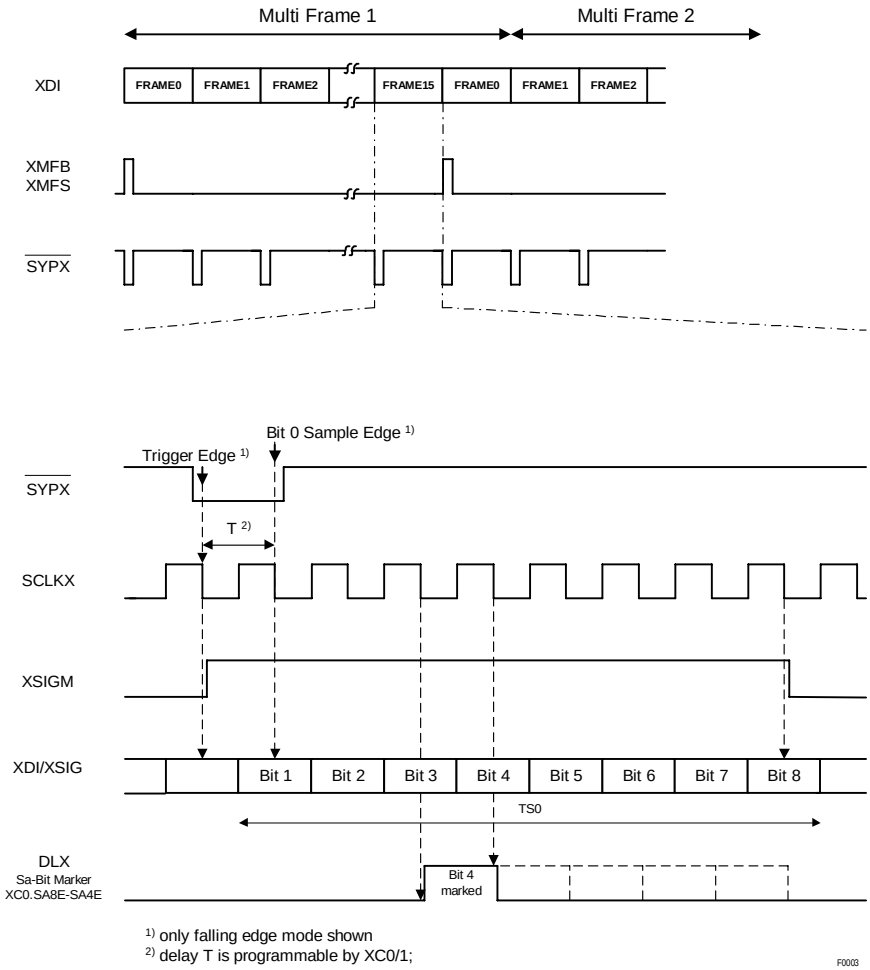


Figure 37 Transmit System Interface Clocking: 2.048 MHz (E1)

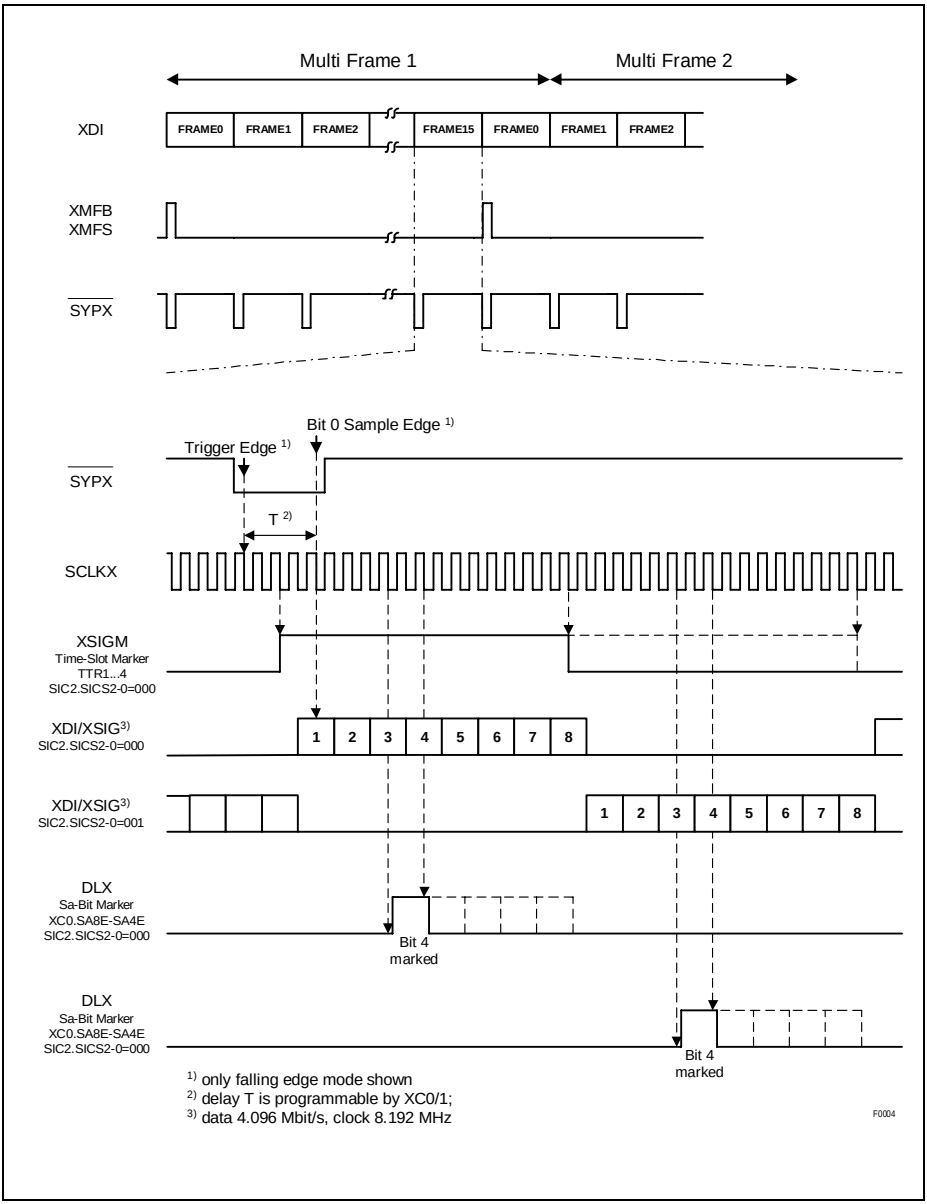


Figure 38 Transmit System Interface Clocking: 8.192 MHz/4.096 Mbit/s (E1)

4.5.2.1 Transmit Offset Programming

The pulse length of $\overline{\text{SYPX}}$ is always the basic E1 bit width (488 ns), independent of the selected system highway clock and data frequency.

$\overline{\text{SYPX}}$ Offset Calculation

T: Time between beginning of $\overline{\text{SYPX}}$ pulse and beginning of next frame (time slot 0, bit 0), measured in number of SCLKX clock intervals maximum delay: $T_{max} = (256 \times SC/SD) - 1$

SD: Basic data rate, 2.048 Mbit/s

SC: System clock rate; 2.048, 4.096, 8.192, or 16.384 MHz

X: Programming value to be written to registers XC0 and XC1 (see **Page 241**).

$0 \le T \le 4$: $X = 4 - T$
$5 \le T \le T_{max}$: $X = 256 \times SC/SD - T + 4$

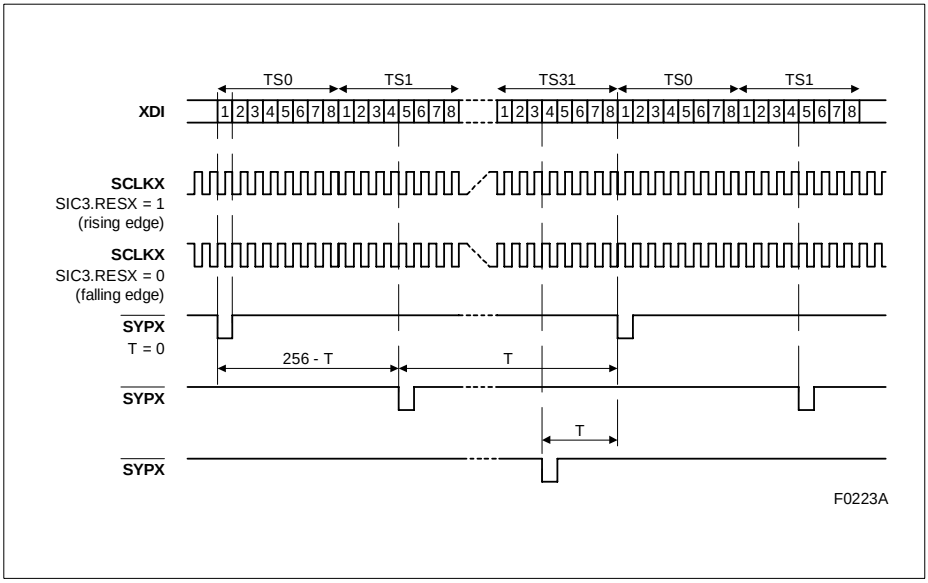


Figure 39 $\overline{\text{SYPX}}$ Offset Programming (2.048 Mbit/s, 2.048 MHz)

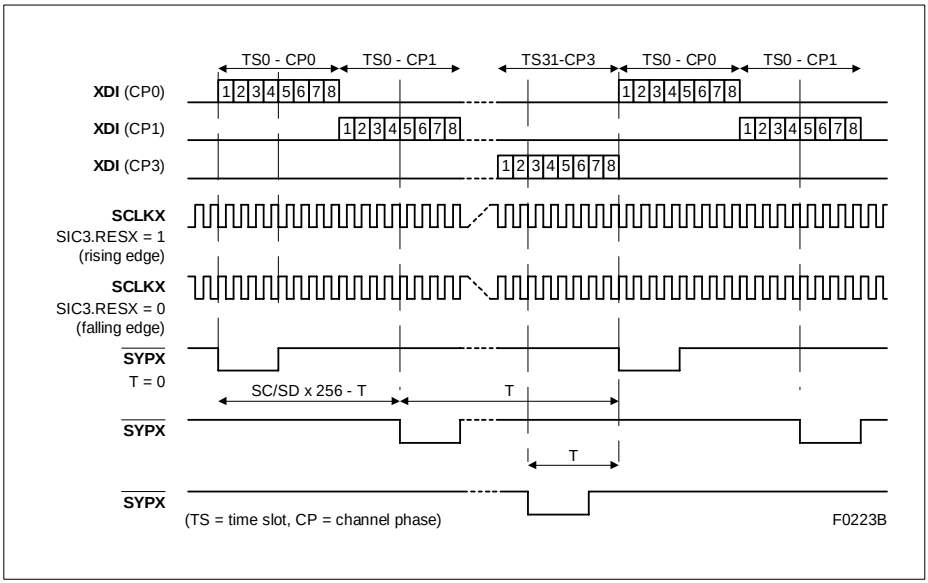


Figure 40 $\overline{\text{SYPX}}$ Offset Programming (8.192 Mbit/s, 8.192 MHz)

4.5.3 Time Slot Assigner (E1)

HDLC channel 1 offers the flexibility to connect data during certain time slots, as defined by registers RTR(4:1) and TTR(4:1), to the RFIFO and XFIFO, respectively. Any combinations of time slots can be programmed for the receive and transmit directions. If CCR1.EITS = 1 the selected time slots (RTR(4:1)) are stored in the RFIFO of the signaling controller and the XFIFO contents is inserted into the transmit path as controlled by registers TTR(4:1).

Within selected time slots single bit positions can be masked to be used/not used for HDLC transmission for all HDLC channels. Additionally, the use of even, odd or both frames can be selected.

Table 25 Time Slot Assigner HDLC Channel 1 (E1)

Receive Time Slot Register	Transmit Time Slot Register	Time Slots	Receive Time Slot Register	Transmit Time Slot Register	Time Slots
RTR 1.7	TTR 1.7	0	RTR 3.7	TTR 3.7	16
RTR 1.6	TTR 1.6	1	RTR 3.6	TTR 3.6	17
RTR 1.5	TTR 1.5	2	RTR 3.5	TTR 3.5	18
RTR 1.4	TTR 1.4	3	RTR 3.4	TTR 3.4	19
RTR 1.3	TTR 1.3	4	RTR 3.3	TTR 3.3	20
RTR 1.2	TTR 1.2	5	RTR 3.2	TTR 3.2	21
RTR 1.1	TTR 1.1	6	RTR 3.1	TTR 3.1	22
RTR 1.0	TTR 1.0	7	RTR 3.0	TTR 3.0	23
RTR 2.7	TTR 2.7	8	RTR 4.7	TTR 4.7	24
RTR 2.6	TTR 2.6	9	RTR 4.6	TTR 4.6	25
RTR 2.5	TTR 2.5	10	RTR 4.5	TTR 4.5	26
RTR 2.4	TTR 2.4	11	RTR 4.4	TTR 4.4	27
RTR 2.3	TTR 2.3	12	RTR 4.3	TTR 4.3	28
RTR 2.2	TTR 2.2	13	RTR 4.2	TTR 4.2	29
RTR 2.1	TTR 2.1	14	RTR 4.1	TTR 4.1	30
RTR 2.0	TTR 2.0	15	RTR 4.0	TTR 4.0	31

4.6 Test Functions (E1)

4.6.1 Pseudo-Random Bit Sequence Generation and Monitor

The QuadFALC has the ability to generate and monitor 2^{15}-1 and 2^{20}-1 pseudo-random bit sequences (PRBS). The generated PRBS pattern is transmitted to the remote end on pins XL1/2 or XDOP/N and can be inverted optionally. Generating and monitoring of PRBS pattern is done according to ITU-T O.151.

The PRBS monitor senses the PRBS pattern in the incoming data stream. Synchronization is done on the inverted and non-inverted PRBS pattern. The current synchronization status is reported in status and interrupt status registers. Enabled by bit LCR1.EPRM each PRBS bit error increments an error counter (CEC2). Synchronization is reached within 400 ms with a probability of 99.9% at a bit error rate of up to 10^{-1}.

The PRBS generator and monitor can be used to handle either a framed (TPC0.FRA = 1) or an unframed (TPC0.FRA = 0) data stream.

4.6.2 Remote Loop

In the remote loopback mode the clock and data recovered from the line inputs RL1/2 or RDIP/RDIN are routed back to the line outputs XL1/2 or XDOP/XDON through the analog or digital transmitter. As in normal mode they are also processed by the synchronizer and then sent to the system interface. The remote loopback mode is selected by setting the corresponding control bits LIM1.RL and LIM1.JATT. Received data can be looped with or without the transmit jitter attenuator (FIFO).

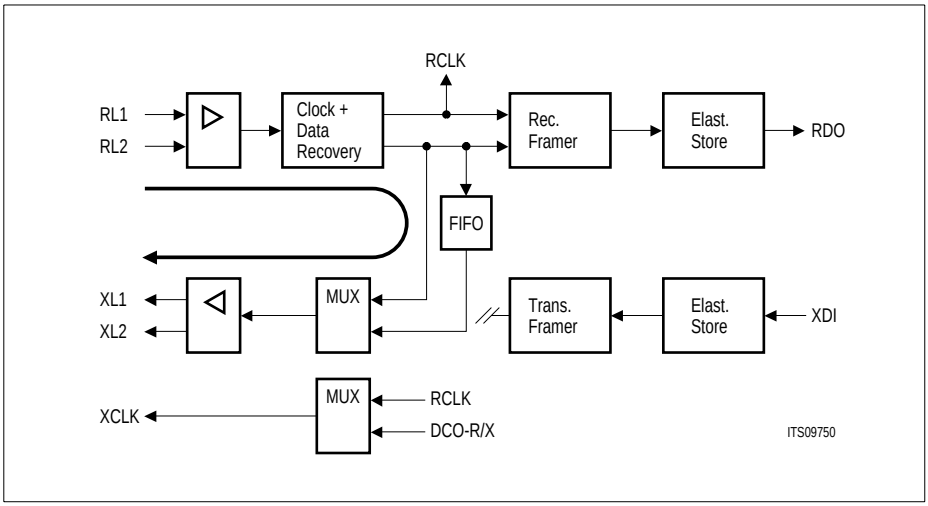


Figure 41 Remote Loop (E1)

4.6.3 Payload Loop Back

To perform an effective circuit test a payload loop is implemented. The payload loop back (FMR2.PLB) loops the data stream from the receiver section back to transmitter section. The looped data passes the complete receiver including the wander and jitter compensation in the receive elastic store and is output on pin RDO. Instead of the data an AIS signal (FMR2.SAIS) can be sent to the system interface.

The framing bits, CRC4 and spare bits are not looped, if XSP.TT0 = 0. They are generated by the QuadFALC transmitter. If the PLB is enabled the transmitter and the data on pins XL1/2 or XDOP/XDON are clocked with SCLKR instead of SCLKX. If XSP.TT0 = 1 the received time slot 0 is sent back transparently to the line interface. Data on the following pins is ignored: XDI, XSIG, SCLKX, $\overline{\text{SYPX}}$ and XMFS. All the received data is processed normally.

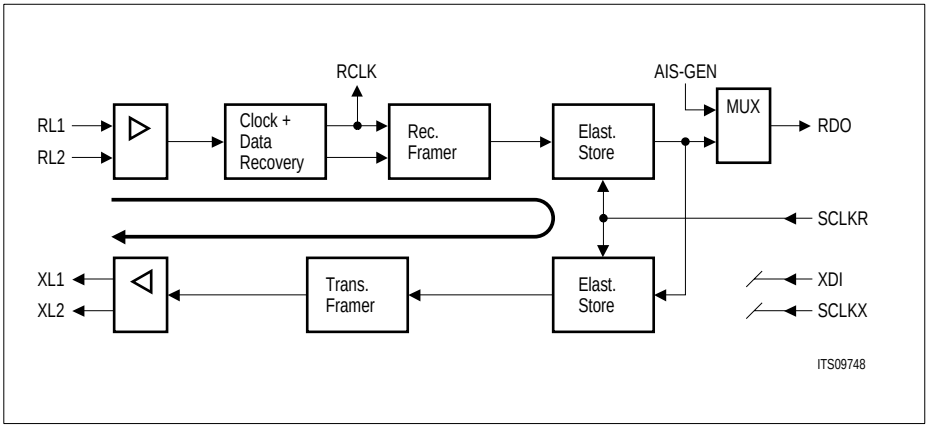


Figure 42 Payload Loop (E1)

4.6.4 Local Loop

The local loopback mode selected by LIM0.LL = 1 disconnects the receive lines RL1/2 or RDIP/RDIN from the receiver. Instead of the signals coming from the line the data provided by the system interface is routed through the analog receiver back to the system interface. However, the bit stream is transmitted undisturbedly on the line. However, an AIS to the distant end can be enabled by setting FMR1.XAIS = 1 without influencing the data looped back to the system interface.

Note that enabling the local loop usually invokes an out-of-frame error until the receiver resynchronizes to the new framing. The serial codes for transmitter and receiver have to be identical.

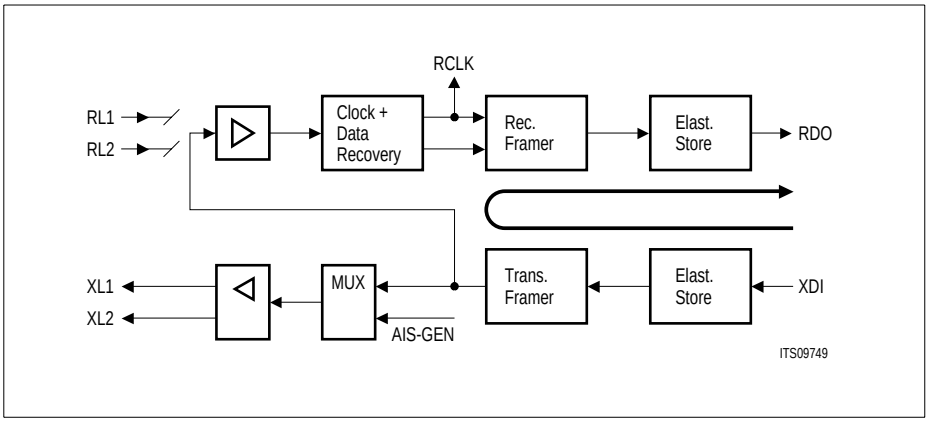


Figure 43 Local Loop (E1)

4.6.5 Single Channel Loop Back

Each of the 32 time slots can be selected for loopback from the system PCM input (XDI) to the system PCM output (RDO). This loopback is programmed for one time slot at a time selected by register LOOP. During loopback, an idle channel code programmed in register IDLE is transmitted to the remote end in the corresponding PCM route time slot.

For the time slot test, sending sequences of test patterns like a 1-kHz check signal shall be avoided. Otherwise an increased occurrence of slips in the tested time slot disturbs testing. These slips do not influence the other time slots and the function of the receive memory. The usage of a quasi-static test pattern is recommended.

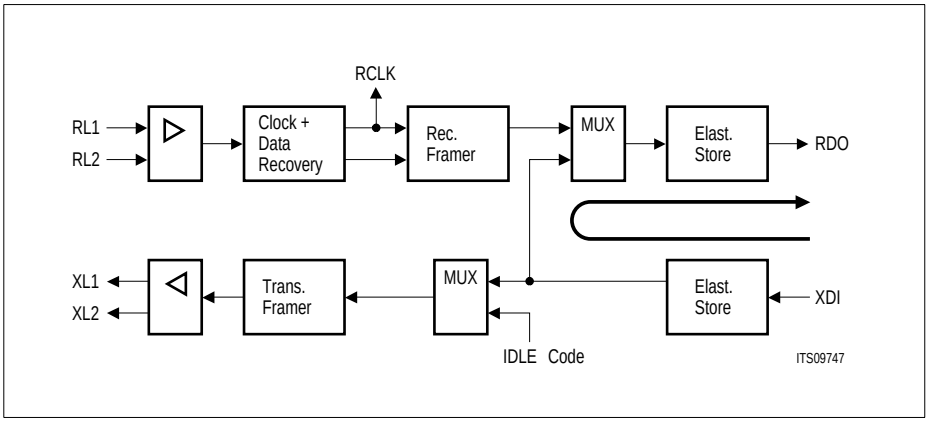


Figure 44 Single Channel Loopback (E1)

4.6.6 Alarm Simulation (E1)

Alarm simulation does not affect the normal operation of the device, i.e. all time slots remain available for transmission. However, possible *real* alarm conditions are *not* reported to the processor or to the remote end when the device is in the alarm simulation mode.

The alarm simulation is initiated by setting the bit FMR0.SIM. The following alarms are simulated:

- Loss of signal
- Alarm Indication Signal (AIS)
- Loss of pulse frame
- Remote alarm indication
- Receive and transmit slip indication
- Framing error counter
- Code violation counter (HDB3 Code)
- CRC4 error counter
- E-Bit error counter
- CEC2 counter
- CEC3 counter

Some of the above indications are only simulated if the QuadFALC is configured to a mode where the alarm is applicable (e.g. no CRC4 error simulation when doubleframe format is enabled).

Setting of the bit FMR0.SIM initiates alarm simulation, interrupt status bits are set. Error counting and indication occurs while this bit is set. After it is reset all simulated error conditions disappear, but the generated interrupt statuses are still pending until the corresponding interrupt status register is read. Alarms like AIS and LOS are cleared automatically. Interrupt status registers and error counters are automatically cleared on read.

4.6.7 Single Bit Defect Insertion

Single bit defects can be inserted into the transmit data stream for the following functions:

FAS defect, multiframe defect, CRC defect, CAS defect, PRBS defect and bipolar violation.

Defect insertion is controlled by register IERR.

5 Functional Description T1/J1

5.1 Receive Path in T1/J1 Mode

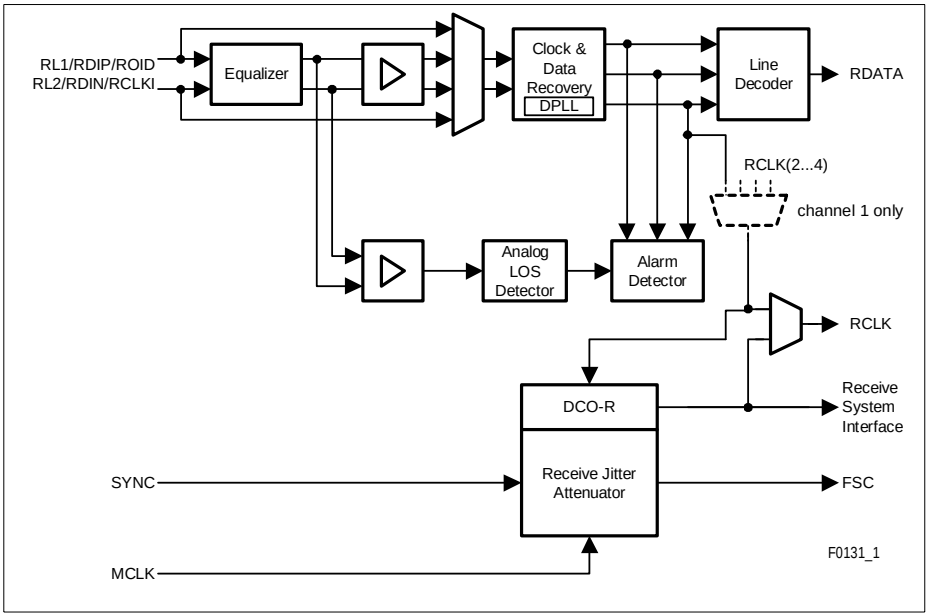


Figure 45 Receive Clock System (T1/J1)

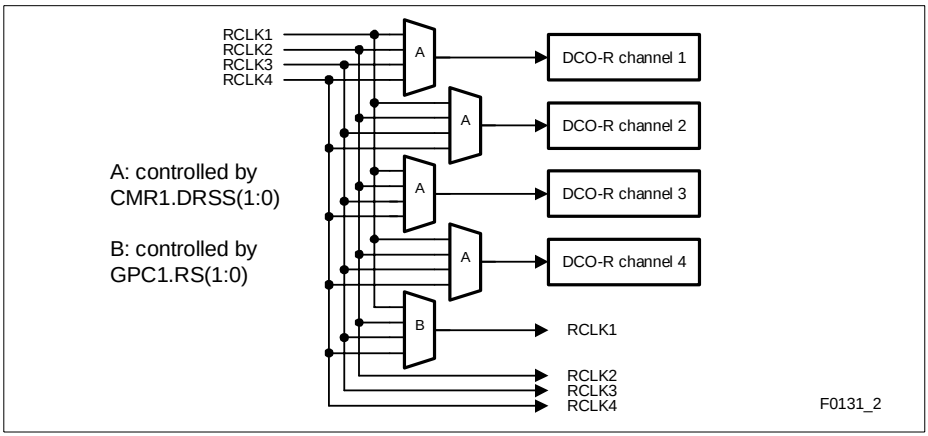


Figure 46 Receive Clock Selection (T1/J1)

5.1.1 Receive Line Interface (T1/J1)

For data input, three different data types are supported:

- Ternary coded signals received at multifunction ports RL1 and RL2 from a -36 dB ternary interface. The ternary interface is selected if LIM1.DRS is reset.
- Digital dual rail signals received on ports RDIP and RDIN. The dual rail interface is selected if LIM1.DRS and FMR0.RC1 is set.
- Unipolar data on port ROID received from a fibre optical interface. The optical interface is selected if LIM1.DRS is set and FMR0.RC1 is reset.

5.1.2 Receive Short and Long Haul Interface (T1/J1)

The QuadFALC has an integrated short haul and long haul line interface, including a receive equalization network, noise filtering and programmable line build-outs (LBO).

5.1.3 Receive Equalization Network (T1/J1)

The QuadFALC automatically recovers the signals received on pins RL1/2. The maximum reachable length with a 22 AWG twisted-pair cable is 2000 m (~6560 ft.). After reset the QuadFALC is in short haul mode, received signals are recovered up to -10 dB of cable attenuation. Automatic short haul/long haul detection and adjustment is done by setting of bit LIM0.EQON.
The integrated receive equalization network recovers signals with up to -36 dB of cable attenuation in long haul mode. Noise filters eliminate the higher frequency part of the received signals. The incoming data is peak detected and sliced to produce the digital data stream. The slicing level is software selectable in four steps (45%, 50%, 55%, 67%). The received data is then forwarded to the clock and data recovery unit.

5.1.4 Receive Line Attenuation Indication (T1/J1)

Status register RES reports the current receive line attenuation in a range from 0 to -36 dB in 25 steps of approximately 1.4 dB each. The least significant 5 bits of this register indicate the cable attenuation in dB. These 5 bits are only valid in combination with the most significant two bits (RES.EV1/0 = 01).

5.1.5 Receive Clock and Data Recovery (T1/J1)

The analog received signal on port RL1/2 is equalized and then peak-detected to produce a digital signal. The digital received signal on port RDIP/N is directly forwarded to the DPLL. The receive clock and data recovery extracts the route clock RCLK from the data stream received at the RL1/2, RDIP/RDIN or ROID lines and converts the data stream into a single rail, unipolar bit stream. The clock and data recovery uses an internally generated high frequency clock based on MCLK.

The recovered route clock or a dejittered clock can be output on pin RCLK as shown in **Table 26**. Additionally, RCLK1 can output the receive clocks of channels 2, 3 or 4 (RCLK(4:2), selected by CMR1.DRSS(1:0)).

See also **Table 29** on page **131** for details of master/slave clocking.

Table 26 RCLK Output Selection (T1/J1)

Clock Source	RCLK Frequency	Register Setting	
		CMR1. RS1/0	SIC2. SSC2
Receive Data (1.544 Mbit/s on RL1/RL2, RDIP/RDIN or ROID)	1.544 MHz	00	X
Receive Data (1.544 Mbit/s on RL1/RL2, RDIP/RDIN or ROID) in case of LOS	constant high	01	X
DCO-R	1.544 MHz	10	1
	2.048 MHz	10	0
	6.176 MHz	11	1
	8.192 MHz	11	0

The intrinsic jitter generated in the absence of any input jitter is not more than 0.035 UI. In digital bipolar line interface mode the clock and data recovery requires HDB3 coded signals with 50% duty cycle.

5.1.6 Receive Line Coding (T1/J1)

The B8ZS line code or the AMI (ZCS, zero code suppression) coding is provided for the data received from the ternary or the dual rail interface. All code violations that do not correspond to zero substitution rules are detected. The detected errors increment the code violation counter (16 bits length). In case of the optical interface a selection between the NRZ code and the CMI Code (1T2B) with B8ZS or AMI postprocessing is provided. If CMI code is selected the receive route clock is recovered from the data stream. The CMI decoder does not correct any errors. In case of NRZ coding data is latched with the falling edge RCLKI.

When using the optical interface with NRZ coding, the decoder is bypassed and no code violations are detected.

Additionally, the receive line interface contains the alarm detection for Alarm Indication Signal AIS (Blue Alarm) and the loss of signal LOS (Red Alarm).

The signal at the ternary interface is received at both ends of a transformer.

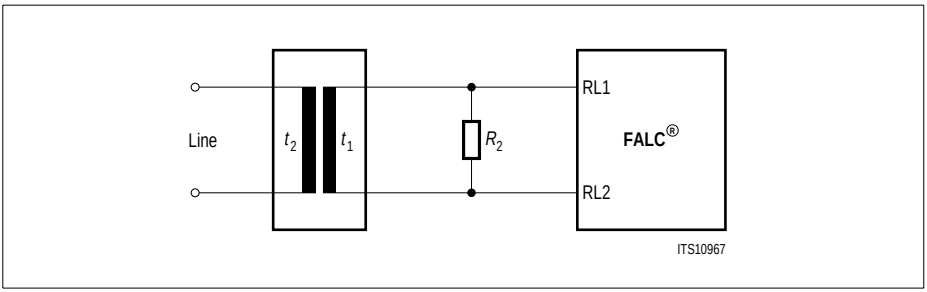


Figure 47 Receiver Configuration (T1/J1)

Table 27 Recommended Receiver Configuration Values (T1/J1)

Parameter[1)]	Characteristic Impedance [Ω]	
	T1	J1
R_2 (± 1%) [Ω]	100	110
$t_2 : t_1$	1 : 1	

1) This includes all parasitic effects caused by circuit board design.

5.1.7 Receive Line Monitoring Mode

For short haul applications like shown in **Figure 48**, the receive equalizer can be switched into receive line monitoring mode (LIM0.RLM = 1). One device is used as a short haul receiver while the other is used as a short haul monitor. In this mode the receiver sensitivity is increased to detect an incoming signal of -20 dB resistive attenuation. The required resistor values are given in **Table 28**.

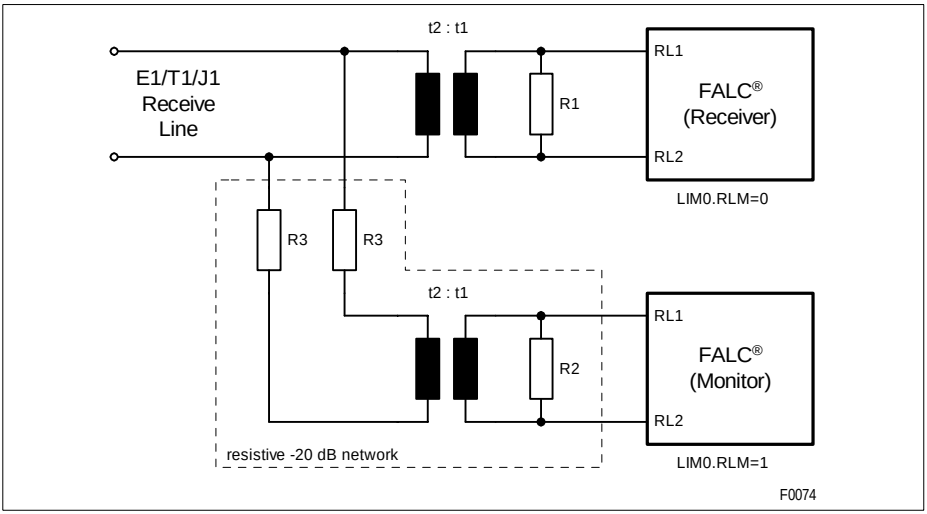


Figure 48 Receive Line Monitoring

Table 28 External Component Recommendations (Monitoring)

Parameter[1)]	Characteristic Impedance [Ω]	
	T1	**J1**
	100	**110**
R_1 (± 1 %) [Ω]	100	110
R_2 (± 1 %) [Ω]	100	110
R_3 (± 1 %) [Ω]	430	470
$t_2 : t_1$	1 : 1	1 : 1

1) This includes all parasitic effects caused by circuit board design.

Using the receive line monitor mode and the hardware tristate function of transmit lines XL1/2, the QuadFALC now supports applications connecting two devices to one receive

and transmission line. In these kind of applications both devices are working in parallel for redundancy purpose (see **Figure 49**). While one of them is driving the line, the other one must be switched into transmit line tristate mode. If both channels are configured identically and supplied with the same system data and clocks, the transmit path can be switched from one channel to the other without causing a synchronization loss at the remote end.

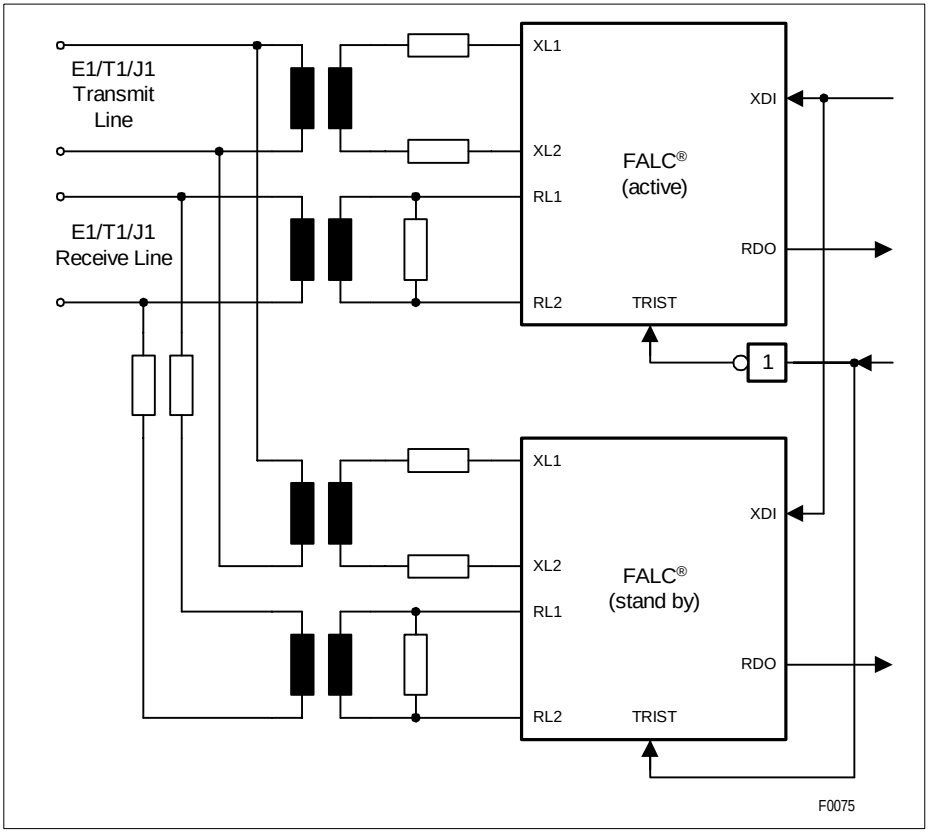


Figure 49 Protection Switching Application

5.1.8 Loss of Signal Detection (T1/J1)

There are different definitions for detecting loss of signal alarms (LOS) in the ITU-T G.775 and AT&T TR 54016. The QuadFALC covers all these standards. The LOS indication is performed by generating an interrupt (if not masked) and activating a status bit. Additionally a LOS status change interrupt is programmable by register GCR.SCI.

- Detection:
  An alarm is generated if the incoming data stream has no pulses (no transitions) for a certain number (N) of consecutive pulse periods. “No pulse” in the digital receive interface means a logical zero on pins RDIP/RDIN or ROID. A pulse with an amplitude less than P dB below nominal is the criteria for “no pulse” in the analog receive interface (LIM1.DRS = 0). The receive signal level P is programmable by three control bits LIM1.RIL(2:0) (see **Chapter 11.3** on page **422**). The number N is set by an 8 bit register (PCD). The contents of the PCD register is multiplied by 16, which results in the number of pulse periods, i.e. the time which has to suspend until the alarm has to be detected. The programmable range is 16 to 4096 pulse periods.
- Recovery:
  In general the recovery procedure starts after detecting a logical ’one’ (digital receive interface) or a pulse (analog receive interface) with an amplitude more than P dB (defined by LIM1.RIL(2:0)) of the nominal pulse. The value in the 8 bit register PCR defines the number of pulses (1 to 255) to clear the LOS alarm. Additional recovery conditions are programmed by register LIM2.

If a loss of signal condition is detected in long-haul mode, the data stream can optionally be cleared automatically to avoid bit errors before LOS is indicated. The selection is done by LIM1.CLOS = 1.

5.1.9 Receive Jitter Attenuator (T1/J1)

The receive jitter attenuator is placed in the receive path. The working clock is an internally generated high frequency clock based on the clock provided on pin MCLK. The jitter attenuator meets the requirements of PUB 62411, PUB 43802, TR-TSY 009,TR-TSY 253, TR-TSY 499 and ITU-T I.431, G.703 and G. 824.

The internal PLL circuitry DCO-R generates a ’jitter free’ output clock which is directly depending on the phase difference of the incoming clock and the jitter attenuated clock.The receive jitter attenuator can be synchronized either on the extracted receive clock RCLK or on a 1.544-, 2.048-MHz or 8-kHz clock provided on pin SYNC (8 kHz in master mode only). The received data is written into the receive elastic buffer with RCLK and are read out with the dejittered clock sourced by DCO-R. The jitter attenuated clock can be output on pins RCLK or SCLKR. Optionally an 8-kHz clock is provided on pin SEC/FSC.

The DCO-R circuitry attenuates the incoming jittered clock starting at 6-Hz jitter frequency with 20 dB per decade fall off. Wander with a jitter frequency below 6 Hz is passed unattenuated. The intrinsic jitter in the absence of any input jitter is < 0.02 UI.

For some applications it might be useful starting of jitter attenuation at lower frequencies. Therefore the corner frequency is switchable by the factor of ten downto 0.6 Hz (LIM2.SCF).

The DCO-R circuitry is automatically centered to the nominal bit rate if the reference clock on pin SYNC/RCLK is missed for 2 to 4 2.048-MHz or 1.544-MHz clock periods

(only if 2.048 MHz or 1.544 MHz clock is used). This center function of DCO-R can be optionally disabled (CMR2.DCF = 1) in order to accept a gapped reference clock.

In analog line interface mode the RCLK is always running. Only in digital line interface mode with single rail data (NRZ) a gapped clock on pin RCLK can occur.

The receive jitter attenuator works in two different modes:

- Slave mode
  In slave mode (LIM0.MAS = 0) the DCO-R is synchronized on the recovered route clock. In case of LOS the DCO-R switches automatically to master mode. If bit CMR1.DCS is set automatic switching from RCLK to SYNC is disabled.
- Master mode
  In master mode (LIM0.MAS = 1) the jitter attenuator is in free running mode if no clock is supplied on pin SYNC. If an external clock on the SYNC input is applied, the DCO-R synchronizes to this input. The external frequency can be 1.544 MHz (LIM1.DCOC = 0; IPC.SSYF = 0), 2.048 MHz (LIM1.DCOC = 1; IPC.SSYF = 0) or 8.0 kHz (IPC.SSYF = 1; LIM1.DCOC = don't care).

The following table shows the clock modes with the corresponding synchronization sources.

Table 29 System Clocking (T1/J1)

Mode	Internal LOS Active	SYNC Input	System Clocks
Master	independent	Fixed to VDD	DCO-R centered, if CMR2.DCF = 0. (CMR2.DCF should not be set)
Master	independent	1.544 MHz	Synchronized on SYNC input (external 1.544 MHz, IPC.SSYF = 0, LIM1.DCOC = 0)
Master	independent	2.048 MHz	Synchronized on SYNC input (external 2.048 MHz, IPC.SSYF = 0, LIM1.DCOC = 1)
Master	independent	8.0 kHz	Synchronized on SYNC input (external 8.0 kHz, IPC.SSYF = 1, CMR2.DCF = 0)
Slave	no	Fixed to VDD	Synchronized on line RCLK
Slave	no	1.544 or 2.048 MHz	Synchronized on line RCLK

Table 29 System Clocking (T1/J1) (cont'd)

Mode	Internal LOS Active	SYNC Input	System Clocks
Slave	yes	Fixed to VDD	CMR1.DCS = 0: DCO-R is centered, if CMR2.DCF = 0. (CMR2.DCF should not be set)
			CMR1.DCS = 1: Synchronized on line RCLK
Slave	yes	1.544 or 2.048 MHz	CMR1.DCS = 0: Synchronized on SYNC input (external 1.544 or 2.048 MHz)
			CMR1.DCS = 1: Synchronized on line clock RCLK(4:1), channel selected by CMR1.DRSS(1:0)

The jitter attenuator meets the jitter transfer requirements of the PUB 62411, PUB 43802, TR-TSY 009,TR-TSY 253, TR-TSY 499 and ITU-T I.431 and G.703 (refer to **Figure 50**).

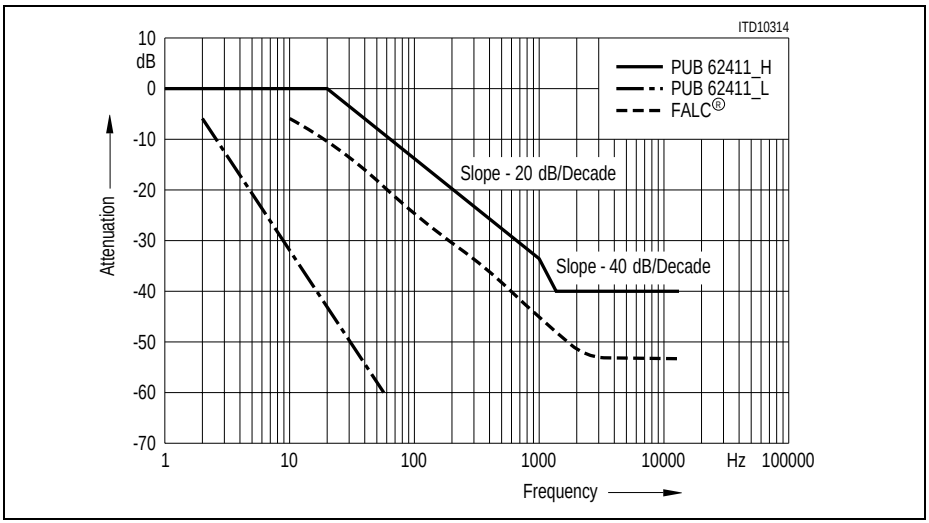


Figure 50 Jitter Attenuation Performance (T1/J1)

5.1.10 Jitter Tolerance (T1/J1)

The QuadFALC receiver's tolerance to input jitter complies to ITU, AT&T and Telcordia requirements for T1 applications.

Figure 51 shows the curves of different input jitter specifications stated below as well as the QuadFALC performance.

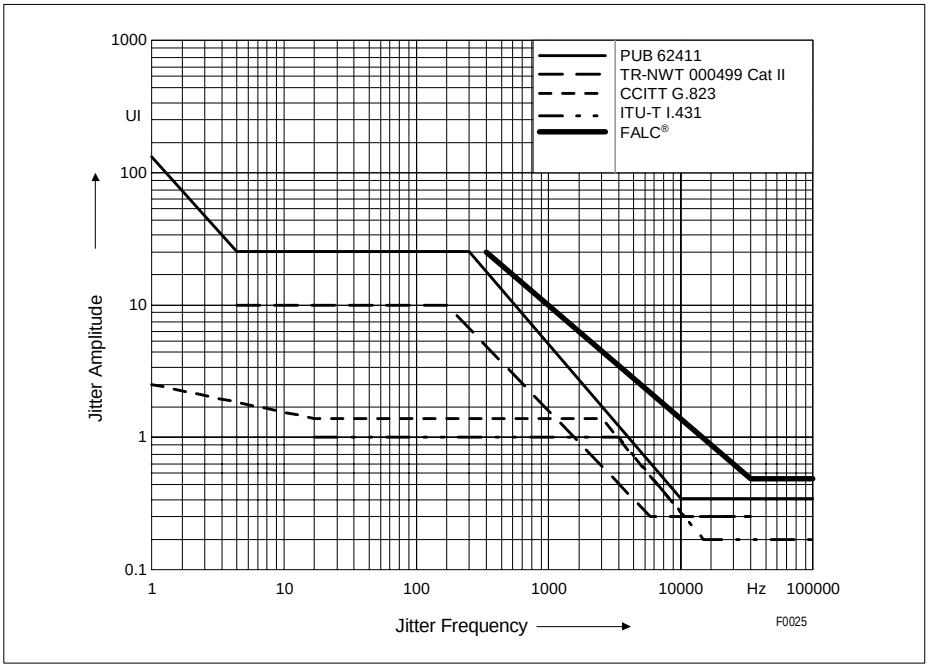


Figure 51 Jitter Tolerance (T1/J1)

5.1.11 Output Jitter (T1/J1)

According to the input jitter defined by PUB62411 the QuadFALC generates the output jitter, which is specified in **Table 30** below.

Table 30 Output Jitter (T1/J1)

Specification	Measurement Filter Bandwidth		Output Jitter (UI peak to peak)
	Lower Cutoff	Upper Cutoff	
PUB 62411	10 Hz	8 kHz	< 0.015
	8 kHz	40 kHz	< 0.015
	10 Hz	40 kHz	< 0.015
	Broadband		< 0.02

5.1.12 Framer/Synchronizer (T1/J1)

The following functions are performed:

- Synchronization on pulse frame and multiframe
- Error indication when synchronization is lost. In this case, AIS is sent to the system side automatically and remote alarm to the remote end if enabled.
- Initiating and controlling of resynchronization after reaching the asynchronous state. This is done automatically by the QuadFALC or user controlled by the microprocessor interface.
- Detection of remote alarm (yellow alarm) indication from the incoming data stream.
- Separation of service bits and data link bits. This information is stored in special status registers.
- Detection of framed or unframed in-band loop up/down code
- Generation of various maskable interrupt statuses of the receiver functions.
- Generation of control signals to synchronize the CRC checker, and the receive elastic buffer.

If programmed and applicable to the selected multiframe format, CRC checking of the incoming data stream is done by generating check bits for a CRC multiframe according to the CRC6 procedure (refer to ITU-T G.704). These bits are compared with those check bits that are received during the next CRC multiframe. If there is at least one mismatch, the CRC error counter (16 bit) is incremented.

5.1.13 Receive Elastic Buffer (T1/J1)

The received bit stream is stored in the receive elastic buffer. The memory is organized as a two-frame elastic buffer with a maximum size of 2×193 bit. The size of the elastic buffer is configured independently for the receive and transmit direction. Programming of the receive buffer size is done by SIC1.RBS1/0:

- RBS1/0 = 00: two frame buffer or 386 bits
  Maximum of wander amplitude (peak-to-peak): (1 UI = 648 ns)
  System interface clocking rate: modulo 2.048 MHz:
  142 UI in channel translation mode 0
  78 UI in channel translation mode 1
  System interface clocking rate: modulo 1.544 MHz:
  Maximum of wander: 140 UI
  average delay after performing a slip: 1 frame or 193 bits
- RBS1/0 = 01: one frame buffer or 193 bits
  System interface clocking rate: modulo 2.048 MHz:
  Maximum of wander: 70 UI in channel translation mode 0
  Maximum of wander: 50 UI in channel translation mode 1
  System interface clocking rate: modulo 1.544 MHz:
  Maximum of wander: 74 UI
  average delay after performing a slip: 96 bits
- RBS1/0 = 10: short buffer or 96 bits
  System interface clocking rate: modulo 2.048 MHz:
  Maximum of wander: 28 UI in channel translation mode 0; channel translation mode 1 not supported
  System interface clocking rate: modulo 1.544 MHz:
  Maximum of wander: 38 UI
  average delay after performing a slip: 48 bits
- RBS1/0 = 11: Bypass of the receive elastic buffer

The functions are:

- Clock adaptation between system clock (SCLKR) and internally generated route clock (RCLK).
- Compensation of input wander and jitter.
- Frame alignment between system frame and receive route frame
- Reporting and controlling of slips

Controlled by special signals generated by the receiver, the unipolar bit stream is converted into bit-parallel, time slot serial data which is circularly written to the elastic buffer using internally generated Receive Route Clock (RCLK).

Reading of stored data is controlled by the system clock sourced by SCLKR or by the receive jitter attenuator and the synchronization pulse ($\overline{\text{SYPR}}$) together with the programmed offset values for the receive time slot/clock slot counters. After conversion into a serial data stream, the data is sent out on port RDO. If the receive buffer is bypassed programming of the time slot offset is disabled and data is clocked off with RCLK instead of SCLKR.

The 24 received time slots (T1/J1) can be translated into the 32 system time slots (E1) in two different channel translation modes (FMR1.CTM). Unequipped time slots are set to 'FF_H'. See **Table 31**.

Table 31 Channel Translation Modes (DS1/J1)

Channels		Time Slots	Channels		Time Slots
Channel Translation Mode 0	Channel Translation Mode 1		Channel Translation Mode 0	Channel Translation Mode 1	
FS/DL	FS/DL	0	–	16	16
1	1	1	13	17	17
2	2	2	14	18	18
3	3	3	15	19	19
–	4	4	–	20	20
4	5	5	16	21	21
5	6	6	17	22	22
6	7	7	18	23	23
–	8	8	–	24	24
7	9	9	19	–	25
8	10	10	20	–	26
9	11	11	21	–	27
–	12	12	–	–	28
10	13	13	22	–	29
11	14	14	23	–	30
12	15	15	24	–	31

– : FF_H

In one frame or short buffer mode the delay through the receive buffer is reduced to an average delay of 96 or 48 bits. In bypass mode the time slot assigner is disabled. In this case $\overline{\text{SYPR}}$ programmed as input is ignored. Slips are performed in all buffer modes except the bypass mode. After a slip is detected the read pointer is adjusted to one half of the current buffer size.

The following table gives an overview of the receive buffer operating mode.

Table 32 Receive Buffer Operation Modes (T1/J1)

Buffer Size (SIC1.RBS1/0)	**TS Offset program.** (RC1/0) + $\overline{\text{SYPR}}$ = input	**Slip perform.**
bypass[1)]	disabled	no
short buffer	not recommended, recommended: RFM	yes
1 frame	not recommended, recommended: RFM	yes
2 frames	enabled	yes

[1)] In bypass mode the clock provided on pin SCLKR is ignored. Clocking is done with RCLK.

Figure 52 gives an idea of operation of the receive elastic buffer:
A slip condition is detected when the write pointer (W) and the read pointer (R) of the memory are nearly coincident, i.e. the read pointer is within the slip limits (S +, S –). If a slip condition is detected, a negative slip (one frame or one half of the current buffer size is skipped) or a positive slip (one frame or one half of the current buffer size is read out twice) is performed at the system interface, depending on the difference between RCLK and the current working clock of the receive backplane interface, i.e. on the position of pointer R and W within the memory. A positive/negative slip is indicated by the interrupt status bits ISR3.RSP and ISR3.RSN.

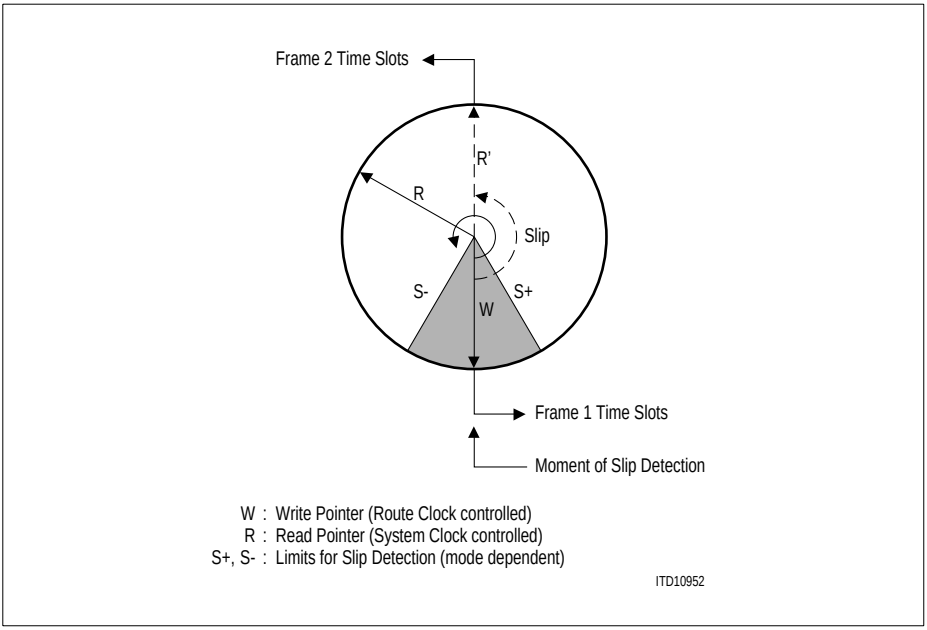


Figure 52 The Receive Elastic Buffer as Circularly Organized Memory

5.1.14 Receive Signaling Controller (T1/J1)

The signaling controller can be programmed to operate in various signaling modes. The QuadFALC performs the following signaling and data link methods.

5.1.14.1 HDLC or LAPD access

The QuadFALC offers one HDLC controller for each channel. All of them provide the following features:

- 64 byte receive FIFO for each channel
- 64 byte transmit FIFO for each channel
- transmission in up to 24 time slots
  (time slot number programmable for each channel individually)
- transmission in even frames only, odd frames only or both
  (programmable for each channel individually)
- bit positions to be used in selected time slots are maskable
  (any bit position can be enabled for each channel individually)
- HDLC or transparent mode
- flag detection
- CRC checking
- bit-stuffing
- flexible address recognition (1 byte, 2 bytes)
- C/R bit processing (according to LAPD protocol)
- SS7 support
- BOM (bit oriented message) support
- flexibility to insert and extract data during certain time slots, any combination of time slots can be programmed independently for the receive and transmit direction

In case of common channel signaling the signaling procedure HDLC/SDLC or LAPD according to Q.921 is supported. The signaling controller of the QuadFALC performs the flag detection, CRC checking, address comparison and zero bit removing. The received data flow and the address recognition features can be performed in very flexible way, to satisfy almost any practical requirements. Depending on the selected address mode, the QuadFALC performs a 1 or 2-byte address recognition. If a 2-byte address field is selected, the high address byte is compared with the fixed value FEH or FCH (group address) as well as with two individually programmable values in RAH1 and RAH2 registers. According to the ISDN LAPD protocol, bit 1 of the high byte address is interpreted as command/response bit (C/R) and is excluded from the address comparison. Buffering of receive data is done in a 64 byte deep RFIFO.
In signaling controller transparent mode, fully transparent data reception without HDLC framing is performed, i.e. without flag recognition, CRC checking or bit stuffing. This allows user specific protocol variations.

5.1.14.2 Support of Signaling System #7

The HDLC controller supports the signaling system #7 (SS7) which is described in ITU-Q.703. The following description assumes, that the reader is familiar with the SS7 protocol definition.

SS7 support must be activated by setting the MODE register. The SS7 protocol is supported by the following hardware features in receive mode:

- all Signaling Units (SU) are stored in the receive FIFO (RFIFO)
- detecting of flags from the incoming data stream
- bit stuffing (zero deletion)
- checking of seven or more consecutive ones in the receive data stream (octet counting mode handling according to ITU-T Q.703)
- checking if the received Signaling Unit is a multiple of eight bits and at least six octets including the opening flag
- calculation of the CRC16 checksum:
  In receive direction the calculated checksum is compared to the received one; errors are reported in register RSIS.
- checking if the signal information field of a received signaling unit consists of more than 272 octets, in this case the current signaling unit is discarded.

In order to reduce the microprocessor load, fill In signaling units (FISUs) are processed automatically. By examining the length indicator of a received signal unit the QuadFALC decides whether a FISU has been received. Consecutively received FISUs are compared and not stored in the receive FIFO (RFIFO, 2×32 bytes), if the contents is equal to the previous one. The same applies to link status signaling units, if bit CCR5.CSF is set. The different types of signaling units as message signaling unit (MSU), link status signaling unit (LSSU) and fill in signaling units (FISU) are indicated in the RSIS register, which is automatically added to the RFIFO with each received signaling unit. The complete signaling unit except start and end flags is stored in the receive FIFO. The functions of bits CCR1.RCRC and CCR1.RADD are still valid in SS7 mode. Errored signaling units are handled automatically according to ITU-T Q.703 as shown in **Figure 24**. SU counter (su) and errored SU counter (C_s) are reset by setting CMDR2.RSUC. The error threshold T can be selected to be 64 (default) or 32 by setting/clearing bit CCR5.SUET. If the defined error limit is exceeded, an interrupt (ISR1.SUEX) is generated, if not masked by IMR1.SUEX = 1.

Note: If SUEX is caused by an aborted/invalid frame, the interrupt will be issued regularly until a valid frame is received (e.g. a FISU).

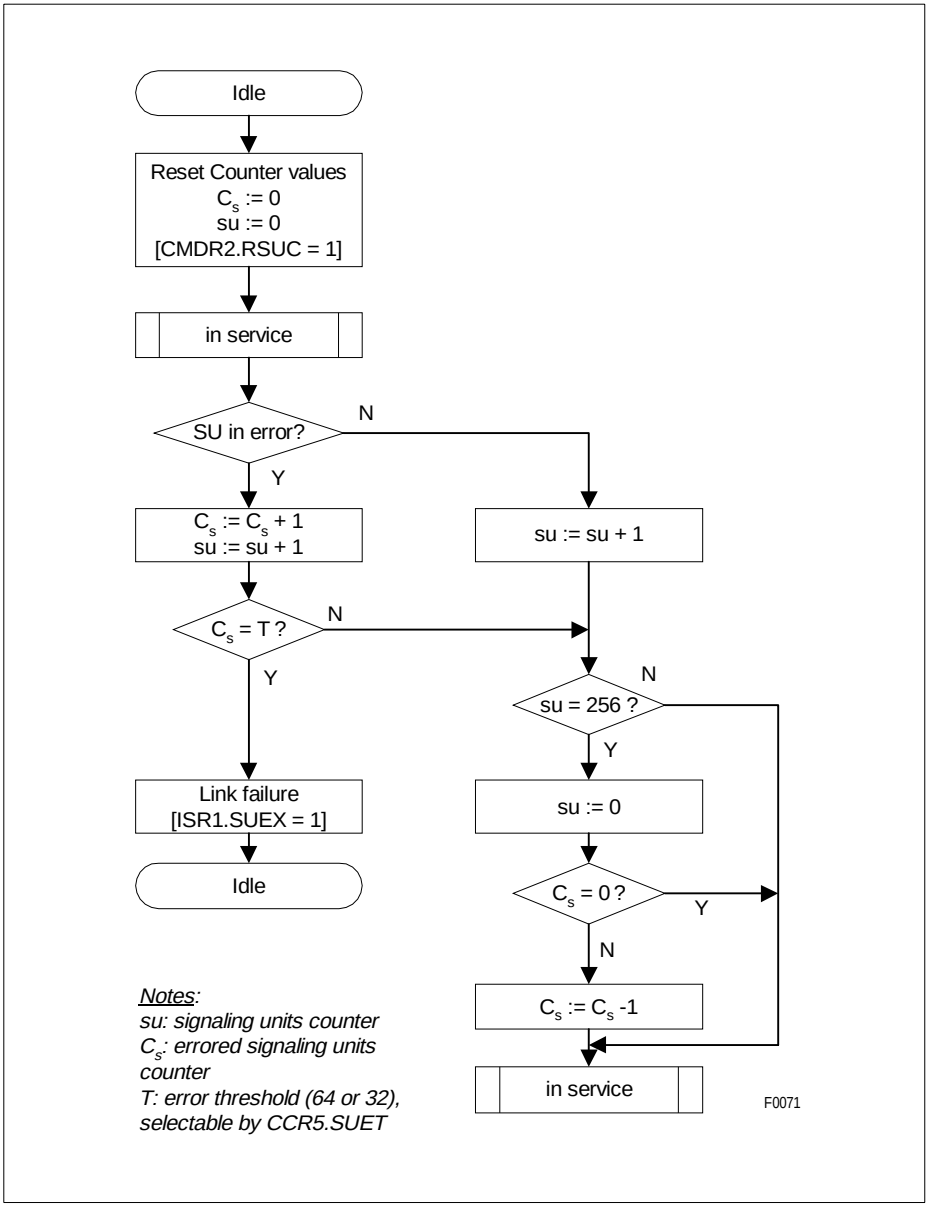


Figure 53 Automatic Handling of Errored Signaling Units

5.1.14.3 CAS Bit-Robbing (T1/J1, serial mode)

The signaling information is carried in the LSB of every sixth frame for each time slot. The signaling controller samples the bit stream either on the receive line side or if external signaling is enabled on the receive system side on port RSIG. Receive signaling data is stored in the registers RS(12:1).
Optionally the complete CAS multiframe is transmitted on pin RSIG (FMR5.EIBR = 1). The signaling data is clocked out with the working clock of the receive highway (SCLKR) together with the receive synchronization pulse ($\overline{\text{SYPR}}$). Data on RSIG is transmitted in the last 4 bits per time slot and are time slot aligned to the data on RDO. In ESF format the A,B,C,D bits are placed in the bit positions 5 to 8 per time slot. In F12/72 format the A and B bits are repeated in the C and D bit positions. The first 4 bits per time slot can be optionally fixed high or low. The FS/DL time slot is transmitted on RDO and RSIG. During idle time slots no signaling information is transmitted. Data on RSIG are only valid if the freeze signaling status is inactive. With FMR2.SAIS all-ones data is transmitted on RDO and RSIG.

Updating of the received signaling information is controlled by the freeze signaling status. The freeze signaling status is automatically activated if a Loss of Signal, or a Loss of Frame Alignment or a receive slip occurs. The current freeze status is output on port FREEZE (RPA to D) and indicated by register SIS.SFS. If SIS.SFS is active updating of the registers RS(12:1) is disabled. Optionally automatic freeze signaling is disabled by setting bit SIC3.DAF.

After CAS resynchronization an interrupt is generated. Because at this time the signaling is still frozen, CAS data is not valid yet. Readout of CAS data has to be delayed until the next CAS multiframe is received.

5.1.14.4 CAS Bit-Robbing (T1/J1, µP access mode)

The signaling information is carried in the LSB of every sixth frame for each time slot. Receive data is stored in registers RS(12:1) aligned to the CAS multiframe boundary.

To relieve the microprocessor load from always reading the complete RS(12:1) buffer every 3 ms the QuadFALC notifies the microprocessor by interrupt ISR0.RSC only when signaling changes from one multiframe to the next. Additionally the QuadFALC generates a receive signaling data change pointer (RSP1/2) which directly points to the updated RS(12:1) register.

Because the CAS controller is working on the PCM highway side of the receive buffer, slips disturb the CAS data.

5.1.14.5 Bit Oriented Messages in ESF-DL Channel (T1/J1)

The QuadFALC supports the DL-channel protocol for ESF format according to ANSI T1.403 specification or according to AT&T TR54016. The HDLC and bit oriented message (BOM) receiver are switched on/off independently. If the QuadFALC is used

for HDLC formats only, the BOM receiver has to be switched off. If HDLC and BOM receiver have been switched on (MODE.HRAC/BRAC), an automatic switching between HDLC and BOM mode is enabled. If eight or more consecutive ones are detected, the BOM mode is entered. Upon detection of a flag in the data stream, the QuadFALC switches back to HDLC mode. In BOM mode, the following byte format is assumed (the left most bit is received first): 111111110xxxxxx0
Three different BOM reception modes can be programmed (CCR1.BRM+ CCR2.RBFE). If CCR2.RFBE is set, the BOM receiver accepts only BOM frames after detecting 7 out of 10 equal BOM pattern. Buffering of receive data is done in a 64 byte deep RFIFO.

5.1.14.6 4 kbit/s Data Link Access in F72 Format (T1/J1)

The DL-channel protocol is supported as follows:

- Access is done on a multiframe basis through registers RDL(3:1),
- The DL-bit information from frame 26 to 72 is stored in the receive FIFO of the signaling controller.

5.2 Framer Operating Modes (T1/J1)

5.2.1 General

Activated with bit FMR1.PMOD = 1.

PCM line bit rate	:	1.544 Mbit/s
Single frame length	:	193 bit, No. 1 to 193
Framing frequency	:	8 kHz
Organization	:	24 time slots, No. 1 to 24 with 8 bits each, No. 1to 8 and one preceding F-bit

Selection of one of the four permissible framing formats is performed by bits FMR4.FM1/0. These formats are:

F4 : 4-frame multiframe
F12 : 12-frame multiframe (D4)
ESF : Extended Superframe (F24)
F72 : 72-frame multiframe (SLC96)

The operating mode of the QuadFALC is selected by programming the carrier data rate and characteristics, line code, multiframe structure, and signaling scheme.

The QuadFALC implements all of the standard and/or common framing structures PCM24 (T1/J1, 1.544 Mbit/s) carriers. The internal HDLC controller supports all signaling procedures including signaling frame synchronization/synthesis in all framing formats.

After reset, the QuadFALC must be programmed with FMR1.PMOD = 1 to enable the T1/J1 (PCM24) mode. Switching between the framing formats is done by bit FMR4.FM1/0 for the receiver and for the transmitter.

5.2.2 General Aspects of Synchronization

Synchronization status is reported by bit FRS0.LFA (Loss Of Frame Alignment). Framing errors (pulse frame and multiframe) are counted by the Framing Error Counter FEC.

Asynchronous state is reached if
2 out of 4 (bit FMR4.SSC1/0 = 00), or
2 out of 5 (bit FMR4.SSC1/0 = 01), or
2 out of 6 (bit FMR4.SSC1/0 = 10), or
4 consecutive multiframe pattern in ESF format are incorrect (bit FMR4.SSC1/0 = 11).
If auto mode is enabled, counting of framing errors is interrupted.

The resynchronization procedure is controlled by either one of the following procedures:

- Automatically (FMR4.AUTO = 1). Additionally, it can be triggered by the user by setting/resetting one of the bits FMR0.FRS (force resynchronization) or FMR0.EXLS (external loss of frame).
- User controlled, exclusively, by the control bits described above in the non-auto mode (FMR4.AUTO = 0).

5.2.3 Addition for F12 and F72 Format

FT and FS bit conditions, i.e. pulse frame alignment and multiframe alignment can be handled separately if programmed by bit FMR2.SSP. Thus, a multiframe resynchronization can be automatically initiated after detecting 2 errors out of 4/5/6 consecutive multiframing bits without influencing the state of the terminal framing.

In the synchronous state, the setting of FMR0.FRS or FMR0.EXLS resets the synchronizer and initiates a new frame search. The synchronous state is reached if there is only one definite framing candidate. In the case of repeated apparent simulated candidates, the synchronizer remains in the asynchronous state.

In asynchronous state, the function of FMR0.EXLS is the same as above. Setting bit FMR0.FRS induces the synchronizer to lock onto the next available framing candidate if there is one. Otherwise a new frame search is started. This is useful in case the framing pattern that defines the pulseframe position is imitated periodically by a pattern in one of the speech/data channels.

The control bit FMR0.EXLS should be used first because it starts the synchronizer to search for a definite framing candidate.

To observe actions of the synchronizer, the Frame Search Restart Flag FRS0.FSRF is implemented. It toggles at the start of a new frame search if no candidate has been found at previous attempt.

When resynchronization is initiated, the following values apply for the time required to achieve the synchronous state in case there is one definite framing candidate within the data stream:

Table 33 Resynchronization Timing (T1/J1)

Frame Mode	Average	Maximum	Units
F4	1.0	1.5	ms
F12	3.5	4.5	
ESF	3.4	6.125	
F72	13.0	17.75	

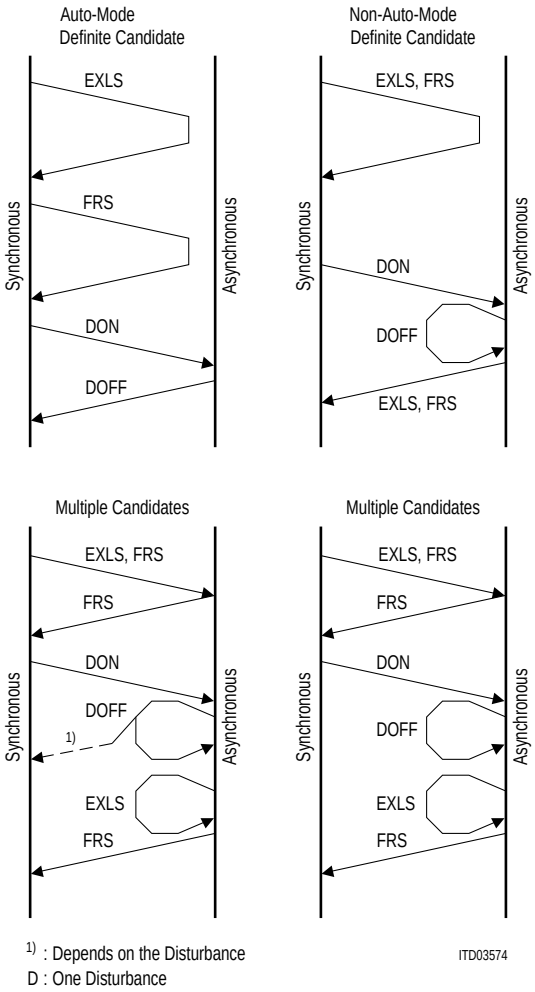


Figure 54 Influences on Synchronization Status (T1/J1)

Figure 54 gives an overview of influences on synchronization status for the case of different external actions. Activation of auto mode and non-auto mode is performed by bit FMR4.AUTO. Generally, for initiating resynchronization it is recommended to use bit: FMR0.EXLS first. In cases where the synchronizer remains in the asynchronous state, bit FMR0.FRS is used to enforce it to lock onto the next framing candidate, although it might be a simulated one.

5.2.4 4-Frame Multiframe (F4 Format, T1/J1)

The allocation of the FT-bits (bit 1 of frames 1 and 3) for frame alignment signal is shown in **Table 34**.

The FS-bit can be used for signaling. Remote alarm (yellow alarm) is indicated by setting bit 2 to 0 in each time slot.

Table 34 4-Frame Multiframe Structure (T1/J1)

Frame Number	F_T	F_S
1	1	
2	–	service bit
3	0	
4	–	service bit

5.2.4.1 Synchronization Procedure

For multiframe synchronization, the terminal framing bits (FT-bits) are observed. The synchronous state is reached if at least one terminal framing candidate is definitely found, or the synchronizer is forced to lock onto the next available candidate (FMR0.FRS).

5.2.5 12-Frame Multiframe (D4 or SF Format, T1/J1)

Normally, this kind of multiframe structure only makes sense when using the CAS robbed-bit signaling. The multiframe alignment signal is located at the FS-bit position of every other frame (refer to **Table 35**).

Table 35 12-Frame Multiframe Structure (T1/J1)

Frame Number	F_T	F_S	Signaling Channel Designation
1	1	–	
2	–	0	
3	0	–	
4	–	0	
5	1	–	
6	–	1	A
7	0	–	
8	–	1	
9	1	–	
10	–	1	
11	0	–	
12	–	0	B

There are two possibilities of remote alarm (yellow alarm) indication:

- Bit 2 = 0 in each time slot of a frame, selected with bit FMR0.SRAF = 0
- The last bit of the multiframe alignment signal (bit 1 of frame 12) changes from ’0’ to ’1’, selected with bit FMR0.SRAF = 1.

5.2.5.1 Synchronization Procedure

In the synchronous state terminal framing (FT-bits) and multiframing (FS-bits) are observed, independently. Further reaction on framing errors depends on the selected synchronization/resynchronization procedure (by bit FMR2.SSP):

- FMR2.SSP = 0: terminal frame and multiframe synchronization are combined.
  Two errors within 4/5/6 framing bits (by bits FMR4.SSC1/0) of one of the above leads to the asynchronous state for terminal framing **and** multiframing. Additionally to the bit FRS0.LFA, loss of multiframe alignment is reported by bit FRS0.LMFA.
  The resynchronization procedure starts with synchronizing upon the terminal framing. If the pulse framing has been regained, the search for multiframe alignment is initiated. Multiframe synchronization has been regained after two consecutive correct multiframe patterns have been received.
- FMR2.SSP = 1: terminal frame and multiframe synchronization are separated
  Two errors within 4/5/6 terminal framing bits lead to the same reaction as described

above for the “combined” mode.
Two errors within 4/5/6 multiframing bits lead to the asynchronous state only for the multiframing. Loss of multiframe alignment is reported by bit FRS0.LMFA. The state of terminal framing is not influenced.
Now, the resynchronization procedure includes only the search for multiframe alignment. Multiframe synchronization has been regained after two consecutive correct multiframe patterns have been received.

5.2.6 Extended Superframe (F24 or ESF Format, T1/J1)

The use of the first bit of each frame for the multiframe alignment word, the data link bits, and the CRC bits is shown in **Table 36** on page **149**.

Table 36 Extended Superframe Structure (F24, ESF; T1/J1)

Multiframe Frame Number	F-Bits				Signaling Channel Designation
	Multiframe Bit Number	Assignments			
		FAS	DL	CRC	
1	0	–	m	–	
2	193	–	–	e_1	
3	386	–	m	–	
4	579	0	–	–	
5	772	–	m	–	
6	965	–	–	e_2	A
7	1158	–	m	–	
8	1351	0	–	–	
9	1544	–	m	–	
10	1737	–	–	e_3	
11	1930	–	m	–	
12	2123	1	–	–	B
13	2316	–	m	–	
14	2509	–	–	e_4	
15	2702	–	m	–	
16	2895	0	–	–	
17	3088	–	m	–	
18	3231	–	–	e_5	C
19	3474	–	m	–	
20	3667	1	–	–	
21	3860	–	m	–	
22	4053	–	–	e_6	
23	4246	–	m	–	
24	4439	1	–	–	D

5.2.6.1 Synchronization Procedures

For multiframe synchronization the FAS-bits are observed. Synchronous state is reached if at least one framing candidate is definitely found, or the synchronizer is forced to lock onto the next available candidate (FMR0.FRS).

In the synchronous state the framing bits (FAS-bits) are observed. The following conditions selected by FMR4.SSC1/0 lead to the asynchronous state:

- two errors within 4/5/6 framing bits
- two or more erroneous framing bits within one ESF multiframe
- more than 320 CRC6 errors per second interval (FMR5.SSC2)
- 4 incorrect (1 out of 6) consecutive multiframes independent of CRC6 errors.

There are four multiframe synchronization modes selectable using FMR2.MCSP and FMR2.SSP.

- FMR2.MCSP/SSP = 00: In the synchronous state, the setting of FMR0.FRS or FMR0.EXLS resets the synchronizer and initiates a new frame search. The synchronous state is reached again, if there is only one definite framing candidate. In the case of repeated apparent simulated candidates, the synchronizer remains in the asynchronous state.
  In asynchronous state, setting bit FMR0.FRS induces the synchronizer to lock onto the next available framing candidate if there is one. At the same time the internal framing pattern memory is cleared and other possible framing candidates are lost.
- FMR2.MCSP/SSP = 01: Synchronization is achieved when 3 consecutive multiframe pattern are correctly found independent of the occurrence of CRC6 errors. If only one or two consecutive multiframe pattern were detected the QuadFALC stays in the asynchronous state, searching for a possible additionally available framing pattern. This procedure is repeated until the framer has found three consecutive multiframe pattern in a row.

- FMR2.MCSP/SSP = 10: This mode has been added in order to be able to choose multiple framing pattern candidates step by step. I.e. if in synchronous state the CRC error counter indicates that the synchronization might have been based on an alias framing pattern, setting of FMR0.FRS leads to synchronization on the next candidate available. However, only the previously assumed candidate is discarded in the internal framing pattern memory. The latter procedure can be repeated until the framer has locked on the right pattern (no extensive CRC errors).
  The synchronizer is reset completely and initiates a new frame search, if there is no multiframing found. In this case bit FRS0.FSRF toggles.

- FMR2.MCSP/SSP = 11: Synchronization including automatic CRC6 checking
  Synchronization is achieved when framing pattern are correctly found and the CRC6 checksum is received without an error. If the CRC6 check failed on the assumed

framing pattern the QuadFALC stays in the asynchronous state, searching for a possible available framing pattern. This procedure is repeated until the framer has locked on the right pattern. This automatic synchronization mode has been added in order to reduce the microprocessor load.

5.2.6.2 Remote Alarm (yellow alarm) Generation/Detection

Remote alarm (yellow alarm) is indicated by the periodical pattern '1111 1111 0000 0000 …' in the DL-bits (T1 mode, RC0.SJR = 0). Remote alarm is declared even in the presence of a bit error rate of up to 10^{-3}. The alarm is reset when the 'yellow alarm pattern' no longer is detected.

Depending on bit RC0.SJR = 1 the QuadFALC generates and detects the remote alarm according to JT G. 704. In the DL-bit position 16 continuous '1' are transmitted if FMR0.SRAF = 0 and FMR4.XRA = 1.

5.2.6.3 CRC6 Generation and Checking (T1/J1)

Generation and checking of CRC6 bits transmitted/received in the E1 to 6 bit positions is done according to ITU-T G.706. The CRC6 checking algorithm is enabled by bit FMR1.CRC. If not enabled, all check bits in the transmit direction are set. In the synchronous state received CRC6 errors are accumulated in a 16 bit error counter and are additionally indicated by an interrupt status.

- CRC6 inversion

If enabled by bit RC0.CRCI, all CRC bits of one outgoing extended multiframe are automatically inverted in case a CRC error is flagged for the previous received multiframe. Setting the bit RC0.XCRCI inverts the CRC bits before transmitted to the distant end. This function is logically ored with RC0.CRCI.

- CRC6 generation/checking according to JT G.706

Setting of RC0.SJR the QuadFALC generates and checks the CRC6 bits according to JT G.706. The CRC6 checksum is calculated including the FS/DL-bits. In synchronous state CRC6 errors increment an error counter.

5.2.7 72-Frame Multiframe (SLC96 Format, T1/J1)

The 72-multiframe is an alternate use of the FS-bit pattern and is used for carrying data link information. This is done by stealing some of redundant multiframing bits after the transmission of the 12-bit framing header (refer to **Figure 37** on page **153**). The position of A and B signaling channels (robbed bit signaling) is defined by zero-to-one and one-to-zero transitions of the FS-bits and is continued when the FS-bits are replaced by the data link bits.

Remote alarm (yellow alarm) is indicated by setting bit 2 to zero in each time slot. An additional use of the D-bits for alarm indication is user defined and must be done externally.

5.2.7.1 Synchronization Procedure

In the synchronous state terminal framing (FT-bits) and multiframing (FS-bits of the framing header) are observed independently. Further reaction on framing errors depends on the selected synchronization/resynchronization procedure (by bit FMR2.SSP):

- FMR2.SSP = 0: terminal frame and multiframe synchronization are combined
  Two errors within 4/5/6 framing bits (by bits FMR4.SSC1/0) of one of the above lead to the asynchronous state for terminal framing **and** multiframing. Additionally to The resynchronization procedure starts with synchronizing upon the terminal framing. If the pulse framing has been regained, the search for multiframe alignment is initiated. Multiframe synchronization has been regained after two consecutive correct multiframe patterns have been received.
- FMR2.SSP = 1: terminal frame and multiframe synchronization are separated
  Two errors within 4/5/6 terminal framing bits lead to the same reaction as described above for the “combined” mode.
  Two errors within 4/5/6 multiframing bits lead to the asynchronous state only for the multiframing. Loss of multiframe alignment is reported by bit FRS0.LMFA. The state of terminal framing is not influenced.
  Now, the resynchronization procedure includes only the search for multiframe alignment. Multiframe synchronization has been regained after two consecutive correct multiframe patterns have been received.

Table 37 72-Frame Multiframe Structure (T1/J1)

Frame Number	F_T	F_S	Signaling Channel Designation
1	1	–	
2	–	0	
3	0	–	
4	–	0	
5	1	–	
6	–	1	A
7	0	–	
8	–	1	
9	1	–	
10	–	1	
11	0	–	
12	–	0	B
13	1	–	
14	–	0	
15	0	–	
16	–	0	
17	1	–	
18	–	1	A
19	0	–	
20	–	1	
21	1	–	
22	–	1	
23	0	–	
24	–	D	B
25	1	–	
26	–	D	
27	.	.	
28	.	.	
.	1	–	
66	–	D	A
67	0	–	
68	–	D	
69	1	–	
70	–	D	
71	0	–	
72	–	0	B

5.2.8 Summary of Frame Conditions (T1/J1)

Table 38 Summary Frame Recover/Out of Frame Conditions (T1/J1)

Format	Frame Recover Condition	Out of Frame Condition
F4	only one FT pattern found, optional forcing on next available FT framing candidate	2 out of 4/5/6 incorrect FT-bits
F12 (D4) and F72 (SLC96)	FMR2.SSP = 0: Combined FT + FS framing search: First searching for FT pattern with optional forcing on next available framing candidates and then for 2 consecutive correct FS pattern[1]. FMR2.SSP = 1: Separated FT + FS pattern search: Loss of FT framing starts first search for FT and then for 2 consecutive correct FS pattern[1]. Loss of FS framing starts only the FS pattern[1] search.	FMR2.SSP = 0: 2 out of 4/5/6 incorrect FT- or FS-bits FMR2.SSP = 1: 2 out of 4/5/6 incorrect FT-bits searched in FT and FS framing bits, 2 out of 4/5/6 incorrect FS-bits searched only the FS framing.
F24 (ESF)	FMR2.MCSP/SSP = 00: only one FAS pattern found, optional forcing on next available FAS framing candidate with discarding of all remaining framing candidates. FMR2.MCSP/SSP = 01: 3 consecutive correct multiframing found independent of CRC6 errors. FMR2.MCSP/SSP = 10: choosing multiple framing pattern step by step, optional forcing on next available FAS framing pattern with discarding only of the previous assumed framing candidate. FMR2.MCSP/SSP = 11: FAS framing correctly found and CRC6 check error free.	2 out of 4/5 incorrect FAS-bits or 2 out of 6 incorrect FAS-bits per multiframe or 4 consecutive incorrect multiframing pattern or more than 320 CRC6 errors per second interval

[1] In F12 (D4) format bit 1 in frame 12 is excluded from the synchronization process.

5.3 Additional Receive Framer Functions (T1/J1)

5.3.1 Error Performance Monitoring and Alarm Handling

Alarm Indication Signal: Detection and recovery is flagged by bit FRS0.AIS and ISR2.AIS. Transmission is enabled by bit FMR1.XAIS.

Loss of Signal: Detection and recovery is flagged by bit FRS0.LOS and ISR2.LOS.

Remote Alarm Indication: Detection and release is flagged by bit FRS0.RRA and ISR2.RA/RAR. Transmission is enabled by bit FMR4.XRA.

Excessive Zeros: Detection is flagged by bit FRS1.EXZD.

Pulse Density Violation: Detection is flagged by bit FRS1.PDEN and ISR0.PDEN.

Transmit Line Shorted: Detection and release is flagged by bit FRS1.XLS and ISR1.XLSC.

Transmit Ones Density: Detection and release is flagged by bit FRS1.XLO and ISR1.XLSC.

Table 39 Summary of Alarm Detection and Release (T1/J1)

Alarm	Detection Condition	Clear Condition
Red Alarm or Loss of Signal (LOS)	no transitions (logical zeros) in a programmable time interval of 16 to 4096 consecutive pulse periods. Programmable receive input signal threshold	programmable number of ones (1 to 256) in a programmable time interval of 16 to 4096 consecutive pulse periods. A one is a signal with a level above the programmed threshold. or the pulse density is fulfilled and no more than 15 contiguous zeros during the recovery interval are detected.
Blue Alarm or Alarm Indication Signal (AIS)	FMR4.AIS3 = 0: less than 3 zeros in 12 frames or 24 frames (ESF), FMR4.AIS3 = 1: less than 4 zeros in 12 frames or less than 6 zeros in 24 frames (ESF)	active for at least one multiframe. FMR4.AIS3 = 0: more than 2 zeros in 12 or 24 frames (ESF), FMR4.AIS3 = 1: more than 3 zeros in 12 frames or more than 5 zeros in 24 frames (ESF)

Table 39 Summary of Alarm Detection and Release (T1/J1) (cont'd)

Alarm	Detection Condition	Clear Condition
Yellow Alarm or Remote Alarm (RRA)[1)]	RC1.RRAM = 0: bit 2 = 0 in 255 consecutive time slots or FS-bit = 1 of frame12 in F12 (D4) format or 8×1,8×0 in the DL channel (ESF) RC1.RRAM = 1: bit 2 = 0 in every time slot per frame or FS-bit = 1 of frame12 in F12 (D4) format or 8×1,8×0 in the DL channel (ESF)	RC1.RRAM = 0: set conditions no longer detected. RC1.RRAM = 1: bit 2 = 0 not detected in 3 consecutive frames or FS-bit not detected in 3 consecutive multiframes or 8×1,8×0 not detected for 3 times in a row (ESF).
Excessive Zeros (EXZD)	more than 7 (B8ZS code) or more than 15 (AMI code) contiguous zeros	Latched Status: cleared on read
Pulse Density Violation (PDEN)	less than N ones in each and every time window of 8×(N+1) time slots with N taking all values of 1 to 23 or more than 15 consecutive zeros	Latched Status: cleared on read
Transmit Line Short (XLS)	more than 3 pulse periods with highly increased transmit line current on XL1/2	transmit line current limiter inactive
Transmit Ones Density (XLO)	32 consecutive zeros in the transmit data stream on XL1/2	Cleared with each transmitted pulse

1) RRA detection operates in the presence of 10^{-3} bit error rate.

5.3.2 Auto Modes

- Automatic remote alarm (Yellow Alarm) access
  If the receiver has lost its synchronization (FRS0.LFA) a remote alarm (yellow alarm) is sent to the distant end automatically, if enabled by bit FMR2.AXRA. In synchronous state the remote alarm bit is removed.
- Automatic AIS to system interface
  In asynchronous state the synchronizer enforces an AIS to the receive system interface automatically. However, received data is switched through transparently if bit FMR2.DAIS is set.

- Automatic clock source switching
  In slave mode (LIM0.MAS = 0) the DCO-R synchronizes on the recovered route clock. In case of loss of signal (LOS) the DCO-R switches to master mode automatically. If bit CMR1.DCS is set, automatic switching from RCLK to SYNC is disabled.
- Automatic freeze signaling:
  Updating of the received signaling information is controlled by the freeze signaling status. The freeze signaling status is activated automatically, if a loss of signal or a loss of multiframe alignment or a receive slip occurs. The internal signaling buffer RS(12:1) is frozen. Optionally automatic freeze signaling is disabled by setting bit SIC3.DAF = 1.

5.3.3 Error Counter

The QuadFALC offers six error counters where each of them has a length of 16 bit. They record code violations, framing bit errors, CRC6 bit errors, errored blocks and the number of received multiframes in asynchronous state or the changes of frame alignment (COFA). Counting of the multiframes in asynchronous state and of the COFA parameter is done in a 6/2-bit counter. Each of the error counters is buffered. Buffer update is done in two modes:

- one second accumulation
- on demand using handshake with writing to the DEC register.

In the one second mode an internal/external one-second timer updates these buffers and resets the counter to accumulate the error events in the next one-second period. The error counter can not overflow. Error events occurring during error counter reset are not be lost.

5.3.4 Errored Second

The QuadFALC supports the error performance monitoring by detecting the following alarms or error events in the received data:
framing errors, CRC errors, code violations, loss of frame alignment, loss of signal, alarm indication signal, receive and transmit slips.
With a programmable interrupt mask register ESM all these alarms or error events can generate an Errored Second Interrupt (ISR3.ES) if enabled.

5.3.5 Second Timer

Additionally a one second timer interrupt can be generated internally to indicate that the enabled alarm status bits or the error counters have to be checked. The one second timer signal is output on port SEC/FSC (GPC1.CSFP1/0). Optionally synchronization to an external second timer is possible which has to be provided at pin SEC/FSC. Selecting the external second timer is done with GCR.SES. Refer also to register GPC1 for input/output selection.

5.3.6 Clear Channel Capability

For support of common T1 applications, clear channels can be specified through the 3-byte register bank CCB(3:1). In this mode the contents of selected transmit time slots are not overwritten by internally or externally sourced bit-robbing and zero code suppression (B7 stuffing) information.

5.3.7 In-Band Loop Generation and Detection

The QuadFALC generates and detects a framed or unframed in-band loop up/activate (00001) and down/deactivate (001) pattern according to ANSI T1.403 with bit error rates as high as 10^{-2}. Framed or unframed in-band loop code is selected by LCR1.FLLB. Replacing the in-band loop codes with transmit data is done by FMR5.XLD/XLU.
The QuadFALC also offers the ability generating and detecting of a flexible in-band loop up and down pattern (LCR1.LLBP = 1). The loop up and loop down pattern is individual programmable from 2 to 8 bit in length (LCR1.LAC1/0 and LCR1.LDC1/0). Programming of loop codes is done in registers LCR2 and LCR3.
Status and interrupt status bits inform the user whether loop up or loop down code was detected.

5.3.8 Transparent Mode

The transparent modes are useful for loopbacks or for routing data unchanged through the QuadFALC.

In receive direction, transparency for ternary or dual/single rail unipolar data is always achieved if the receiver is in the synchronous state. All bits in F-bit position of the incoming multiframe are forwarded to RDO and inserted in the FS/DL time slot or in the F-bit position. In asynchronous state the received data is switched through transparently if bit FMR2.DAIS is set. Setting of bit LOOP.RTM disconnects control of the elastic buffer from the receiver. The elastic buffer is now in a “free running” mode without any possibility to update the time slot assignment to a new frame position in case of resynchronization of the receiver. Together with FMR2.DAIS this function is used to realize undisturbed transparent reception.

Setting bit FMR4.TM switches the QuadFALC in transmit transparent mode:

In transmit direction bit 8 of the FS/DL time slot from the system highway (XDI) is inserted in the F-bit position of the outgoing frame. For complete transparency the internal signaling controller, idle code generation, AIS alarm generation, single channel and payload loop back has to be disabled and ’cleared channels’ have to be defined by registers CCB1…3.

5.3.9 Pulse Density Detection

The QuadFALC examines the receive data stream on the pulse density requirement which is defined by ANSI T1. 403. More than 14 consecutive zeros or less than N ones

in each and every time window of 8×(N+1) data bits where N = 23 are detected. Violations of these rules are indicated by setting the status bit FRS1.PDEN and the interrupt status bit ISR0.PDEN. Generation of the interrupt status is programmed either with the detection or with any change of state of the pulse density alarm (GCR.SCI).

5.4 Transmit Path in T1/J1 Mode

5.4.1 Transmitter (T1/J1)

The serial bit stream is then processed by the transmitter which has the following functions:

- Frame/multiframe synthesis of one of the four selectable framing formats
- Insertion of service and data link information
- AIS generation (blue alarm)
- Remote alarm (yellow alarm) generation
- CRC generation and insertion of CRC bits
- CRC bits inversion in case of a previously received CRC error or in case of activating per control bit
- Generation of loop up/down code
- Idle code generation per DS0

The frame/multiframe boundaries of the transmitter can be synchronized externally by using the $\overline{\text{SYPX}}$/XMFS pin. Any change of the transmit time slot assignment subsequently produces a change of the framing bit positions on the line side. This feature is required if signaling and data link bits are routed through the switching network and are inserted in transmit direction by the system interface.

In loop-timed configuration (LIM2.ELT) disconnecting the control of the transmit system highway from the transmitter is done by setting FMR5.XTM. The transmitter is now in a free running mode without any possibility to update the multiframe position in case of changing the transmit time slot assignment. The FS/DL-bits are generated independent of the transmit system interface. For proper operation the transmit elastic buffer size should be programmed to 2 frames.

The contents of selectable time slots is overwritten by the pattern defined by register IDLE. The selection of “idle channels” is done by programming the three-byte registers ICB(3:1).

If AMI coding with zero code suppression (B7-stuffing) is selected, “clear channels” without B7-stuffing can be defined by programming registers CCB(3:1).

5.4.2 Transmit Line Interface (T1/J1)

The analog transmitter transforms the unipolar bit stream to ternary (alternate bipolar) return to zero signals of the appropriate programmable shape. The unipolar data is provided by pin XDI and the digital transmitter.

Similar to the receive line interface three different data types are supported:

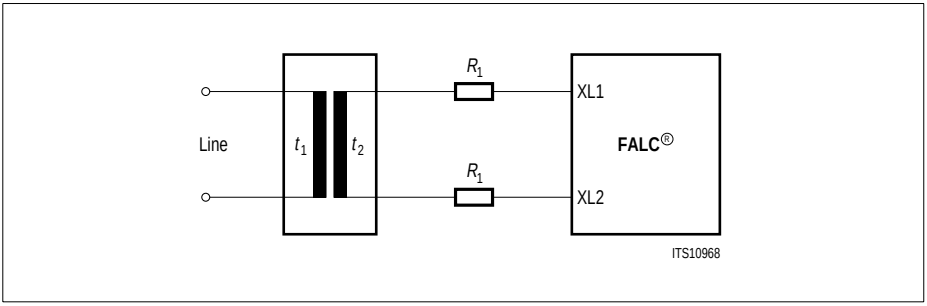


Figure 55 Transmitter Configuration (T1/J1)

Table 40 Recommended Transmitter Configuration Values (T1/J1)

Parameter	T1	J1
Characteristic Impedance [Ω]	100	110
R_1 (± 1%) [Ω]	2[1)]	
t2 : t1	1 : 2.4	

1) This value refers to an ideal transformer without any parasitics. Any transformer resistance or other parasitic resistances have to be taken into account when calculating the final value of the output serial resistors.

- Ternary Signal
  Single rail data is converted into a ternary signal which is output on pins XL1 and XL2. Selection between B8ZS or simple AMI coding with zero code suppression (B7 stuffing) is provided. B7 stuffing can be disabled on a per time slot basis (Clear Channel capability). Selected by FMR0.XC1/0 and LIM1.DRS = 0.
- Dual rail data PCM(+), PCM(-) at multifunction ports XDOP and XDON with 50% or 100% duty cycle and with programmable polarity. Line coding is done in the same way as in ternary interface mode. Selected by FMR0.XC1 = 1 and LIM1.DRS = 1.
- Unipolar data on port XOID is transmitted in NRZ (non return to zero) with 100% duty cycle or in CMI code with or without (SIC3.CMI) preprocessed by B8ZS coding to a fibre optical interface. Clocking off data is done with the rising edge of the transmit clock XCLK (1544 kHz) and with a programmable polarity. Selection is done by FMR0.XC1 = 0 and LIM1.DRS = 1.

5.4.3 Transmit Jitter Attenuator (T1/J1)

The transmit jitter attenuator DCO-X circuitry generates a 'jitter free' transmit clock and meets the following requirements: PUB 62411, PUB 43802, TR-TSY 009,TR-TSY 253, TR-TSY 499 and ITU-T I.431 and G.703. The DCO-X circuitry works internally with the

same high frequency clock as the receive jitter attenuator. It synchronizes either to the working clock of the transmit backplane interface or the clock provided on pin TCLK or the receive clock RCLK (remote loop/loop-timed). The DCO-X attenuates the incoming jitter starting at 6 Hz with 20 dB per decade fall off. With the jitter attenuated clock, which is directly depending on the phase difference of the incoming clock and the jitter attenuated clock, data is read from the transmit elastic buffer (2 frames) or from the JATT buffer (2 frames, remote loop). Wander with a jitter frequency below 6 Hz is passed transparently.

The DCO-X accepts gapped clocks which are used in ATM or SDH/SONET applications. The jitter attenuated clock is output on pin XCLK.

In case of missing clock on pin SCLKX the DCO-X centers automatically, if selected by bit CMR2.DCOXC = 1.

The transmit jitter attenuator can be disabled. In that case data is read from the transmit elastic buffer with the clock sourced by pin TCLK (1.544 or 6.176 MHz). Synchronization between SCLKX and TCLK has to be done externally.

In the loop-timed clock configuration (LIM2.ELT) the DCO-X circuitry generates a transmit clock which is frequency synchronized on RCLK. In this configuration the transmit elastic buffer has to be enabled.

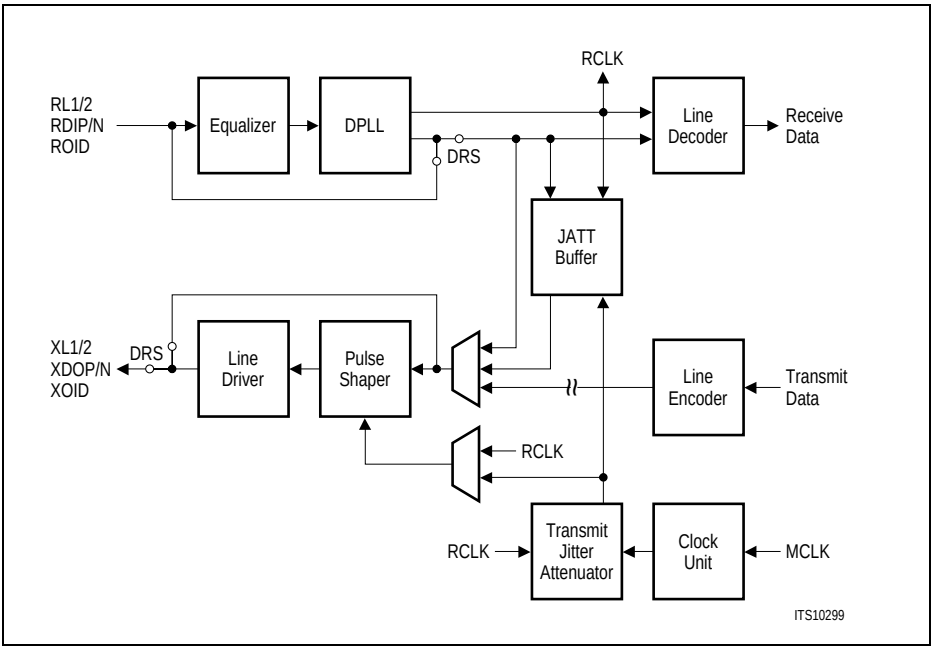


Figure 56 Clocking in Remote Loop Configuration (T1/J1)

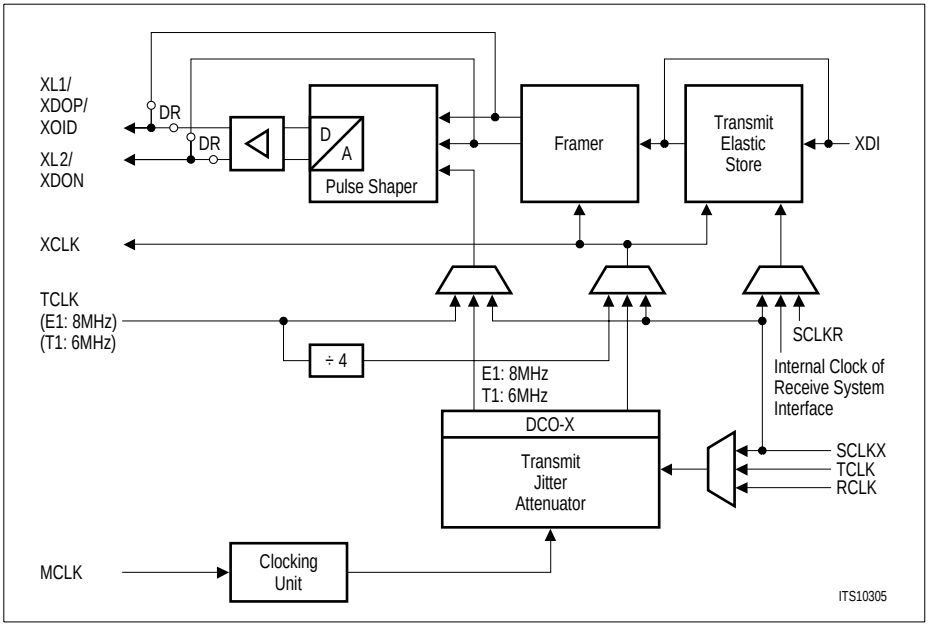


Figure 57 Transmit Clock System (T1/J1)

Note: DR = Dual Rail Interface
DCO-X Digital Controlled Oscillator Transmit

5.4.4 Transmit Elastic Buffer (T1/J1)

The transmit elastic store with a size of max. 2×193 bit (two frames) serves as a temporary store for the PCM data to adapt the system clock (SCLKX) to the internally generated clock for the transmit data, and to retranslate time slot structure used in the system to that of the line side. Its optimal start position is initiated when programming the transmit time slot offset values. A difference in the effective data rates of system side and transmit side lead to an overflow or underflow of the transmit memory. Thus, errors in data transmission to the remote end occur. This error condition (transmit slip) is reported to the microprocessor by interrupt status registers.
The received bit stream from pin XDI is optionally stored in the transmit elastic buffer. The memory is organized as the receive elastic buffer. Programming of the transmit buffer size is done by SIC1.XBS1/0:

- XBS1/0 = 00: bypass of the transmit elastic buffer
- XBS1/0 = 01: one frame buffer or 193 bits
  Maximum of wander amplitude (peak-to-peak): (1 UI = 648 ns)
  System interface clocking rate: modulo 2.048 MHz:

Maximum of wander: 70 UI in channel translation mode 0
Maximum of wander: 45 UI in channel translation mode 1
System interface clocking rate: modulo 1.544 MHz:
Maximum of wander: 74 UI
average delay after performing a slip: 96 bits

- XBS1/0 = 10: two frame buffer or 386 bits
  System interface clocking rate: modulo 2.048 MHz:
  142 UI in channel translation mode 0
  78 UI in channel translation mode 1
  System interface clocking rate: modulo 1.544 MHz:
  Maximum of wander: 140 UI
  average delay after performing a slip: 193 bits
- XBS1/0 = 11: short buffer or 96 bits:
  System interface clocking rate: modulo 2.048 MHz:
  Maximum of wander: 28 UI in channel translation mode 0; channel translation mode 1 not supported
  System interface clocking rate: modulo 1.544 MHz:
  Maximum of wander: 38 UI
  average delay after performing a slip: 48 bits

The functions of the transmit buffer are:

- Clock adaptation between system clock (SCLKX/R) and internally generated transmit route clock (XCLK) or externally sourced TCLK.
- Compensation of input wander and jitter.
- Frame alignment between system frame and transmit route frame
- Reporting and controlling of slips

Writing of received data from XDI is controlled by SCLKX/R and $\overline{\text{SYPX}}$/XMFS in combination with the programmed offset values for the transmit time slot/clock slot counters. Reading of stored data is controlled by the clock generated by DCO-X circuitry or the externally generated TCLK and the transmit framer. With the dejittered clock data is read from the transmit elastic buffer and are forwarded to the transmitter. Reporting and controlling of slips is automatically done according to the receive direction. Positive/negative slips are reported in interrupt status bits ISR4.XSP and ISR4.XSN.

A reinitialization of the transmit memory is done by reprogramming the transmit time slot counter XC1 and with the next $\overline{\text{SYPX}}$ pulse. After that, this memory has its optimal start position.

The frequency of the working clock for the transmit system interface is programmable by SIC1.SSC1/0 and SIC2.SSC2 in a range of 1.544 ... 12.352 MHz/2.048 ... 16.384 MHz. Generally the data or marker on the system interface are clocked off or latched on the rising or falling edge (SIC3.RESX) of the SCLKX clock. Some clocking rates allow transmission of time slots/marker in different channel phases. Each channel phase

which shall be latched on ports XDI and XP(A to D) is programmable by bits SIC2.SICS(2:0), the remaining channel phases are cleared or ignored respectively.

The following table gives an overview of the transmit buffer operating modes.

Table 41 Transmit Buffer Operating Modes (T1/J1)

Buffer Size	TS Offset programming	Slip performance
bypass	enabled	no
short buffer	disabled	yes
1 frame	enabled	yes
2 frames	enabled	yes

5.4.5 Programmable Pulse Shaper and Line Build-Out (T1/J1)

In long haul applications the transmit pulse masks are optionally generated according to FCC68 and ANSI T1. 403. To reduce the crosstalk on the received signals the QuadFALC offers the ability to place a transmit attenuator in the data path. Transmit attenuation is selectable from 0, -7.5, -15 or -22.5 dB (register LIM2.LBO2/1). ANSI T1. 403 defines only 0 to 15 dB.

The QuadFALC includes a programmable pulse shaper to satisfy the requirements of ANSI T1. 102, also various DS1, DSX-1 specifications are met. The amplitude of the pulse shaper is individually programmable by the microprocessor to allow a maximum of different pulse templates. The line length is selected by programming the registers XPM(2:0) as shown for typical values in **Table 65** on **Page 349**.

The transmitter requires an external step up transformer to drive the line.

5.4.6 Transmit Line Monitor (T1/J1)

The transmit line monitor compares the transmit line current on XL1 and XL2 with an on-chip transmit line current limiter. The monitor detects faults on the primary side of the transformer indicated by a highly increased transmit line current (more than 120 mA for at least 3 consecutive pulses sourced by V_{DDX}[1)]) and protects the device from damage by setting the transmit line driver XL1/2 into high impedance state automatically (if enabled by XPM2.DAXLT = 0). The current limiter checks the actual current value of XL1/2 and if the transmit line current drops below the detection limit the high impedance state is cleared.

Two conditions are detected by the monitor: transmit line ones density (more than 31 consecutive zeros) indicated by FRS1.XLO and transmit line high current indicated by FRS1.XLS. In both cases a transmit line monitor status change interrupt is provided.

1) shorts between XL1 or XL2 and V_{DDX} are not detected

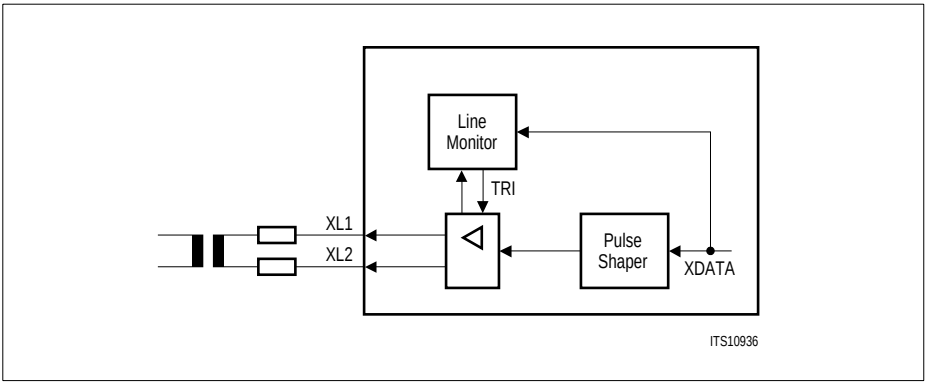


Figure 58 Transmit Line Monitor Configuration (T1/J1)

5.4.7 Transmit Signaling Controller (T1/J1)

Similar to the receive signaling controller the same signaling methods and the same time slot assignment are provided. The QuadFALC performs the following signaling and data link methods.

5.4.7.1 HDLC or LAPD access

The transmit signaling controller of the QuadFALC performs the flag generation, CRC generation, zero bit stuffing and programmable idle code generation. Buffering of transmit data is done in the 64 byte deep XFIFO. The signaling information is internally multiplexed with the data applied to port XDI or XSIG.
In signaling controller transparent mode, fully transparent data transmission without HDLC framing is performed. Optionally the QuadFALC supports the continuous transmission of the XFIFO contents.
Operating in HDLC or BOM mode “flags” or “idle” are transmitted as interframe timefill. The QuadFALC offers the flexibility to insert data during certain time slots. Any combinations of time slots can be programmed separately for the receive and transmit direction.

5.4.7.2 Support of Signaling System #7

The HDLC controller supports the signaling system #7 (SS7) which is described in ITU-Q.703. The following description assumes, that the reader is familiar with the SS7 protocol definition.

SS7 support must be activated by setting the MODE register. Data stored in the transmit FIFO (XFIFO) is sent automatically. The SS7 protocol is supported by the following hardware features in transmit direction:

- transmission of flags at the beginning of each Signaling Unit
- bit stuffing (zero insertion)
- calculation of the CRC16 checksum:
  The transmitter adds the checksum to each Signaling Unit.
  Each signaling unit written to the transmit FIFO (XFIFO, 2×32 bytes) is sent once or repeatedly including flags, CRC checksum and stuffed bits. After e.g. an MSU has been transmitted completely, the QuadFALC optionally starts sending of FISUs containing the forward sequence number (FSN) and the backward sequence number (BSN) of the previously transmitted signaling unit. Setting bit CCR5.AFX causes Fill In Signaling Units (FISUs) to be sent continuously, if no HDLC or Signaling Unit (SU) is to be transmitted from XFIFO. During update of XFIFO, automatic transmission is interrupted and resumed after update is completed. The internally generated FISUs contain FSN and BSN of the last transmitted signaling unit written to XFIFO.

  Using CMDR.XREP = 1, the contents of XFIFO can be sent continuously. Clearing of CMDR.XRES/SRES stops the automatic repetition of transmission. This function is also available for HDLC frames, so no flag generation, CRC byte generation and bit stuffing is necessary.
  Example: After an MSU has been sent repetitively and XREP has been cleared, FISUs are sent automatically.

5.4.7.3 CAS Bit-Robbing (T1/J1, serial mode)

The signaling controller inserts the bit stream either on the transmit line side or if external signaling is enabled on the transmit system side. Signaling data is sourced on port XSIG, which is selected by register PC(4:1) and FMR5.EIBR = 1.

In external signaling mode the signaling data is sampled with the working clock of the transmit system interface (SCLKX) together with the transmit synchronous pulse ($\overline{\text{SYPX}}$). Data on XSIG is latched in the bit positions 5 to 8 per time slot, bits 1 to 4 are ignored. The FS/DL-bit is sampled on port XSIG and inserted in the outgoing data stream. The received CAS multiframe is inserted frame aligned into the data stream on XDI. Data sourced by the internal signaling controller overwrites the external signaling data which must be valid during the last frame of a multiframe.
Internal multiplexing of data and signaling data can be disabled on a per time slot basis (clear channel capability). This is also valid when using the internal and external signaling mode.

5.4.7.4 CAS Bit-Robbing (T1/J1, µP access mode)

The signaling controller inserts the bit stream either on the transmit line side or if external signaling is enabled on the transmit system side. Signaling data is sourced internally from registers XS(12:1).
Internal multiplexing of data and signaling data can be disabled on a per time slot basis

(clear channel capability). This is also valid when using the internal and external signaling mode.

5.4.7.5 Data Link Access in ESF/F24 and F72 Format (T1/J1)

The DL-channel protocol is supported as follows:

- access is done on a multiframe basis through registers XDL(3:1) or
- HDLC access or transparent transmission (non HDLC mode) from XFIFO

The signaling information stored in the XFIFO is inserted in the DL-bits of frame 26 to 72 in F72 format or in every other frame in ESF format. Transmission can be done on a multiframe boundary (CCR1.XMFA = 1). Operating in HDLC or BOM mode “flags” or “idle” are transmitted as interframe timefill.

5.4.7.6 Periodical Performance Report in ESF Format (T1/J1)

According to ANSI T1.403 the QuadFALC can automatically generate the **P**eriodical **P**erformance **R**eport (PPR) and transmit it every second in the data link channel of the extended superframe format (ESF/F24 only). Automatic sending of this report can be enabled/disabled by the use of bit CCR5.EPR. A single report can be initiated manually at any time (by setting CMDR2.XPPR = 1).

Performance information is sampled every second and the report contains data of the last four seconds as shown in the following tables.

Table 42 Structure of Periodical Performance Report (T1/J1)[1)]

Octet No.	8	7	6	5	4	3	2	1	time
1	FLAG	=	01111110						
2	SAPI	=	001110				CR[2)]	EA=0	
3	TEI	=	0000000					EA=1	
4	CONTROL = 00000011 = unacknowledged frame								
5	G3	LV	G4	U1	U2	G5	SL	G6	t_0
6	FE	SE	LB	G1	R	G2	Nm	N1	
7	G3	LV	G4	U1	U2	G5	SL	G6	t_0-1 s
8	FE	SE	LB	G1	R	G2	Nm	N1	
9	G3	LV	G4	U1	U2	G5	SL	G6	t_0-2 s
10	FE	SE	LB	G1	R	G2	Nm	N1	
11	G3	LV	G4	U1	U2	G5	SL	G6	t_0-3 s
12	FE	SE	LB	G1	R	G2	Nm	N1	
13	FCS								
14	FCS								
15	FLAG	=	01111110						

1) The rightmost bit (bit 1) is transmitted first for all fields except for the two bytes of the FCS that are transmitted leftmost bit (bit 8) first.

2) reflects state of bit CCR5.CR

Table 43 Bit Functions in Periodical Performance Report[1)]

Bit Value	Interpretation
G1 = 1	number of CRC error events = 1
G2 = 1	1 < number of CRC error events ≤ 5
G3 = 1	5 < number of CRC error events ≤ 10
G4 = 1	10 < number of CRC error events ≤ 100
G5 = 1	100 < number of CRC error events ≤ 319
G6 = 1	number of CRC error events ≥ 320
SE = 1	Severely errored framing event ≥ 1 (FE shall be 0)
FE = 1	Frame synchronization bit error event ≥ 1 (SE shall be 0)
LV = 1	Line code violation event ≥ 1
SL = 1	Slip event ≥ 1
LB = 1	Payload loop back activated
U1	not used (default value = 0)
U2	not used (default value = 0)
R	not used (default value = 0)
NmNi	One-second report modulo 4 counter

1) according to ANSI T1.403

5.5 System Interface in T1/J1 Mode

The QuadFALC offers a flexible feature for system designers where for transmit and receive direction different system clocks and system pulses are necessary. The interface to the receive system highway is realized by two data buses, one for the data RDO and one for the signaling data RSIG. The receive highway is clocked by pin SCLKR, while the interface to the transmit system highway is independently clocked by pin SCLKX. The frequency of these working clocks and the data rate of 2.048/4.096/8.192/16.384/1.544/3.088/6.192/12.352 Mbit/s for the receive and transmit system interface is programmable by SIC1.SSC1/0, SIC2.SSC2 and SIC1.SSD1, FMR1.SSD0. Selectable system clock and data rates and their valid combinations are shown in the table below.

Table 44 System Clocking and Data Rates (T1/J1)

System Data Rate	Clock Rate 1.544/2.048 MHz	Clock Rate 3.088/4.096 MHz	Clock Rate 6.176/8.192 MHz	Clock Rate 12.352/16.384 MHz
1.544/2.048 Mbit/s	x	x	x	x
3.088/4.096 Mbit/s	--	x	x	x
6.176/8.192 Mbit/s	--	--	x	x
12.352/16.384 Mbit/s	--	--	--	x

x = valid, -- = invalid

Generally the data or marker on the system interface are clocked off or latched on the rising or falling edge (SIC3.RESR/X) of the SCLKR/X clock. Some clocking rates allow transmission of time slots in different channel phases. Each channel phase which shall be active on ports RDO, XDI, RP(A to D) and XP(A to D) is programmable by bit SIC2.SICS(2:0), the remaining channel phases are cleared or ignored.
The signals on pin $\overline{\text{SYPR}}$ in combination with the assigned time slot offset in register RC0 and RC1 define the beginning of a frame on the receive system highway. The signal on pin $\overline{\text{SYPX}}$ or XMFS together with the assigned time slot offset in register XC0 and XC1 define the beginning of a frame on the transmit system highway.

Adjusting the frame begin (time slot 0, bit 0) relative to $\overline{\text{SYPR/X}}$ or XMFS is possible in the range of 0 to 125 µs. The minimum shift of varying the time slot 0 begin can be programmed between 1 bit and 1/8 bit depending of the system clocking and data rate, e.g. with a clocking/data rate of 2.048 MHz shifting is done bit by bit, while running the QuadFALC with 16.384 MHz and 2.048 Mbit/s data rate it is done by 1/8 bit.

A receive frame marker RFM can be activated during any bit position of the entire frame. Programming is done with registers RC1/0. The pin function RFM is selected by PC(4:1).RPC(2:0) = 001. The RFM selection disables the internal time slot assigner, no offset programming is performed. The receive frame marker is active high for one 1.544/2.048 MHz cycle and is clocked off with the rising or falling edge of the clock which is in/output on port SCLKR (see SIC3.RESX/R).

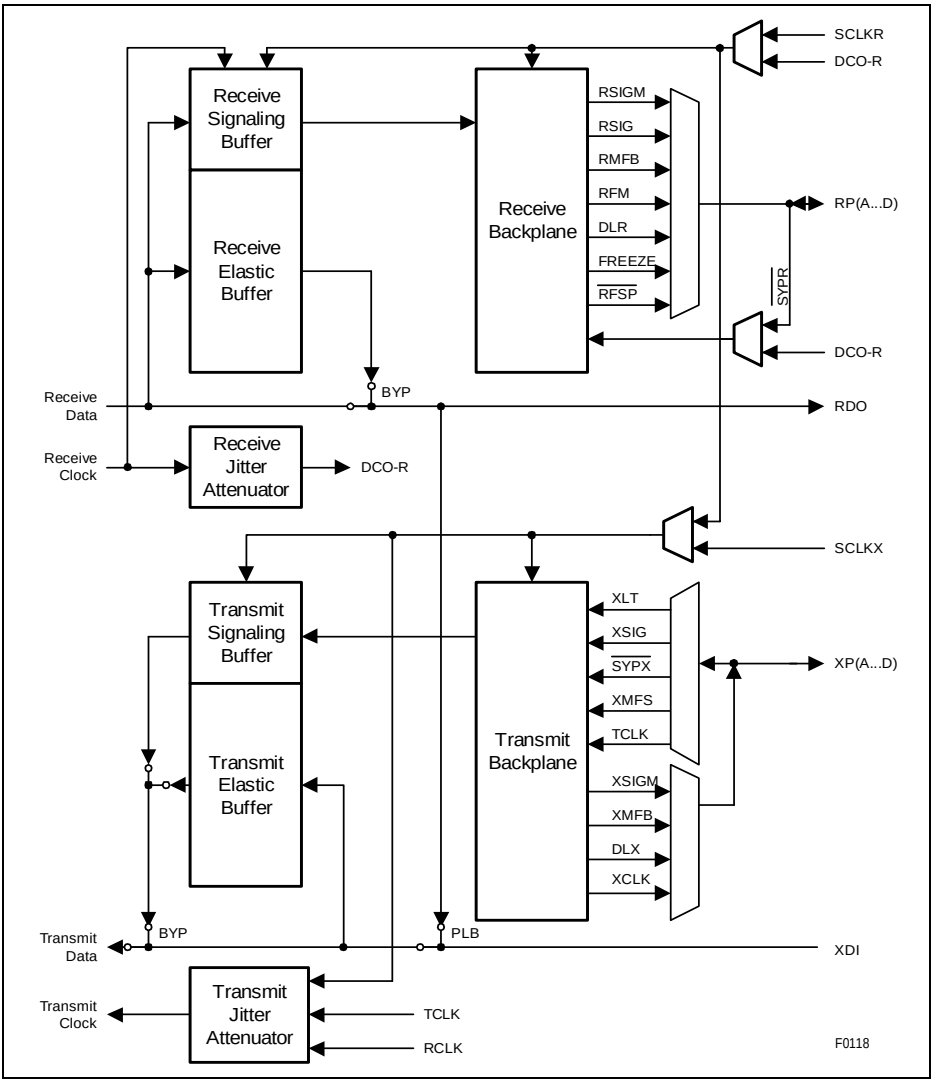


Figure 59 System Interface (T1/J1)

5.5.1 Receive System Interface (T1/J1)

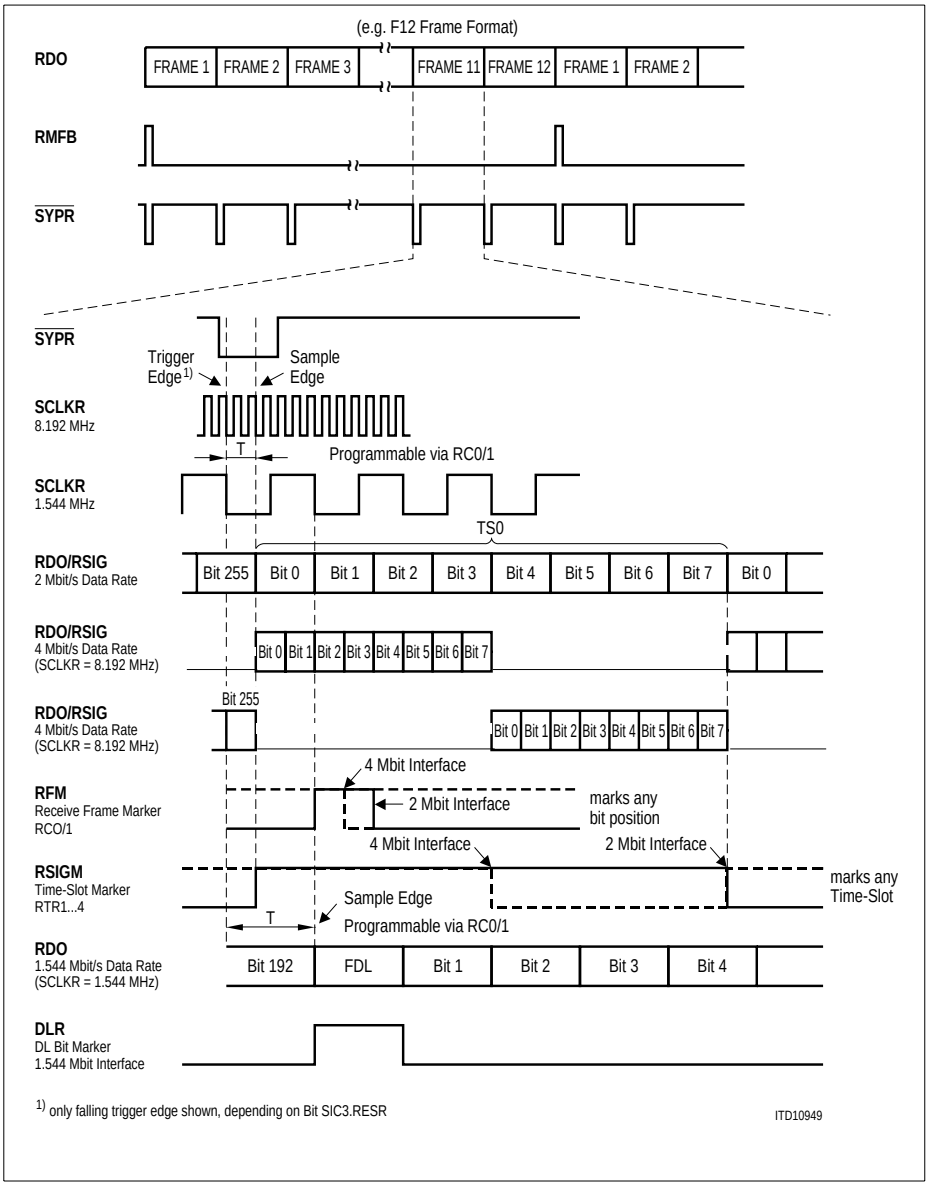


Figure 60 Receive System Interface Clocking (T1/J1)

5.5.1.1 Receive Offset Programming

Depending on the selection of the synchronization signals ($\overline{\text{SYPR}}$ or RFM), different calculation formulas are used to define the position of the synchronization pulses. These formulas are given below, see **Figure 61** to **Figure 64** for explanation. The pulse length of $\overline{\text{SYPR}}$ and RFM is always the basic T1/J1 bit width (648 ns) in 1.544-MHz mode or the E1 bit width (488 ns) in 2.048-MHz mode.

This chapter describes the system highway operation in 1.544-MHz mode only. If the system highway is operated in 2.048-MHz mode, the description given in **Chapter 4.5.1.1** on **Page 111** applies.

$\overline{\text{SYPR}}$ Offset Calculation

T: time between beginning of $\overline{\text{SYPR}}$ pulse and beginning of next frame (time slot 0, bit 0), measured in number of SCLKR clock intervals
maximum delay: $T_{max} = (193 \times SC/SD) - 1$

SD: basic data rate, 1.544 Mbit/s

SC: system clock rate; 1.544, 3.088, 6.176, or 12.352 MHz

X: programming value to be written to registers RC0 and RC1 (see **Page 347**).

$0 \le T \le 4$: $X = 4 - T + (7 \times SC/SD)$
$5 \le T \le T_{max}$: $X = (200 \times SC/SD) + 4 - T$

RFM Offset Calculation

MP: marker position of RFM, counting in SCLKR clock cycles (0 = F-bit)

SC = 1.544 MHz: $0 \le MP \le 192$
SC = 3.088 MHz: $0 \le MP \le 385$
SC = 6.176 MHz: $0 \le MP \le 771$
SC = 12.352 MHz: $0 \le MP \le 1543$

SD: basic data rate, 1.544 Mbit/s

SC: system clock rate; 1.544, 3.088, 6.176, or 12.352 MHz

X: programming value to be written to registers RC0 and RC1 (see **Page 347**).

$0 \le MP \le 193 \times (SC/SD) - 3$: $X = MP + 2 + (7 \times SC/SD)$
$193 \times (SC/SD) - 2 \le MP \le 193 \times (SC/SD) - 1$: $X = MP + 2 - (186 \times SC/SD)$

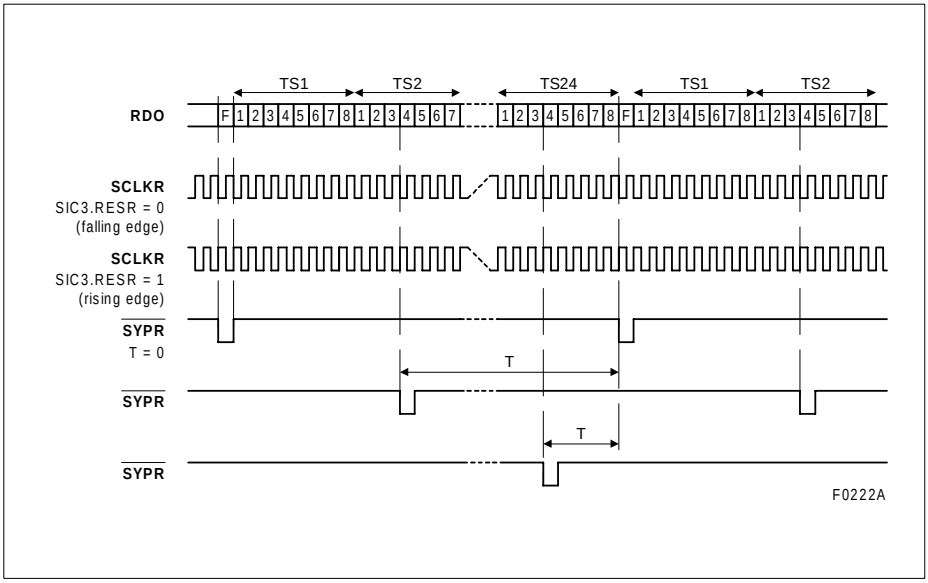


Figure 61 $\overline{\text{SYPR}}$ Offset Programming (1.544 Mbit/s, 1.544 MHz)

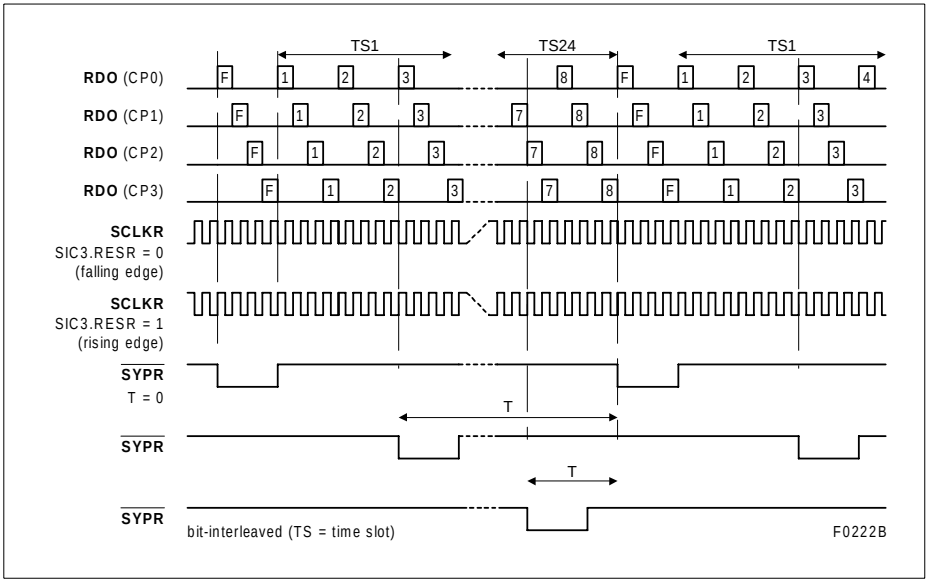


Figure 62 $\overline{\text{SYPR}}$ Offset Programming (6.176 Mbit/s, 6.176 MHz)

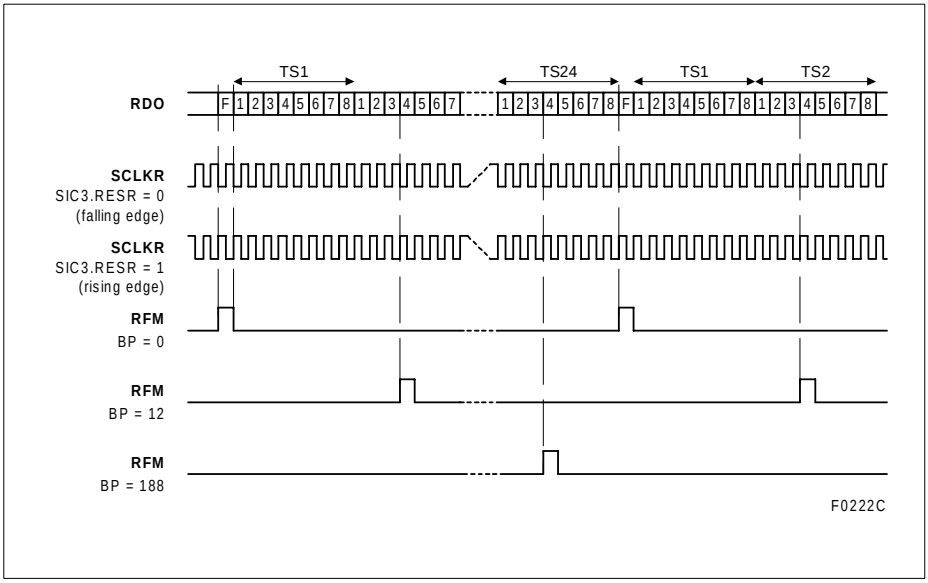


Figure 63 RFM Offset Programming (1.544 Mbit/s, 1.544 MHz)

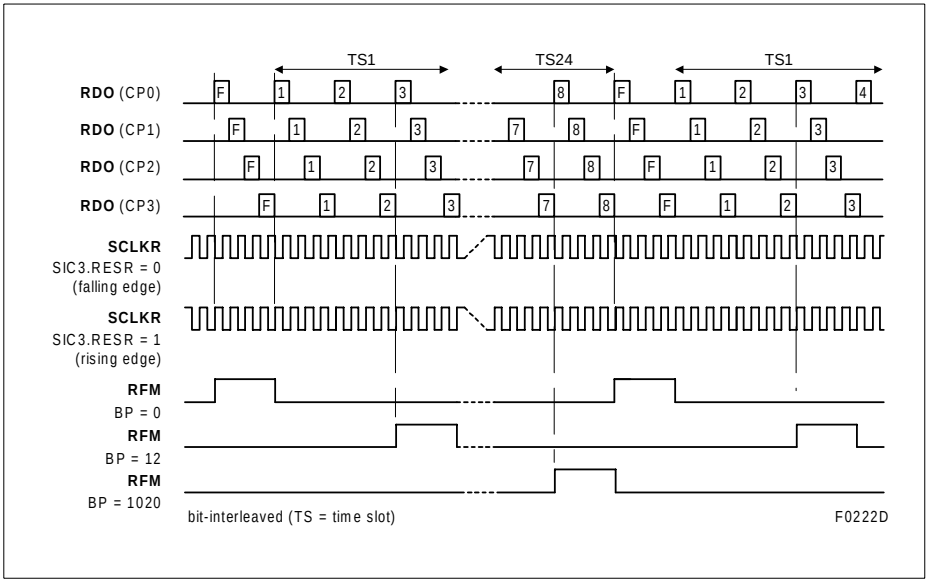


Figure 64 RFM Offset Programming (6.176 Mbit/s, 6.176 MHz)

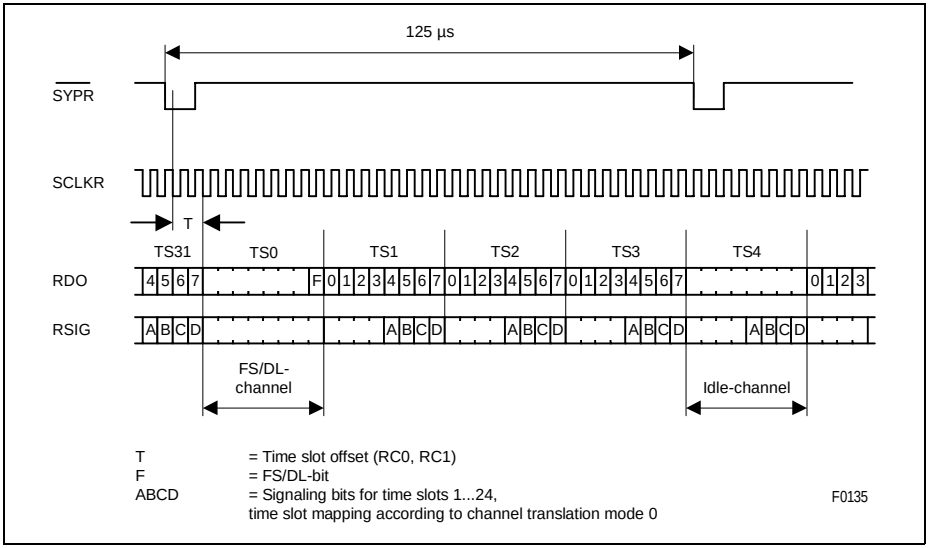


Figure 65 2.048 MHz Receive Signaling Highway (T1/J1)

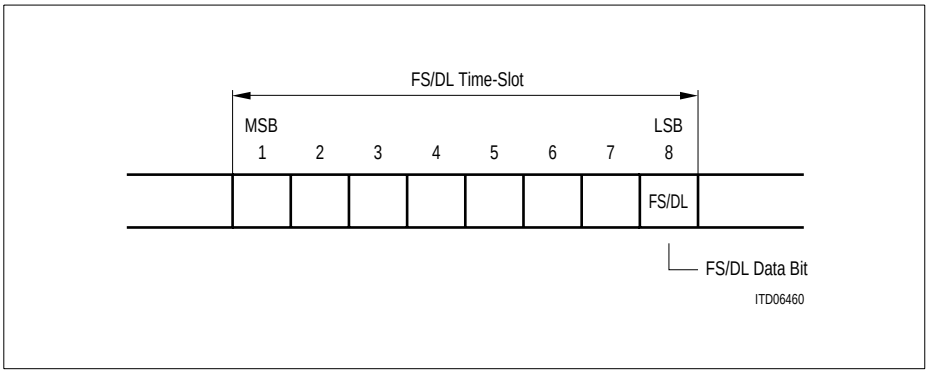


Figure 66 Receive FS/DL-Bits in Time Slot 0 on RDO (T1/J1)

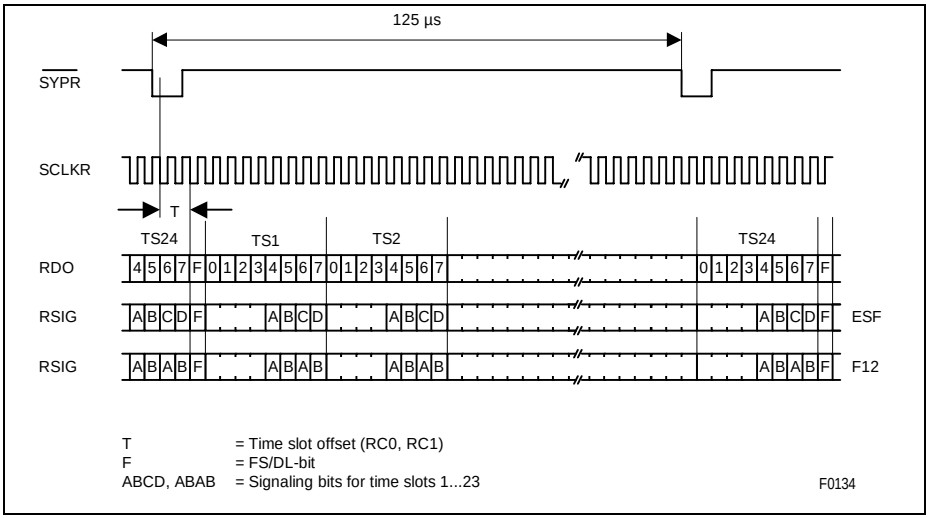


Figure 67 1.544 MHz Receive Signaling Highway (T1/J1)

5.5.2 Transmit System Interface (T1/J1)

Compared to the receive paths the inverse functions are performed for the transmit direction.

The interface to the transmit system highway is realized by two data buses, one for the data XDI and one for the signaling data XSIG. The time slot assignment is equivalent to the receive direction. All unequipped (idle) time slots are ignored.

Latching of data is controlled by the system clock (SCLKX or SCLKR) and the synchronization pulse ($\overline{\text{SYPX}}$/XMFS) in combination with the programmed offset values for the transmit time slot/clock slot counters XC1/0. The frequency of the working clock 2.048/4.096/8.192/16.384 MHz or 1.544/3.088/6.176/12.352 MHz for the transmit system interface is programmable by SIC1.SSC1/0 and SIC2.SSC2. Refer also **Table 44**.

The received bit stream on ports XDI and XSIG can be multiplexed internally on a time slot basis, if enabled by SIC3.TTRF = 1. The data received on port XSIG can be sampled if the transmit signaling marker XSIGM is active high. Data on port XDI is sampled if XSIGM is low for the corresponding time slot. Programming the XSIGM marker is done with registers TTR(4:1).

Note: XSIG is required in the last frame of a multiframe only and ignored in all other frames.

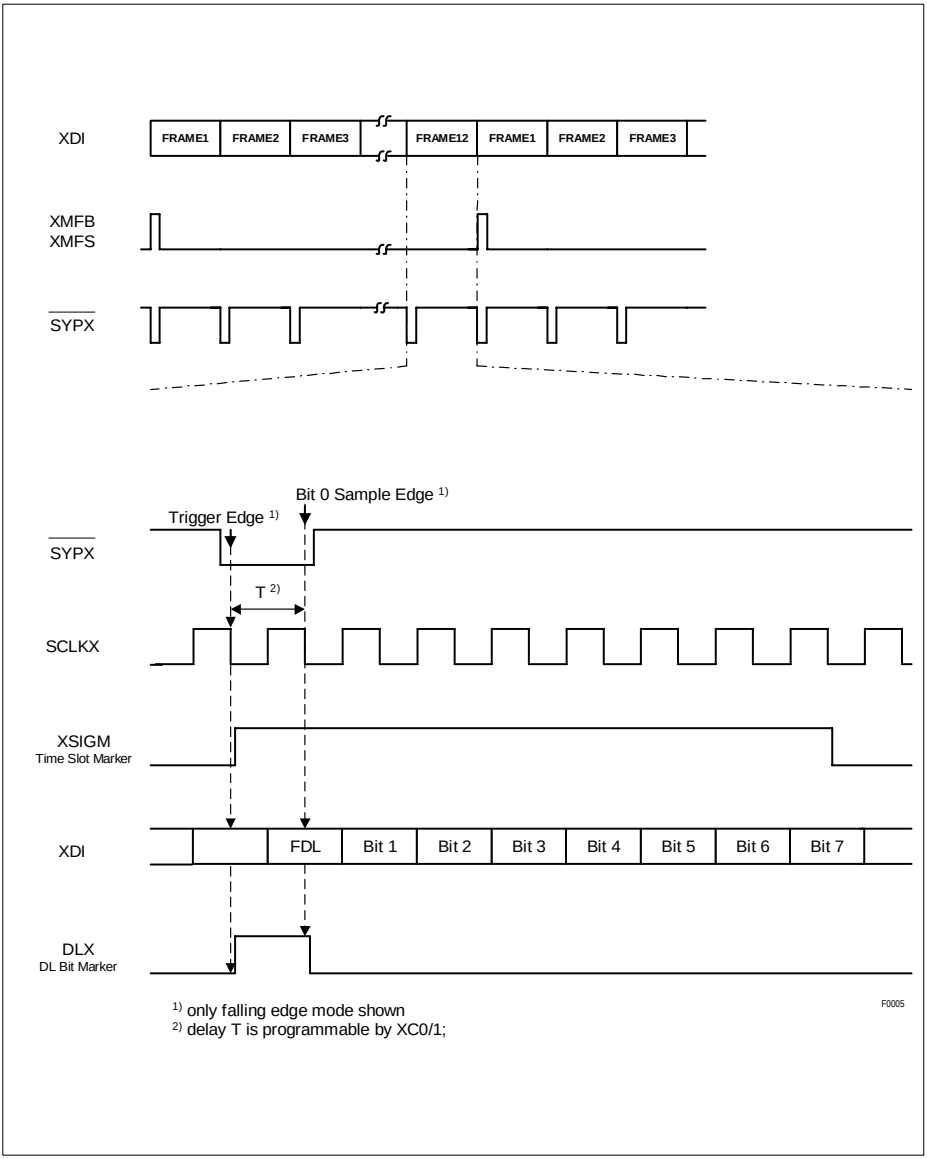


Figure 68 Transmit System Clocking: 1.544 MHz (T1/J1)

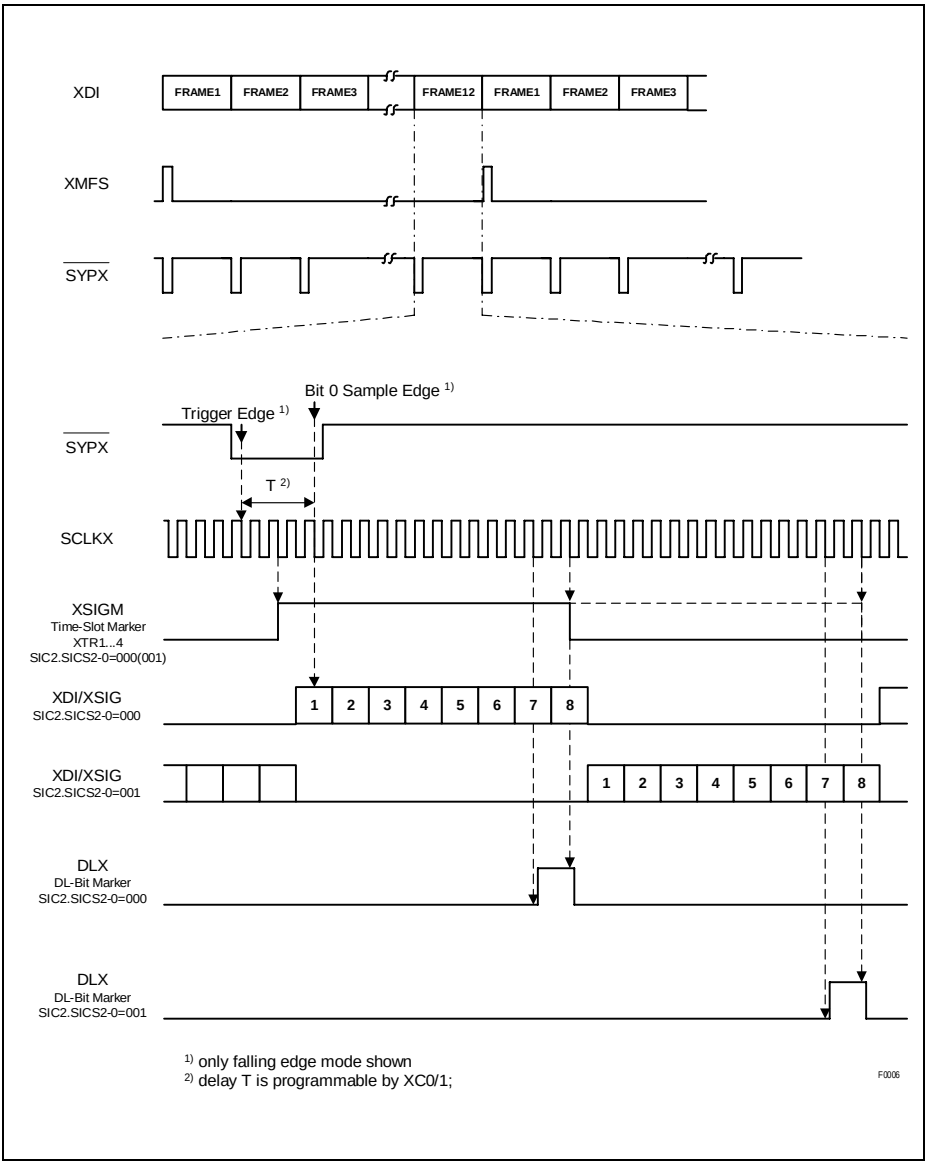


Figure 69 Transmit System Clocking: 8.192 MHz/4.096 Mbit/s (T1/J1)

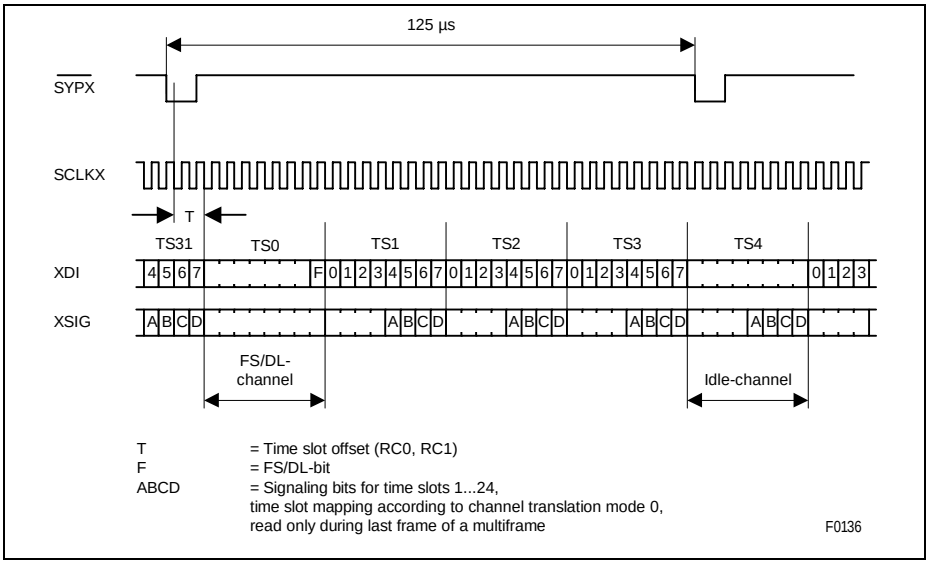


Figure 70 2.048 MHz Transmit Signaling Clocking (T1/J1)

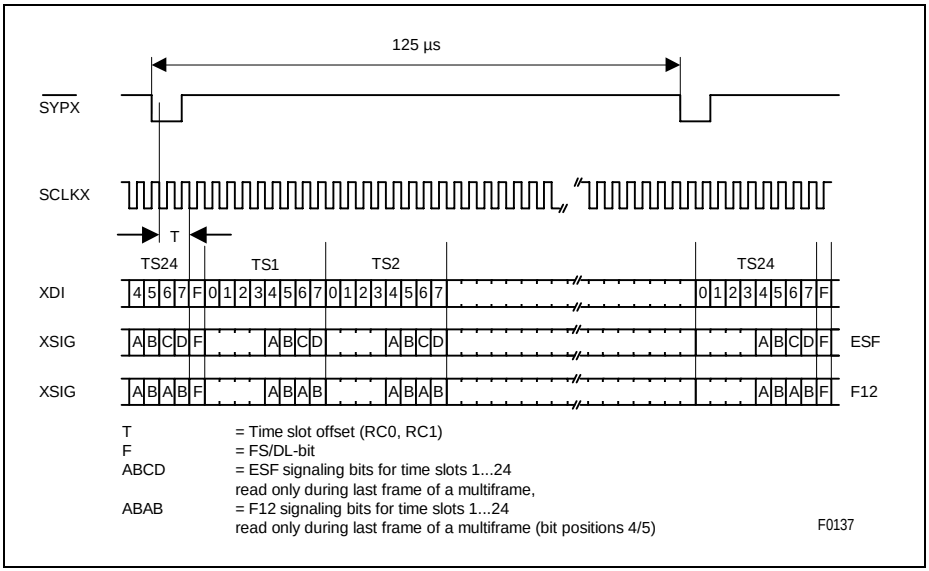


Figure 71 1.544 MHz Transmit Signaling Highway (T1/J1)

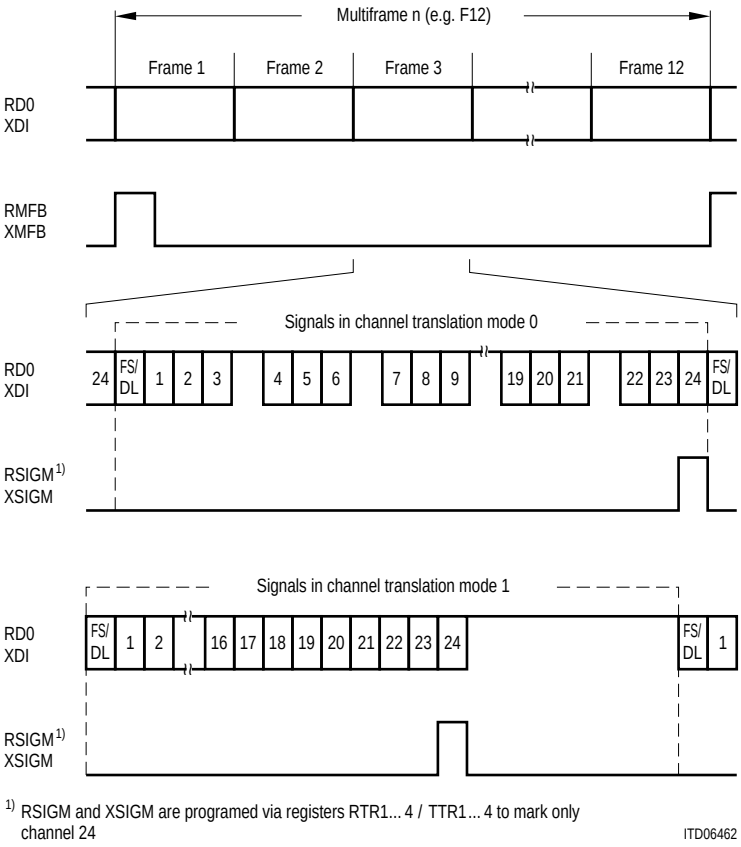


Figure 72 Signaling Marker for CAS/CAS-CC Applications (T1/J1)

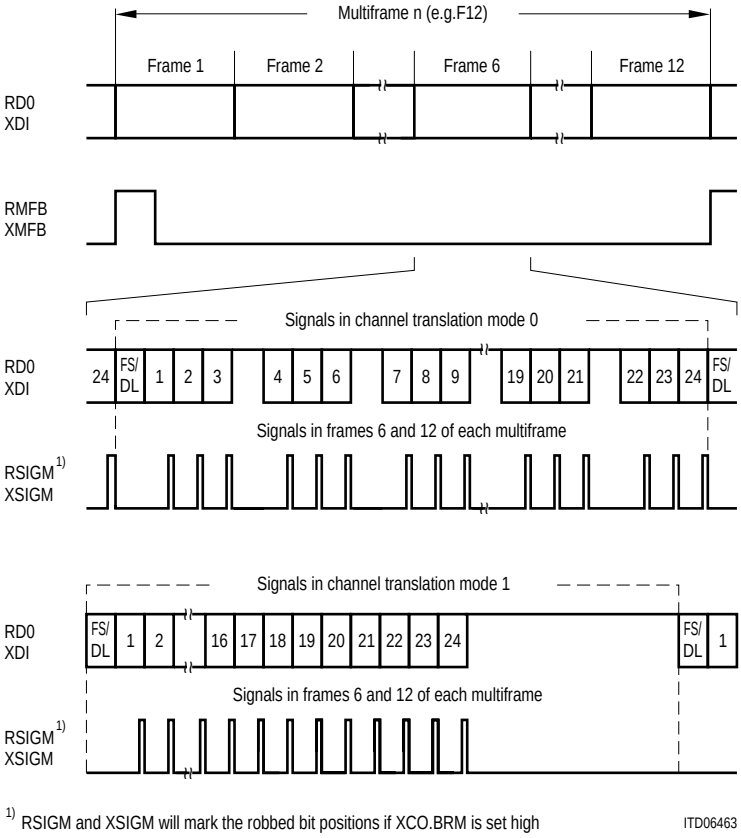


Figure 73 Signaling Marker for CAS-BR Applications (T1/J1)

FS/DL data on system transmit highway (XDI), time slot 0:

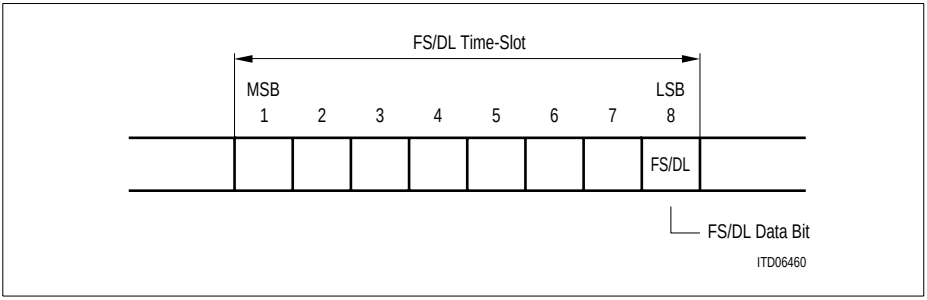


Figure 74 Transmit FS/DL Bits on XDI (T1/J1)

5.5.2.1 Transmit Offset Programming

The pulse length of $\overline{SYPR}$ and RFM is always the basic T1/J1 bit width (648 ns) in 1.544-MHz mode or the E1 bit width (488 ns) in 2.048-MHz mode.

This chapter describes the system highway operation in 1.544-MHz mode only. If the system highway is operated in 2.048-MHz mode, the description given in **Chapter 4.5.2.1** on **Page 116** applies.

$\overline{SYPX}$ Offset Calculation

T: time between beginning of $\overline{SYPX}$ pulse and beginning of next frame (time slot 0, bit 0, channel phase 0), measured in number of SCLKX clock intervals; maximum delay: $T_{max} = (200 \times SC/SD) - (7 \times SC/SD) - 1$

SD: basic data rate, 1.544 Mbit/s

SC: system clock rate; 1.544, 3.088, 6.176, or 12.352 MHz

X: programming value to be written to registers RC0 and RC1 (see **Page 344**).

$0 \leq T \leq 4$: $X = 4 - T + (7 \times SC/SD)$
$5 \leq T \leq T_{max}$: $X = (200 \times SC/SD) - T + 4$

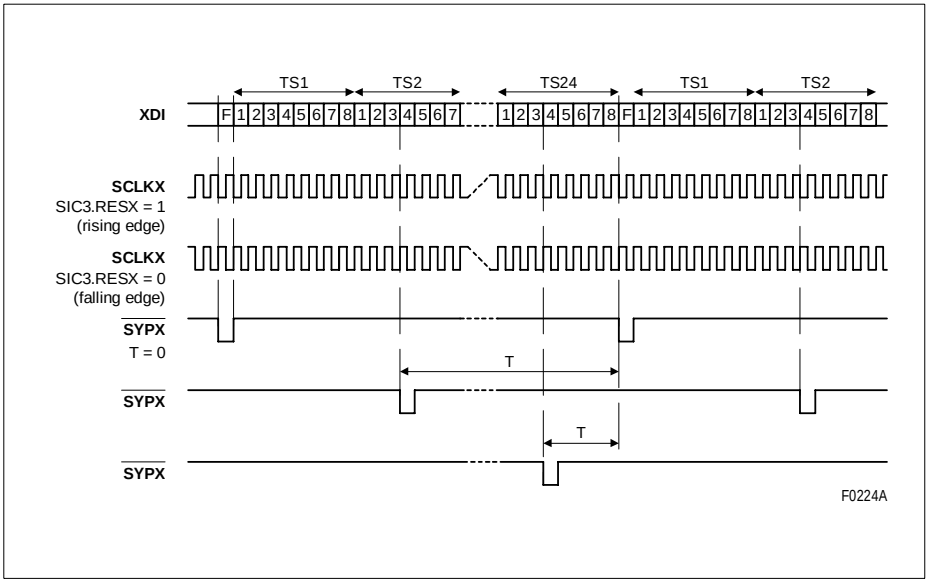


Figure 75 $\overline{\text{SYPX}}$ Offset Programming (1.544 Mbit/s, 1.544 MHz)

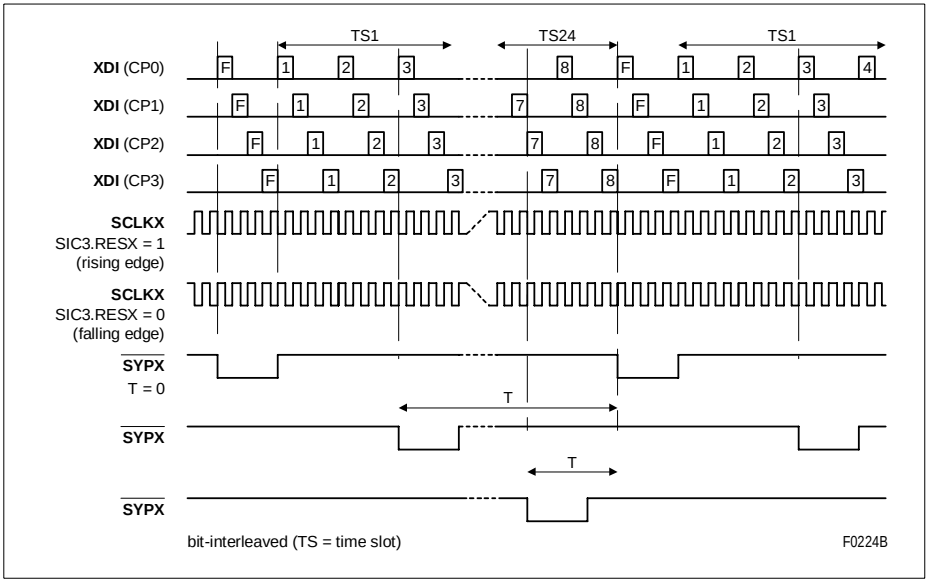


Figure 76 $\overline{\text{SYPX}}$ Offset Programming (6.176 Mbit/s, 6.176 MHz)

5.5.3 Time Slot Assigner (T1/J1)

HDLC channel 1 offers the flexibility to connect data during certain time slots, as defined by registers RTR(4:1) and TTR(4:1), to the RFIFO and XFIFO, respectively. Any combinations of time slots can be programmed for the receive and transmit directions. If CCR1.EITS = 1 the selected time slots (RTR(4:1)) are stored in the RFIFO of the signaling controller and the XFIFO contents is inserted into the transmit path as controlled by registers TTR(4:1).

Within selected time slots single bit positions can be masked to be used/not used for HDLC transmission for all HDLC channels. Additionally, the use of even, odd or both frames can be selected for each HDLC channel individually.

Table 45 Time Slot Assigner HDLC Channel 1 (T1/J1)

Receive Time Slot Register	Transmit Time Slot Register	Time Slots	Receive Time Slot Register	Transmit Time Slot Register	Time Slots
RTR 1.7	TTR 1.7	0	RTR 3.7	TTR 3.7	16
RTR 1.6	TTR 1.6	1	RTR 3.6	TTR 3.6	17
RTR 1.5	TTR 1.5	2	RTR 3.5	TTR 3.5	18
RTR 1.4	TTR 1.4	3	RTR 3.4	TTR 3.4	19
RTR 1.3	TTR 1.3	4	RTR 3.3	TTR 3.3	20
RTR 1.2	TTR 1.2	5	RTR 3.2	TTR 3.2	21
RTR 1.1	TTR 1.1	6	RTR 3.1	TTR 3.1	22
RTR 1.0	TTR 1.0	7	RTR 3.0	TTR 3.0	23
RTR 2.7	TTR 2.7	8	RTR 4.7	TTR 4.7	24
RTR 2.6	TTR 2.6	9	RTR 4.6	TTR 4.6	25
RTR 2.5	TTR 2.5	10	RTR 4.5	TTR 4.5	26
RTR 2.4	TTR 2.4	11	RTR 4.4	TTR 4.4	27
RTR 2.3	TTR 2.3	12	RTR 4.3	TTR 4.3	28
RTR 2.2	TTR 2.2	13	RTR 4.2	TTR 4.2	29
RTR 2.1	TTR 2.1	14	RTR 4.1	TTR 4.1	30
RTR 2.0	TTR 2.0	15	RTR 4.0	TTR 4.0	31

The format for receive FS/DL data transmission in time slot 0 of the system interface is as shown in **Figure 68** below. In order to get an undisturbed reception even in the asynchronous state bit FMR2.DAIS has to be set.

5.6 Test Functions (T1/J1)

5.6.1 Pseudo-Random Bit Sequence Generation and Monitor

The QuadFALC has the added ability to generate and monitor a 2^{15}-1 and 2^{20}-1 pseudo-random bit sequences (PRBS). The generated PRBS pattern is transmitted to the remote end on pins XL1/2 or XDOP/N and can be inverted optionally. Generating and monitoring of PRBS pattern is done according to ITU-T O.151 and TR62411 with maximum 14 consecutive zero restriction.

The PRBS monitor senses the PRBS pattern in the incoming data stream. Synchronization is done on the inverted and non-inverted PRBS pattern. The current synchronization status is reported in status and interrupt status registers. Enabled by bit LCR1.EPRM each PRBS bit error increments an error counter (BEC). Synchronization is reached within 400 ms with a probability of 99.9% and a bit error rate of up to 10^{-1}.

The PRBS generator and monitor can be used to handle either a framed (TPC0.FRA = 1) or an unframed (TPC0.FRA = 0) data stream.

5.6.2 Remote Loop

In the remote loopback mode the clock and data recovered from the line inputs RL1/2 or RDIP/RDIN are routed back to the line outputs XL1/2 or XDOP/XDON through the analog or digital transmitter. As in normal mode they are also processed by the synchronizer and then sent to the system interface.The remote loopback mode is selected by setting the corresponding control bits LIM1.RL+JATT. Received data is looped with or without use of the transmit jitter attenuator (FIFO).

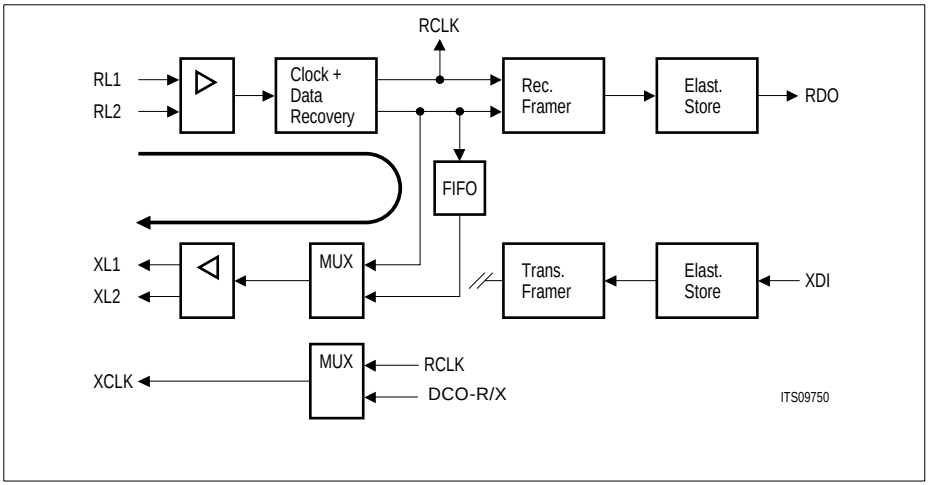


Figure 77 Remote Loop (T1/J1)

5.6.3 Payload Loop Back

To perform an effective circuit test a line loop is implemented.

If the payload loopback (FMR2.PLB) is activated the received 192 bits of payload data is looped back to the transmit direction. The framing bits, CRC6 and DL-bits are not looped, if FMR4.TM = 0. They are originated by the QuadFALC transmitter. If FMR4.TM = 1 the received FS/DL-bit is sent transparently back to the line interface. Following pins are ignored: XDI, XSIG, TCLK, SCLKX, $\overline{\text{SYPX}}$ and XMFS. All the received data is processed normally. With bit FMR2.SAIS an AIS can be sent to the system interface on pin RDO.

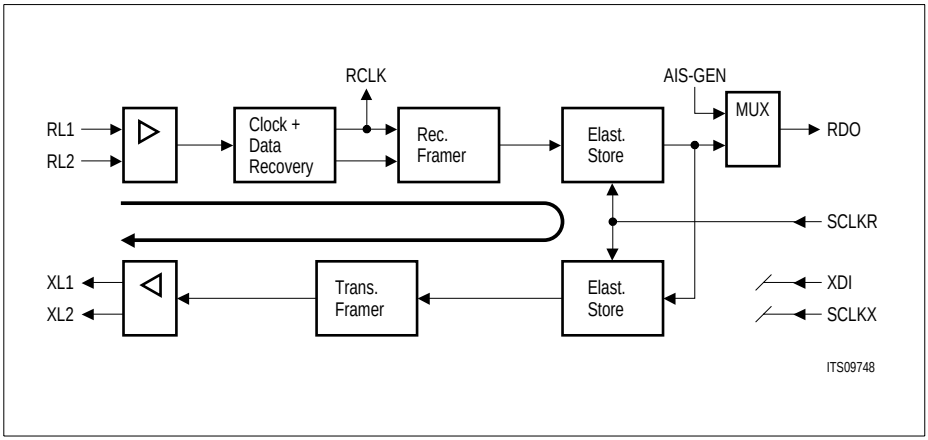


Figure 78 Payload Loop (T1/J1)

5.6.4 Local Loop

The local loopback mode, selected by LIM0.LL = 1, disconnects the receive lines RL1/2 or RDIP/RDIN from the receiver. Instead of the signals coming from the line the data provided by system interface are routed through the analog receiver back to the system interface. However, the bit stream is transmitted undisturbedly on the line. An AIS to the distant end can be enabled by setting FMR1.XAIS without influencing the data looped back to the system interface.

Note that enabling the local loop usually invokes an out of frame error until the receiver resynchronizes to the new framing. The serial codes for transmitter and receiver have to be identical.

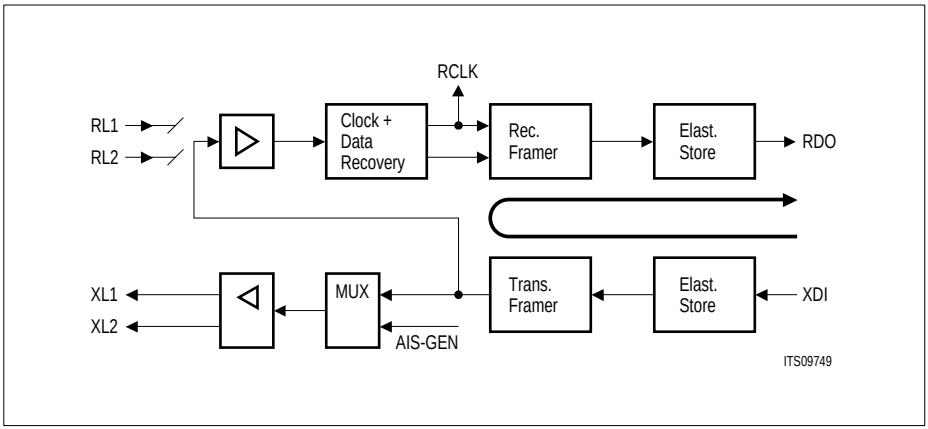


Figure 79 Local Loop (T1/J1)

5.6.5 Single Channel Loop Back (loopback of time slots)

The channel loopback is selected by LOOP.ECLB = 1.

Each of the 24 time slots can be selected for loopback from the system PCM input (XDI) to the system PCM output (RDO). This loopback is programmed for one time slot at a time selected by register LOOP. During loopback, an idle channel code programmed in register IDLE is transmitted to the remote end in the corresponding PCM route time slot.

For the time slot test, sending sequences of test patterns like a 1-kHz check signal should be avoided. Otherwise an increased occurrence of slips in the tested time slot disturbs testing. These slips do not influence the other time slots and the function of the receive memory. The usage of a quasi-static test pattern is recommended.

If CAS-BR is used, this must be switched off (FMR5.EIBR = 0) during channel loop back testing.

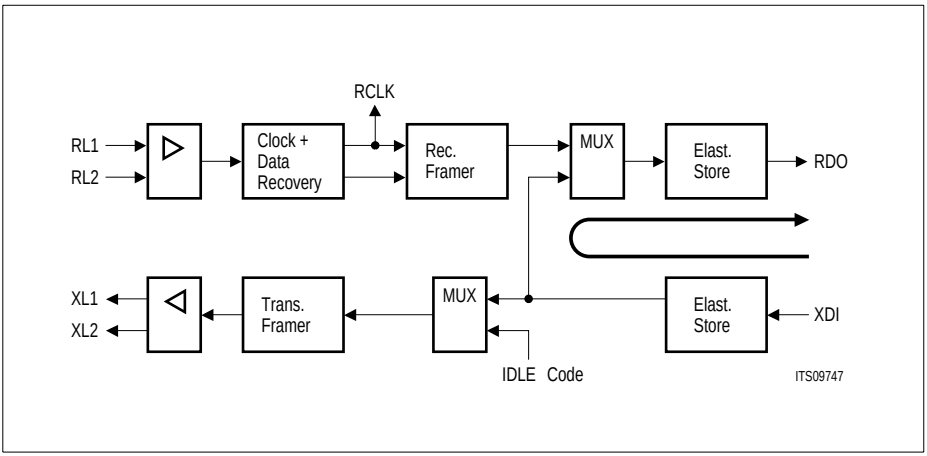


Figure 80 Channel Loopback (T1/J1)

5.6.6 Alarm Simulation (T1/J1)

Alarm simulation does not affect the normal operation of the device, i.e. all time slots remain available for transmission. However, possible *real* alarm conditions are *not* reported to the processor or to the remote end when the device is in the alarm simulation mode.

The alarm simulation is initiated by setting the bit FMR0.SIM. The following alarms are simulated:

- Loss of signal (LOS, red alarm)
- Alarm indication signal (AIS, blue alarm)
- Loss of pulse frame
- Remote alarm (yellow alarm) indication
- Receive and transmit slip indication
- Framing error counter
- Code violation counter
- CRC6 error counter

Some of the above indications are only simulated if the QuadFALC is configured in a mode where the alarm is applicable.

The alarm simulation is controlled by the value of the alarm simulation counter: FRS2.ESC which is incremented by setting bit FMR0.SIM.

Clearing of alarm indications:

- Automatically for LOS, remote (yellow) alarm, AIS, and loss of synchronization and
- User controlled for slips by reading the corresponding interrupt status register ISR3.
- Error counter have to be cleared by reading the corresponding counter registers.

is only possible at defined counter steps of FRS2.ESC. For complete simulation (FRS2.ESC = 0), eight simulation steps are necessary.

5.6.7 Single Bit Defect Insertion

Single bit defects can be inserted into the transmit data stream for the following functions:

FAS defect, multiframe defect, CRC defect, CAS defect, PRBS defect and bipolar violation.

Defect insertion is controlled by register IERR.

5.7 J1-Feature Overview

The Japanese J1 standard is very similar to the T1 standard, but differs in some details. To support these differences easily, the following features are provided within the QuadFALC:

- CRC6 generation and checking according to ITU-JT G.706
  (CRC checksum calculation includes FS/DL-bits, see **Chapter 5.2.6.3** on **page 151**)
- Remote alarm handling according to ITU-JT G.704
  (remote alarm pattern in DL-channel is '1111111111111111', see **Chapter 5.2.6.2** on **page 151**)
- NTT synchronization requirements in ESF framing mode
- Pulse shaping according to JT G.704
- Receive input thresholds according to ITU-JT G.703

J1 mode is globally selected by setting RC0.SJR = 1 (see **page 345**). For specific J1 framer initialization see **Table 56** on **page 203**.

No special pulse mask setting is required, the described T1-settings also fulfill the J1 requirements.

6 Operational Description E1

6.1 Operational Overview E1

The QuadFALC can be operated in two modes, which are either E1 mode or T1/J1 mode.

Each of the four channels can be configured to E1 or T1/J1 mode independently.

The device is programmable via a microprocessor interface which enables byte or word access to all control and status registers.

After reset the QuadFALC must be initialized first. General guidelines for initialization are described in **Chapter 6.3**.

The status registers are read-only and are updated continuously. Normally, the processor reads the status registers periodically to analyze the alarm status and signaling data.

Signals (for example RL1/2 receive line) should not be applied before the device is powered up.

6.2 Device Reset E1

The QuadFALC is forced to the reset state if a low signal is input on pin $\overline{\text{RES}}$ for a minimum period of 10 µs. During reset the QuadFALC needs an active clock on pin MCLK. All output stages are in a high impedance state, all internal flip-flops are reset and most of the control registers are initialized with default values.

After reset the device is initialized to E1 operation.

6.3 Device Initialization in E1 Mode

After reset, the QuadFALC is initialized for doubleframe format with register values listed in the following table.

Table 46 Initial Values after Reset (E1)

Register	Reset Value	Meaning
FMR0	00_H	NRZ Coding, no alarm simulation.
FMR1 FMR2	00_H	E1-doubleframe format, 2 Mbit/s system data rate, no AIS transmission to remote end or system interface, payload loop off.
SIC1 SIC2, SIC3	00_H 00_H 00_H	8.192 MHz system clocking rate, receive buffer 2 frames, transmit buffer bypass, data sampled or transmitted on the falling edge of SCLKR/X, automatic freeze signaling, data is active in the first channel phase

Table 46 Initial Values after Reset (E1) (cont'd)

Register	Reset Value	Meaning
LOOP XSW XSP TSWM	00_H 00_H 00_H 00_H	Channel loop back and single frame mode are disabled. All bits of the transmitted service word are cleared. Spare bit values are cleared. No transparent mode active.
XC0 XC1	00_H $9C_H$	The transmit clock offset is cleared. The transmit time slot offset is cleared.
RC0 RC1	00_H $9C_H$	The receive clock slot offset is cleared. The receive time slot offset is cleared.
IDLE ICB (4:1)	00_H 00_H	Idle channel code is cleared. Normal operation (no "Idle Channel" selected).
LIM0 LIM1 PCD PCR	00_H 00_H 00_H 00_H	Slave Mode, local loop off Analog interface selected, remote loop off Pulse count for LOS detection cleared Pulse count for LOS recovery cleared
XPM(2:0)	40_H, 03_H, $7B_H$	Transmit pulse mask (transmitter in tristate mode)
IMR(4:1)	FF_H	All interrupts are disabled
RTR(4:1) TTR(4:1)	all 00_H all 00_H	No time slots selected
GCR	00_H	Internal second timer, power on
CMR1	00_H	RCLK output: DPLL clock, DCO-X enabled, DCO-X internal reference clock
CMR2	00_H	SCLKR selected, SCLKX selected, receive synchronization pulse sourced by $\overline{\text{SYPR}}$, transmit synchronization pulse sourced by $\overline{\text{SYPX}}$
PC(4:1)	00_H, 00_H 00_H, 00_H	Input function of ports RP(A to D): $\overline{\text{SYPR}}$, Input function of ports XP(A to D): $\overline{\text{SYPX}}$
PC5	00_H	SCLKR, SCLKX, RCLK configured to inputs, XMFS active low
MODE	00_H	Signaling controller disabled
RAH1/2 RAL1/2	FD_H, FF_H FF_H, FF_H	Compare register for receive address cleared
GCM(8:1)	all 00_H	Fixed clock mode selected (2.048 MHz on pin MCLK required, all channels E1).

E1 Initialization

For a correct start up of the primary access interface a set of parameters specific to the system and hardware environment must be programmed after reset goes inactive. Both the basic and the operational parameters must be programmed **before** the activation procedure of the PCM line starts. Such procedures are specified in ITU-T and ETSI recommendations (e.g. fault conditions and consequent actions). Setting optional parameters primarily makes sense when basic operation via the PCM line is guaranteed. **Table 47** gives an overview of the most important parameters in terms of signals and control bits which are to be programmed in one of the above steps. The sequence is recommended but not mandatory. Accordingly, parameters for the basic and operational set up, for example, can be programmed simultaneously. The bit FMR1.PMOD should always be kept low (otherwise T1/J1 mode is selected).

Table 47 Initialization Parameters (E1)

Basic Set Up	
Master clocking mode	GCM(8:1) according to external MCLK clock frequency
E1 mode select	FMR1.PMOD = 0
Specification of line interface and clock generation	LIM0, LIM1, XPM(2:0)
Line interface coding	FMR0.XC1/0, FMR0.RC1/0
Loss of signal detection/recovery conditions	PCD, PCR, LIM1, LIM2
System clocking and data rate	SIC1.SSC1/0, SIC1.SSD1,FMR1.SSD0 CMR2.IRSP/IRSC/IXSP/IXSC
Transmit offset counters	XC0.XCO, XC1.XTO
Receive offset counters	RC0.RCO, RC1.RTO
AIS to system interface	FMR2.DAIS/SAIS
Operational Set Up	
Select framing	FMR2.RFS1/0, FMR1.XFS
Framing additions	RC1.ASY4, RC1.SWD
Synchronization mode	FMR1.AFR, FMR2.ALMF
Signaling mode	XSP, XSW, FMR1.ENSA, XSA(8:4), TSWM, MODE, CCR1, CCR2, RAH1/2, RAL1/2

Features like channel loop back, idle channel activation, extensions for signaling support, alarm simulation, etc. are activated later. Transmission of alarms (e.g. AIS, remote alarm) and control of synchronization in connection with consequent actions to remote end and internal system depend on the activation procedure selected.

Note: Read access to unused register addresses: value should be ignored.
Write access to unused register addresses: should be avoided, or set to "00" hex in address range. up to xA9; must be avoided in address range above xA9 if not defined elsewhere (for example in ***Table 49*** *on* ***Page 195****).*
All control registers (except XFIFO, XS(16:1), CMDR, DEC) are of type Read/ Write.

Specific E1 Register Settings

The following is a suggestion for a basic initialization to meet most of the E1 requirements. Depending on different applications and requirement any other initialization can be used.

Table 48 Line Interface Initialization (E1)

FMR0.XC0/ FMR0.RC0/ LIM1.DRS FMR3.CMI	The QuadFALC supports requirements for the analog line interface as well as the digital line interface. For the analog line interface the codes AMI and HDB3 are supported. For the digital line interface modes (dual or single rail) the QuadFALC supports AMI, HDB3, CMI (with and without HDB3 precoding) and NRZ.
PCD = 0x0A	LOS detection after 176 consecutive "zeros" (fulfills G.775).
PCR = 0x15	LOS recovery after 22 "ones" in the PCD interval. (fulfills G.775).
LIM1.RIL(2:0) = 010_B	LOS threshold of 0.5 V (fulfills G.775).

To achieve optimum receiver sensitivity in long haul mode (> 38 dB) the following sequence must be run:

Table 49 Receive Line Interface Initialization (E1)

Address	Data
BB_H	17_H
BC_H	55_H
BB_H	97_H
BB_H	11_H
BC_H	AA_H
BB_H	91_H

Table 49 Receive Line Interface Initialization (E1) (cont'd)

Address	Data
BB_H	12_H
BC_H	55_H
BB_H	92_H
BB_H	$0C_H$
BC_H	00_H
BB_H	$8C_H$

Note: sequence must be repeated whenever receiver reset (CMDR.RRES) of arbitrary channel was performed (e.g. after setting bit LIM1.EQON).

E1 Framer Initialization

The selection of the following modes during the basic initialization supports the ETSI requirements for E-Bit Access, remote alarm and synchronization (please refer also to QuadFALC driver code of the evaluation system EASY22554 and application notes) and helps to reduce the software load. They are very helpful especially to meet requirements as specified in ETS300 011.

Table 50 Framer Initialization (E1)

XSP.AXS = 1	ETS300 011 C4.x for instance requires the sending of E-Bits in TS0 if CRC4 errors have been detected. By programming XSP.AXS = 1 the submultiframe status is inserted automatically in the next outgoing multiframe.
XSP.EBP = 1	If the QuadFALC has reached asynchronous state the E-Bit is cleared if XSP.EBP = 0 and set if XSP.EBP = 1. ETS300 011 requires that the E-Bit is set in asynchronous state.
FMR2.AXRA = 1	The transmission of RAI via the line interface is done automatically by the QuadFALC in case of loss of frame alignment (FRS0.LFA = 1). If basic framing has been reinstalled RAI is automatically reset.
FMR2.FRS1/2 = 10 FMR1.AFR = 1	In this mode a search of double framing is automatically restarted, if no CRC4 multiframing is found within 8ms. Together with FMR2.AXRA = 1 this mode is essential to meet ETS300 011 and reduces the processor load heavily.

Table 50 Framer Initialization (E1) (cont'd)

FMR2.ALMF = 1	The receiver initiates a new basic- and multiframing research if more than 914 CRC4 errors have been detected in one second.
FMR2.FRS1/0 = 11	In the interworking mode the QuadFALC stays in double framing format if no multiframe pattern is found in a time interval of 400 ms. This is also indicated by a 400 ms interrupt. Additionally the extended interworking mode (FMR3.EXTIW = 1) will activate after 400 ms the remote alarm (FMR2.AXRA = 1) and will still search the multiframing without switching completely to the double framing. A complete resynchronization in an 8 ms interval is not initiated.

Table 51 HDLC Controller Initialization (E1)

MODE = 0x88	HDLC receiver active, no address comparison.
CCR1 = 0x18	Enable signaling via TS(31:0), interframe time fill with continuous flags.
IMR0.RME = 0 IMR0.RPF = 0 IMR1.XPR = 0	Unmask interrupts for HDLC processor requests.
RTR3.TS16 = 1 TTR3.TS16 = 1 TSEO = 0x00 TSBS1 = 0xFF	Select TS16 for HDLC data reception and transmission. Even and odd frames are used for HDLC reception and transmission. Select all bits of selected time slot.

Table 52 CAS-CC Initialization (E1)

XSP.CASEN = 1 CCR1.EITS = 0	Send CAS info stored in the XS(16:1) registers.
IMR0.CASC = 0	Enable interrupt with any data change in the RS(16:1) registers.

Attention: After the device initialization a software reset should be executed by setting of bits CMDR.XRES/RRES.

7 Operational Description T1/J1

7.1 Operational Overview T1/J1

The QuadFALC can be operated in two principle modes, which are either E1 mode or T1/J1 mode.

Each of the four channels can be configured to E1 or T1/J1 mode independently.

The device is programmable via a microprocessor interface which enables byte or word access to all control and status registers.

After reset the QuadFALC must be initialized first. General guidelines for initialization are described in **Chapter 7.3**

The status registers are read-only and are updated continuously. Normally, the processor reads the status registers periodically to analyze the alarm status and signaling data.

Signals (for example RL1/2 receive line) should not be applied before the device is powered up.

7.2 Device Reset T1/J1

The QuadFALC is forced to the reset state if a low signal is input on pin $\overline{\text{RES}}$ for a minimum period of 10 µs. During reset the QuadFALC needs an active clock on pin MCLK. All output stages are in a high impedance state, all internal flip-flops are reset and most of the control registers are initialized with default values.

After reset the device is initialized to E1 operation.

7.3 Device Initialization in T1/J1 Mode

After reset, the QuadFALC is initialized for E1 doubleframe format. To initialize T1/J1 mode, bit FMR1.PMOD has to be set high. After the internal clocking is settled to T1/J1mode (takes up to 20 µs), the following register values are initialized:

Table 53 Initial Values after reset and FMR1.PMOD = 1 (T1/J1)

Register	Initiated Value	Meaning
FMR0	00_H	NRZ coding, no alarm simulation
FMR1 FMR2	00_H 00_H	PCM24 mode, 2.048 Mbit/s system data rate, no AIS transmission to remote end or system interface, payload loop off, channel translation mode 0

Table 53 Initial Values after reset and FMR1.PMOD = 1 (T1/J1) (cont'd)

Register	Initiated Value	Meaning
SIC1 SIC2, SIC3	00_H 00_H 00_H	2.048 MHz system clocking rate, receive buffer 2 frames, transmit buffer bypass, data sampled or transmitted on the falling edge of SCLKR/X, automatic freeze signaling, data is active in the first channel phase
LOOP	00_H	loop backs are disabled.
FMR4 FMR5	00_H 00_H	Remote alarm indication towards remote end is disabled. LFA condition: 2 out of 4/5/6 framing bits, non-auto-synchronization mode, F12 multiframing, internal bit robbing access disabled
XC0 XC1	00_H $9C_H$	The transmit clock slot offset is cleared. The transmit time slot offset is cleared.
RC0 RC1	00_H $9C_H$	The receive clock slot offset is cleared. The receive time slot offset is cleared.
IDLE ICB (3:1)	00_H 00_H	Idle channel code is cleared. Normal operation (no "Idle Channels" selected).
CCB (3:1)	00_H	Normal operation (no clear channel operation).
LIM0 LIM1 PCD PCR	00_H 00_H 00_H 00_H	Slave mode, local loop off, analog interface selected, remote loop off pulse count for LOS detection cleared pulse count for LOS recovery cleared
XPM(2:0)	40_H,03_H,$7B_H$	Transmit pulse mask (transmitter in tristate mode)
IMR(4:0)	FF_H	All interrupts are disabled
GCR	00_H	Internal second timer, power on
CMR1	00_H	RCLK output: DPLL clock, DCO-X enabled, DCO-X internal reference clock
CMR2	00_H	SCLKR selected, SCLKX selected, receive synchronization pulse sourced by $\overline{SYPR}$, transmit synchronization pulse sourced by $\overline{SYPX}$
GPC1	00_H	SEC port input active high
PC(4:1)	00_H, 00_H 00_H, 00_H	Input function of ports RP(A to D): $\overline{SYPR}$, Input function of ports XP(A to D): $\overline{SYPX}$
PC5	00_H	SCLKR, SCLKX, RCLK configured to inputs, XMFS active low

Table 53 Initial Values after reset and FMR1.PMOD = 1 (T1/J1) (cont'd)

Register	Initiated Value	Meaning
MODE	00_H	Signaling controller disabled
RAH1/2 RAL1/2	FD_H, FF_H FF_H, FF_H	Compare register for receive address cleared
GCM(8:1)	all 00_H	Fixed clock mode selected (1.544 MHz on pin MCLK required, all channels T1/J1).
RTR(4:1) TTR(4:1)	all 00_H all 00_H	No time slots selected

T1/J1 Initialization

For a correct start up of the primary access interface a set of parameters specific to the system and hardware environment must be programmed after $\overline{RES}$ goes inactive (high). Both the basic and the operational parameters must be programmed **before** the activation procedure of the PCM line starts. Such procedures are specified in ITU-T recommendations (e.g. fault conditions and consequent actions). Setting optional parameters primarily makes sense when basic operation via the PCM line is guaranteed. **Table 54** gives an overview of the most important parameters in terms of signals and control bits which are to be programmed in one of the above steps. The sequence is recommended but not mandatory. Accordingly, parameters for the basic and operational set up, for example, can be programmed simultaneously. The bit FMR1.PMOD must always be kept high (otherwise E1 mode is selected). J1 mode is selected by additionally setting RC0.SJR = 1.

Features like channel loop back, idle channel activation, clear channel activation, extensions for signaling support, alarm simulation, etc. are activated later. Transmission of alarms (e.g. AIS, remote alarm) and control of synchronization in connection with consequent actions to remote end and internal system depend on the activation procedure selected.

Table 54 Initialization Parameters (T1/J1)

Basic Set Up	**T1**	**J1**
Master clocking mode	GCM(8:1) according to external MCLK clock frequency	
T1/J1 mode select	FMR1.PMOD = 1, RC0.SJR = 0	FMR1.PMOD = 1, RC0.SJR = 1
Specification of line interface and clock generation	LIM0, LIM1, XPM(2:0)	
Line interface coding	FMR0.XC(1:0), FMR0.RC(1:0)	
Loss of signal detection/ recovery conditions	PCD, PCR, LIM1, LIM2	
System clocking and data rate	SIC1.SSC(1:0), SIC1.SSD1, FMR1.SSD0, CMR1.IRSP/ IRSC/IXSP/IXSC	
Channel translation mode	FMR1.CTM	
Transmit offset counters	XC0.XCO, XC1.XTO	
Receive offset counters	RC0.RCO, RC1.RTO	
AIS to system interface	FMR2.DAIS/SAIS	
Operational Set Up		
Select framing	FMR4.FM1/0	
Framing additions	FMR1.CRC, FMR0.SRAF	
Synchronization mode	FMR4.AUTO, FMR4.SSC1/0, FMR2.MCSP, FMR2.SSP	
Signaling mode	FMR5.EIBR, XC0.BRM, MODE, CCR1, CCR2, RAH1/2, RAL1/2	

Note: Read access to unused register addresses: value should be ignored.
*Write access to unused register addresses: should be avoided, or set to “00” hex in address range. up to xA9; must be avoided in address range above xA9 if not defined elsewhere (for example in **Table 49** on **Page 195**).*
All control registers (except XFIFO, XS(12:1), CMDR, DEC) are of type read/write

Specific T1/J1 Initialization

The following is a suggestion for a basic initialization to meet most of the T1/J1 requirements. Depending on different applications and requirements any other initialization can be used.

Table 55 Line Interface Initialization (T1/J1)

Register	Function
FMR0.XC0/1 FMR0.RC0/1 LIM1.DRS CCB(3:1) SIC3.CMI	The QuadFALC supports requirements for the analog line interface as well as the digital line interface. For the analog line interface the codes AMI (with and without bit 7stuffing) and B8ZS are supported. For the digital line interface modes (dual or single rail) the QuadFALC supports AMI (with and without bit 7 stuffing), B8ZS (with and without B8ZS precoding) and NRZ.
PCD = 0x0A	LOS detection after 176 consecutive “zeros” (fulfills G.775/ Telcordia (Bellcore)/AT&T)
PCR = 0x15	LOS recovery after 22 “ones” in the PCD interval (fulfills G.775, Bellcore/AT&T).
LIM1.RIL(2:0) = 010_B	LOS threshold of 0.5 V (fulfills G.775).
GCR.SCI = 1	Additional Recovery Interrupts. Help to meet alarm activation and deactivation conditions in time.
LIM2.LOS1 = 1	Automatic pulse density check on 15 consecutive zeros for LOS recovery condition (Bellcore requirement)

Table 56 Framer Initialization (T1/J1)

Register	Function	
	T1	J1
FMR4.SSC1/0	Selection of framing sync conditions	
FMR4.FM1/0	Select framing format	
FMR2.AXRA = 1	The transmission of RAI via the line interface is done automatically by the QuadFALC in case of Loss of Frame Alignment (FRS0.LFA = 1). If framing has been reinstalled RAI is automatically reset	
FMR4.AUTO = 1	Automatic synchronization in case of definite framing candidate (FRS0.FSRF). In case of multiple framing candidates and CRC6 errors different resynchronization conditions can be programmed via FMR2.MCSP/SSP.	
RCO.SJR[1] = 1 FMR0.SRAF = 0 XSW.XRA = 1		Remote alarm handling via DL-channel according to ITU-T JG.704 using pattern "1111111111111111"
RCO.SJR = 0	CRC6 calculation without FS/ DL-bits	
RCO.SJR = 1		CRC6 calculation including FS/ DL-bits
FMR4.AUTO = 1	Automatic synchronization in case of definite framing candidate (FRS0.FSRF). In case of multiple framing candidates and CRC6 errors different resynchronization conditions can be programmed via FMR2.MCSP/SSP.	
FMR4.SSC1 = 1 FMR4.SSC0 = 1 FMR2.MCSP = 0 FMR2.SSP = 1		Synchronization and resynchronization conditions, for details see register description

[1] Remote alarm handling and CRC6 calculation are commonly selected by RC0.SJR

Table 57 HDLC Controller Initialization (T1/J1)

MODE = 0x88	HDLC receiver active, no address comparison.
CCR1 = 0x18	Enable signaling via TS(24:1), interframe time fill with continuous flags.
IMR0.RME = 0 IMR0.RPF = 0 IMR1.XPR = 0	Unmask interrupts for HDLC processor requests.
RTR4.0 = 1 TTR4.0 = 1 TSEO = 0x00 TSBS1 = 0xFF	Select time slot 24 for HDLC data reception and transmission. Even and odd frames are used for HDLC reception and transmission. Select all bits of selected time slot.

Table 58 Initialization of the CAS-BR Controller (T1/J1)

FMR5.EIBR = 1	Enable CAS-BR Mode Send CAS-BR information stored in XS(12:1)
IMR1.CASE = 0 IMR0.RSC = 0	Enable interrupts which indicate the access to the XS(12:1) CAS-BR registers and any data change in RS(12:1)

Note: After the device initialization a software reset should be executed by setting of bits CMDR.XRES/RRES.

8 Signaling Controller Operating Modes

The HDLC controller can be programmed to operate in various modes, which are different in the treatment of the HDLC frame in receive direction. Thus, the receive data flow and the address recognition features can be performed in a very flexible way, to satisfy almost any practical requirements.

There are 4 different operating modes which can be set via the mode register (MODE).

8.1 HDLC Mode

All frames with valid addresses are forwarded directly via the RFIFO to the system memory.

Depending on the selected address mode, the QuadFALC can perform a 1- or 2-byte address recognition (MODE.MDS0).

If a 2-byte address field is selected, the high address byte is compared to the fixed value FEH or FCH (group address) as well as with two individually programmable values in RAH1 and RAH2 registers. According to the ISDN LAPD protocol, bit 1 of the high byte address is interpreted as command/response bit (C/R) and is excluded from the address comparison.

Similarly, two compare values can be programmed in special registers (RAL1, RAL2) for the low address byte. A valid address is recognized in case the high and low byte of the address field correspond to one of the compare values. Thus, the QuadFALC can be called (addressed) with 6 different address combinations. HDLC frames with address fields that do not match any of the address combinations, are ignored by the QuadFALC.

In case of a 1-byte address, RAL1 and RAL2 are used as compare registers. The HDLC control field, data in the I-field and an additional status byte are temporarily stored in the RFIFO. Additional information can also be read from a special register (RSIS).

As defined by the HDLC protocol, the QuadFALC performs the zero bit insertion/deletion (bit stuffing) in the transmit/receive data stream automatically. That means, it is guaranteed that at least one “0” will appear after 5 consecutive “1”s.

8.1.1 Non-Auto Mode

(MODE.MDS(2:1) = 01)

Characteristics: address recognition, flag- and CRC generation/check, bit stuffing

All frames with valid addresses are forwarded directly via the RFIFO to the system memory.

8.1.2 Transparent Mode 1

(MODE.MDS(2:0) = 101)

Characteristics: address recognition, flag- and CRC generation/check, bit stuffing

Only the high byte of a 2-byte address field is compared to registers RAH1/2. The whole frame excluding the first address byte is stored in RFIFO.

8.1.3 Transparent Mode 0

(MODE.MDS(2:0) = 100)

Characteristics: flag- and CRC generation/check, bit stuffing
No address recognition is performed and each frame is stored in the RFIFO.

8.1.4 SS7 Support

SS7 protocol is supported by means of several hardware features as described in **Chapter 4.1.14.2** on page **79** and **Chapter 5.1.14.2** on page **140**.

8.1.5 Receive Data Flow

The following figure gives an overview of the management of the received HDLC frames in the different operating modes.

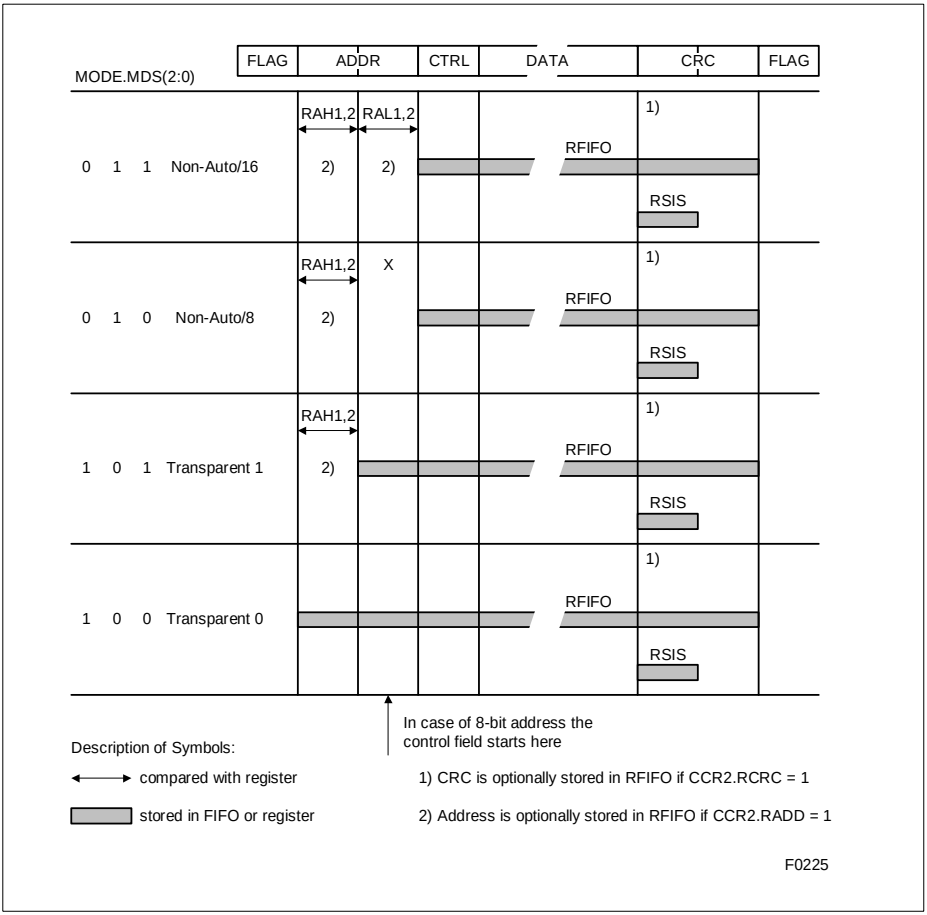


Figure 81 HDLC Receive Data Flow

8.1.6 Transmit Data Flow

The frames can be transmitted as shown below.

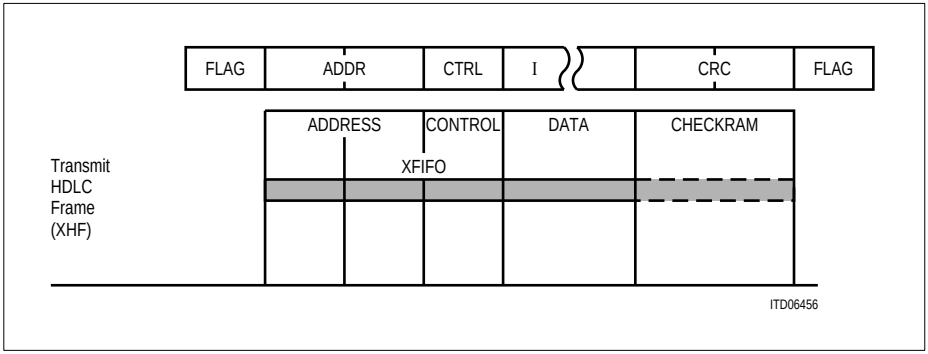


Figure 82 HDLC Transmit Data Flow

Transmitting a HDLC frame via register CMDR.XTF, the address, the control fields and the data field have to be entered in the XFIFO.

If CCR2.XCRC is set, the CRC checksum will not be generated internally. The checksum has to be provided via the transmit FIFO (XFIFO) as the last two bytes. The transmitted frame is closed automatically with a closing flag only.

The QuadFALC does not check whether the length of the frame, i.e. the number of bytes to be transmitted makes sense or not.

8.2 Extended Transparent Mode

Characteristics: fully transparent

In no HDLC mode, fully transparent data transmission/reception without HDLC framing is performed, i.e. without flag generation/recognition, CRC generation/check, or bit stuffing. This feature can be profitably used e.g. for:

- Specific protocol variations
- Transmission of a BOM frame
- Test purposes

Data transmission is always performed out of the XFIFO. In transparent mode, the receive data is shifted into the RFIFO.

Note: If a 1-byte frame is sent in extended transparent mode, in addition to interrupt ISR1.XPR (transmit pool ready) the interrupt ISR1.XDU (transmit buffer underrun) is set and XFIFO is blocked.

8.3 Signaling Controller Functions

8.3.1 Transparent Transmission and Reception

When programmed in the extended transparent mode via the MODE register (MODE.MDS(2:0) = 111), the QuadFALC performs fully transparent data transmission and reception without HDLC framing, i.e. without

- flag insertion and deletion
- CRC generation and checking
- Bit stuffing

In order to enable fully transparent data transfer, bit MODE.HRAC has to be set.

Received data is always shifted into RFIFO.

Data transmission is always performed out of XFIFO by shifting the contents of XFIFO into the outgoing data stream directly. Transmission is initiated by setting CMDR.XTF (04_H). A synchronization byte FF_H is sent automatically before the first byte of the XFIFO is transmitted.

Cyclic Transmission (fully transparent)

If the extended transparent mode is selected, the QuadFALC supports the continuous transmission of the contents of the transmit FIFO.

After having written 1 to 32 bytes to XFIFO, the command XREP&XTF (CMDR = 00100100 = 24_H) forces the QuadFALC to transmit the data stored in XFIFO to the remote end repeatedly.

Note: The cyclic transmission continues until a reset command (CMDR.SRES) is issued or with resetting of CMDR.XREP, after which continuous “1”s are transmitted. During cyclic transmission the XREP-bit has to be set with every write operation to CMDR.

8.3.2 CRC on/off Features

As an option in HDLC mode the internal handling of the received and transmitted CRC checksum can be influenced via control bits CCR2.RCRC and CCR2.XCRC.

- Receive Direction

The received CRC checksum is always assumed to be in the 2 last bytes of a frame (CRC-ITU), immediately preceding a closing flag. If CCR2.RCRC is set, the received CRC checksum is written to RFIFO where it precedes the frame status byte (contents of register RSIS). The received CRC checksum is additionally checked for correctness. If HDLC mode is selected, the limits for “Valid Frame” check are modified (refer to description of bit RSIS.VFR).

- Transmit Direction

If CCR2.XCRC is set, the CRC checksum is not generated internally. The checksum has to be provided via the transmit FIFO (XFIFO) as the last two bytes. The transmitted frame is closed automatically by a closing flag only.
The QuadFALC does not check whether the length of the frame, i.e. the number of bytes to be transmitted is valid or not.

8.3.3 Receive Address Pushed to RFIFO

The address field of received frames can be pushed to the receive FIFO (first one or two bytes of a frame). This function is used together with extended address recognition. It is enabled by setting control bit CCR2.RADD.

8.3.4 HDLC Data Transmission

In transmit direction 2×32 byte FIFO buffers are provided. After checking the XFIFO status by polling bit SIS.XFW or after an interrupt ISR1.XPR (Transmit Pool Ready), up to 32 bytes can be entered by the CPU to the XFIFO.

The transmission of a frame can be started by issuing a XTF or XHF command via the command register. If the transmit command does not include an end of message indication (CMDR.XME), the QuadFALC will repeatedly request for the next data block by means of an XPR interrupt as soon as no more than 32 bytes are stored in the XFIFO, i.e. a 32-byte pool is accessible to the CPU.

This process is repeated until the CPU indicates the end of message by XME command, after which frame transmission is finished correctly by appending the CRC and closing flag sequence. Consecutive frames can share a flag, or can be transmitted as back-to-back frames, if service of the XFIFO is fast enough.

In case no more data is available in the XFIFO prior to the arrival of XME, the transmission of the frame is terminated with an abort sequence and the CPU is notified by interrupt ISR1.XDU. The frame can be aborted by software using CMDR.SRES.

The data transmission sequence, from the CPU's point of view, is outlined in **Figure 83**.

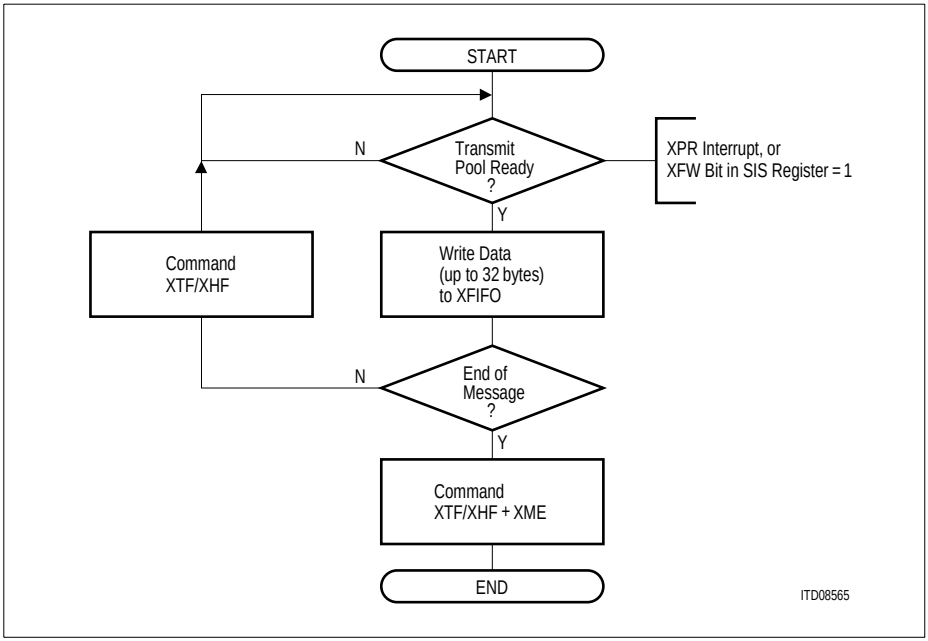


Figure 83 Interrupt Driven Data Transmission (flow diagram)

The activities at both serial and CPU interface during frame transmission (supposed frame length = 70 bytes) shown in **Figure 84**.

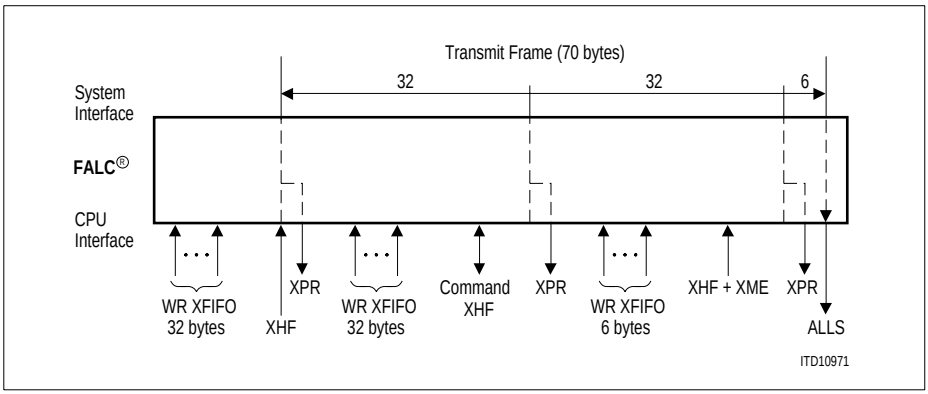


Figure 84 Interrupt Driven Transmission Example

8.3.5 HDLC Data Reception

2×32 byte FIFO buffers are also provided in receive direction. There are different interrupt indications concerned with the reception of data:

- RPF (receive pool full) interrupt, indicating that a 32-byte block of data can be read from RFIFO and the received message is not yet complete.
- RME (receive message end) interrupt, indicating that the reception of one message is completed.

The following figure gives an example of a reception sequence, assuming that a “long” frame (66 bytes) followed by two short frames (6 bytes each) are received.

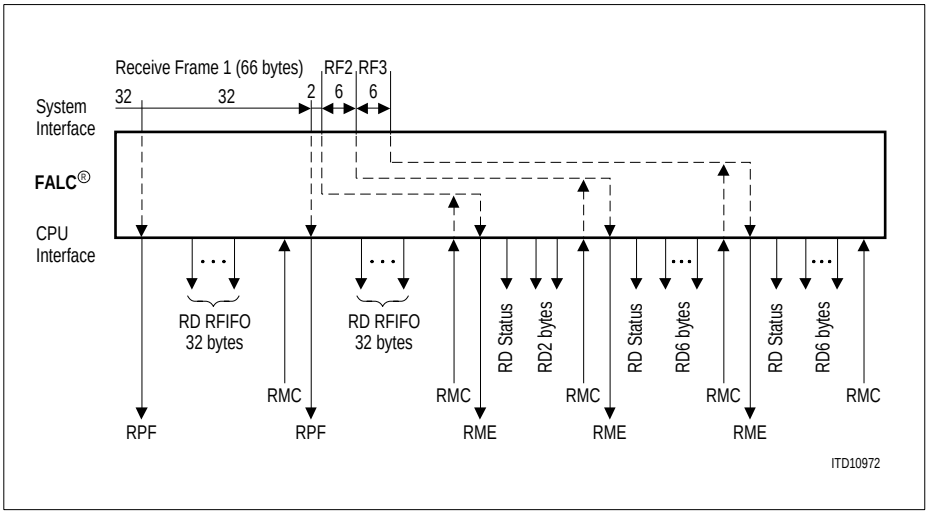


Figure 85 Interrupt Driven Reception Sequence Example

8.3.6 S_a-bit Access (E1)

The QuadFALC supports the S_a-bit signaling of time slot 0 of every other frame as follows:

- Access via registers RSW/XSW
- Access via registers RSA(8:4)/XSA(8:4)
  capable of storing the information for a complete multiframe
- Access via the 64 byte deep receive/transmit FIFO of the integrated signaling controller. This S_a-bit access gives the opportunity to transmit/receive a transparent bit stream as well as HDLC frames where the signaling controller automatically processes the HDLC protocol. Enabling is done by setting of bit CCR1.EITS and resetting of registers TTR(4:1), RTR(4:1) and FMR1.ENSA.

Data written to the XFIFO will be transmitted subsequently in the S_a-bit positions defined by register XC0.SA(8:4)E and the corresponding bits of TSWM.TSA(8:4). Any combination of S_a-bits can be selected. After the data has been sent out completely an “all ones” or Flags (CCR1.ITF) is transmitted. The continuous transmission of a transparent bit stream, which is stored in the XFIFO, can be enabled.
With the setting of bit MODE.HRAC the received S_a-bits can be forwarded to the receive FIFO.
The access to and from the FIFOs is supported by ISR0.RME/RPF and ISR1.XPR/ALS.

8.3.7 Bit Oriented Message Mode (T1/J1)

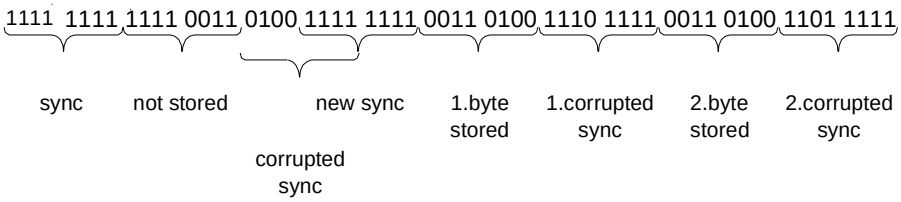
The QuadFALC supports signaling and maintenance functions for T1/J1 primary rate Interfaces using the Extended Super Frame format. The device supports the DL-channel protocol for ESF format according to T1.403-1989 ANSI or to AT&T TR54016 specification. The HDLC and Bit Oriented Message (BOM) -Receiver can be switched on/off independently. If the QuadFALC is used for HDLC formats only, the BOM receiver has to be switched off. If HDLC and BOM receiver has been switched on (MODE.HRAC/BRAC), an automatic switching between HDLC and BOM mode is enabled. Storing of received DL-bit information in the RFIFO of the signaling controller and transmitting the XFIFO contents in the DL-bit positions is enabled by CCR1.EDLX/EITS = 10. After hardware-reset (pin $\overline{\text{RES}}$ low) or software-reset (CMDR.RRES = 1) the QuadFALC operates in HDLC mode. If eight or more consecutive ones are detected, the BOM mode is entered. Upon detection of a flag in the data stream, the QuadFALC switches back to HDLC mode. Operating in BOM mode, the QuadFALC is able to receive an HDLC frame immediately, i.e. without any preceding flags.

In BOM mode, the following byte format is assumed (the left most bit is received first; 111111110xxxxxx0).

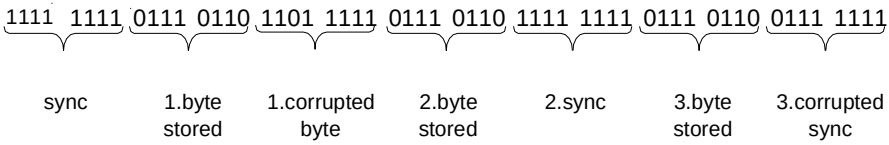
The QuadFALC uses the FF_H byte for synchronization, the next byte is stored in RFIFO (first bit received: LSB) if it starts and ends with a “0”. Bytes starting and ending with a “1” are not stored. If there are no 8 consecutive ones detected within 32 bits, an interrupt is generated. However, byte sampling is not stopped.

Byte sampling in BOM Mode (T1/J1)

a)



b)



Three different BOM reception modes can be programmed (CCR1.BRM, CCR2.RBFE).

10 byte packets: CCR1.BRM = 0
After storing 10 bytes in RFIFO the receive status byte marking a BOM frame (RSIS.HFR) is added as the eleventh byte and an interrupt (ISR0.RME) is generated. The sampling of data bytes continues and interrupts are generated every 10 bytes until an HDLC flag is detected.

Continuous reception: CCR1.BRM = 1
Interrupts are generated every 32 (16, 4, 2) bytes. After detecting an HDLC flag, byte sampling is stopped, the receive status byte is stored in RFIFO and an RME interrupt is generated.

Reception with enabled BOM filter: CCR2.RBFE = 1
The BOM receiver will only accept BOM frames after detecting 7 out of 10 equal BOM pattern. The BOM pattern is stored in the RFIFO adding a receive status byte, marking a BOM frame (RSIS.HFR) and generating an interrupt status ISR0.RME. The current state of the BOM receiver is indicated in register SIS.IVB. When the valid BOM pattern disappears an interrupt ISR0.BIV is generated.

The user can switch between these modes at any time. Byte sampling can be stopped by deactivating the BOM receiver (MODE.BRAC). In this case the receive status byte is added, an interrupt is generated and HDLC mode is entered. Whether the QuadFALC operates in HDLC or BOM mode are checked by reading the signaling status register (SIS.BOM).

8.3.8 Data Link Access in ESF/F72 Format (T1/J1)

The QuadFALC supports the DL-channel protocol using the ESF or F72 (SLC96) format as follows:

- Sampling of DL-bits is done on a multiframe basis and stored in the registers RDL(3:1). A receive multiframe begin interrupt is provided to read the received data DL-bits. The contents of registers XDL(3:1) is subsequently sent out on the transmit multiframe basis if it is enabled via FMR1.EDL. A transmit multiframe begin interrupt requests for writing new information to the DL-bit registers.
- If enabled via CCR1.EDLX/EITS = 10, the DL-bit information is stored in the receive FIFO of the signaling controller. The DL-bits stored in the XFIFO are inserted into the outgoing data stream. If CCR1.EDLX is cleared, a HDLC frame or a transparent frame can be sent or received via the RFIFO/XFIFO.

Register Description

Due to the different device function is E1 and T1/J1 mode, several registers and register bits have dedicated functions according to the selected operation mode.

To maintain easy readability this chapter is divided into separate E1 and T1/J1 sections. Please choose the correct description according to your application (E1 or T1/J1).

9 E1 Registers

9.1 E1 Control Register Addresses

Table 59 E1 Control Register Address Arrangement

Address[1)]	Register	Type	Comment	Page
x00	XFIFO	W	Transmit FIFO	220
x01	XFIFO	W	Transmit FIFO	220
x02	CMDR	W	Command Register	221
x03	MODE	R/W	Mode Register	223
x04	RAH1	R/W	Receive Address High 1	224
x05	RAH2	R/W	Receive Address High 2	224
x06	RAL1	R/W	Receive Address Low 1	224
x07	RAL2	R/W	Receive Address Low 2	224
08	IPC	R/W	Interrupt Port Configuration	225
x09	CCR1	R/W	Common Configuration Register 1	225
x0A	CCR2	R/W	Common Configuration Register 2	227
x0C	RTR1	R/W	Receive Time Slot Register 1	228
x0D	RTR2	R/W	Receive Time Slot Register 2	228
x0E	RTR3	R/W	Receive Time Slot Register 3	228
x0F	RTR4	R/W	Receive Time Slot Register 4	228
x10	TTR1	R/W	Transmit Time Slot Register 1	230
x11	TTR2	R/W	Transmit Time Slot Register 2	230
x12	TTR3	R/W	Transmit Time Slot Register 3	230
x13	TTR4	R/W	Transmit Time Slot Register 4	230
x14	IMR0	R/W	Interrupt Mask Register 0	231
x15	IMR1	R/W	Interrupt Mask Register 1	231
x16	IMR2	R/W	Interrupt Mask Register 2	231
x17	IMR3	R/W	Interrupt Mask Register 3	231
x18	IMR4	R/W	Interrupt Mask Register 4	231
x1B	IERR	R/W	Single Bit Error Insertion Register	231
x1C	FMR0	R/W	Framer Mode Register 0	232
x1D	FMR1	R/W	Framer Mode Register 1	234

Table 59 E1 Control Register Address Arrangement (cont'd)

Address[1)]	Register	Type	Comment	Page
x1E	FMR2	R/W	Framer Mode Register 2	236
x1F	LOOP	R/W	Channel Loop Back	237
x20	XSW	R/W	Transmit Service Word	238
x21	XSP	R/W	Transmit Spare Bits	239
x22	XC0	R/W	Transmit Control 0	240
x23	XC1	R/W	Transmit Control 1	241
x24	RC0	R/W	Receive Control 0	242
x25	RC1	R/W	Receive Control 1	243
x26	XPM0	R/W	Transmit Pulse Mask 0	245
x27	XPM1	R/W	Transmit Pulse Mask 1	245
x28	XPM2	R/W	Transmit Pulse Mask 2	245
x29	TSWM	R/W	Transparent Service Word Mask	246
x2B	IDLE	R/W	Idle Channel Code	247
x2C	XSA4	R/W	Transmit S_a4-Bit Register	247
x2D	XSA5	R/W	Transmit S_a5-Bit Register	247
x2E	XSA6	R/W	Transmit S_a6-Bit Register	247
x2F	XSA7	R/W	Transmit S_a7-Bit Register	247
x30	XSA8	R/W	Transmit S_a8-Bit Register	247
x31	FMR3	R/W	Framer Mode Register 3	248
x32	ICB1	R/W	Idle Channel Register 1	249
x33	ICB2	R/W	Idle Channel Register 2	249
x34	ICB3	R/W	Idle Channel Register 3	249
x35	ICB4	R/W	Idle Channel Register 4	249
x36	LIM0	R/W	Line Interface Mode 0	250
x37	LIM1	R/W	Line Interface Mode 1	252
x38	PCD	R/W	Pulse Count Detection	253
x39	PCR	R/W	Pulse Count Recovery	254
x3A	LIM2	R/W	Line Interface Mode 2	254
x3B	LCR1	R/W	Loop Code Register 1	255
x3C	LCR2	R/W	Loop Code Register 2	257

Table 59 E1 Control Register Address Arrangement (cont'd)

Address[1)]	Register	Type	Comment	Page
x3D	LCR3	R/W	Loop Code Register 3	257
x3E	SIC1	R/W	System Interface Control 1	258
x3F	SIC2	R/W	System Interface Control 2	259
x40	SIC3	R/W	System Interface Control 3	261
x44	CMR1	R/W	Clock Mode Register 1	262
x45	CMR2	R/W	Clock Mode Register 2	264
x46	GCR	R/W	Global Configuration Register	266
x47	ESM	R/W	Errored Second Mask	267
x60	DEC	W	Disable Error Counter	267
x70	XS1	W	Transmit CAS Register 1	268
x71	XS2	W	Transmit CAS Register 2	268
x72	XS3	W	Transmit CAS Register 3	268
x73	XS4	W	Transmit CAS Register 4	268
x74	XS5	W	Transmit CAS Register 5	268
x75	XS6	W	Transmit CAS Register 6	268
x76	XS7	W	Transmit CAS Register 7	268
x77	XS8	W	Transmit CAS Register 8	268
x78	XS9	W	Transmit CAS Register 9	268
x79	XS10	W	Transmit CAS Register 10	268
x7A	XS11	W	Transmit CAS Register 11	268
x7B	XS12	W	Transmit CAS Register 12	268
x7C	XS13	W	Transmit CAS Register 13	268
x7D	XS14	W	Transmit CAS Register 14	268
x7E	XS15	W	Transmit CAS Register 15	268
x7F	XS16	W	Transmit CAS Register 16	268
x80	PC1	R/W	Port Configuration 1	269
x81	PC2	R/W	Port Configuration 2	269
x82	PC3	R/W	Port Configuration 3	269
x83	PC4	R/W	Port Configuration 4	269
x84	PC5	R/W	Port Configuration 5	271

Table 59 E1 Control Register Address Arrangement (cont'd)

Address[1)]	Register	Type	Comment	Page
85	GPC1	R/W	Global Port Configuration 1	272
x87	CMDR2	W	Command Register 2	274
x8D	CCR5	R/W	Common Control Register 5	275
92	GCM1	R/W	Global Counter Mode 1	276
93	GCM2	R/W	Global Counter Mode 2	276
94	GCM3	R/W	Global Counter Mode 3	276
95	GCM4	R/W	Global Counter Mode 4	277
96	GCM5	R/W	Global Counter Mode 5	277
97	GCM6	R/W	Global Counter Mode 6	277
98	GCM7	R/W	Global Counter Mode 7	278
99	GCM8	R/W	Global Counter Mode 8	278
xA0	TSEO	R/W	Time Slot Even/Odd Select	281
xA1	TSBS1	R/W	Time Slot Bit Select 1	281
xA8	TPC0	R/W	Test Pattern Control Register 0	282

1) x = 0: channel 1 register; x = 1: channel 2 register; x = 2: channel 3 register; x = 3: channel 4 register

After reset all control registers except the XFIFO and XS(16:1) are initialized to defined values. Unused bits have to be cleared.

9.2 Detailed Description of E1 Control Registers

Transmit FIFO (Write)

	7		0	
XFIFO	XF7		XF0	(x00)
XFIFO	XF15		XF8	(x01)

Writing data to XFIFO can be done in 8-bit (byte) or 16-bit (word) access. The LSB is transmitted first.

Up to 32 bytes/16 words of transmit data can be written to the XFIFO following a XPR interrupt.

Command Register (Write)

Value after reset: 00_H

	7							0	
CMDR	RMC	RRES	XREP	XRES	XHF	XTF	XME	SRES	(x02)

RMC **Receive Message Complete**

Confirmation from CPU to QuadFALC that the current frame or data block has been fetched following a RPF or RME interrupt, thus the occupied space in the RFIFO can be released. If RMC is given while RFIFO is already cleared, the next incoming data block is cleared instantly, although interrupts are generated.

RRES **Receiver Reset**

The receive line interface except the clock and data recovery unit (DPLL), the receive framer, the one-second timer and the receive signaling controller are reset. However the contents of the control registers is not deleted.

XREP **Transmission Repeat**

If XREP is set together with XTF (write 24_H to CMDR), the QuadFALC repeatedly transmits the contents of the XFIFO (1 to 32 bytes) without HDLC framing fully transparently, i.e. without flag, CRC.

The cyclic transmission is stopped with a SRES command or by resetting XREP.

Note:During cyclic transmission the XREP-bit has to be set with every write operation to CMDR.

XRES **Transmitter Reset**

The transmit framer and transmit line interface excluding the system clock generator and the pulse shaper are reset. However the contents of the control registers is not deleted.

XHF **Transmit HDLC Frame**

After having written up to 32 bytes to the XFIFO, this command initiates the transmission of a HDLC frame.

XTF **Transmit Transparent Frame**

Initiates the transmission of a transparent frame without HDLC framing.

XME **Transmit Message End**

Indicates that the data block written last to the transmit FIFO completes the current frame. The QuadFALC can terminate the transmission operation properly by appending the CRC and the closing flag sequence to the data.

SRES **Signaling Transmitter Reset**

The transmitter of the signaling controller is reset. XFIFO is cleared of any data and an abort sequence (seven 1's) followed by interframe time fill is transmitted. In response to SRES a XPR interrupt is generated.

This command can be used by the CPU to abort a frame currently in transmission.

Note: The maximum time between writing to the CMDR register and the execution of the command takes 2.5 periods of the current system data rate. Therefore, if the CPU operates with a very high clock rate in comparison with the QuadFALC's clock, it is recommended that bit SIS.CEC should be checked before writing to the CMDR register to avoid any loss of commands.

Note: If SCLKX is used to clock the transmission path, commands to the HDLC transmitter should only be sent while this clock is available. If SCLKX is missing, the command register is blocked after an HDLC command is given.

Mode Register (Read/Write)

Value after reset: 00_H

	7							0	
MODE	MDS2	MDS1	MDS0		HRAC	DIV			(x03)

MDS(2:0) **Mode Select**

The operating mode of the HDLC controller is selected.

000 Reserved
001 Signaling System 7 (SS7) support[1)]
010 1 byte address comparison mode (RAL1,2)
011 2 byte address comparison mode (RAH1,2 and RAL1,2)
100 No address comparison
101 1 byte address comparison mode (RAH1,2)
110 Reserved
111 No HDLC framing mode

HRAC **Receiver Active**

Switches the HDLC receiver to operational or inoperational state.

0 Receiver inactive
1 Receiver active

DIV **Data Inversion**

Setting this bit inverts the internal generated HDLC data stream.

0 normal operation, HDLC data stream not inverted
1 HDLC data stream inverted

1) CCR2.RADD must be set, if SS7 mode is selected

Receive Address Byte High Register 1 (Read/Write)
Value after reset: FD_H

	7			0	
RAH1			0		(x04)

In operating modes that provide high byte address recognition, the high byte of the received address is compared to the individually programmable values in RAH1 and RAH2.

RAH1 **Value of the First Individual High Address Byte**

Bit 1 (C/R-bit) is excluded from address comparison.

Receive Address Byte High Register 2 (Read/Write)
Value after reset: FF_H

	7		0	
RAH2				(x05)

RAH2 **Value of Second Individual High Address Byte**

Receive Address Byte Low Register 1 (Read/Write)
Value after reset: FF_H

	7		0	
RAL1				(x06)

RAL1 **Value of First Individual Low Address Byte**

Receive Address Byte Low Register 2 (Read/Write)
Value after reset: FF_H

	7		0	
RAL2				(x07)

RAL2 **Value of the second individually programmable low address byte.**

Interrupt Port Configuration (Read/Write)

Value after reset: 00_H

	7							0	
IPC						SSYF	IC1	IC0	(08)

Note: Unused bits have to be cleared.

SSYF **Select SYNC Frequency**

Only applicable in master mode (LIM0.MAS = 1) and bit CMR2.DCF is cleared.

0 Reference clock at port SYNC is 2.048 MHz
1 Reference clock at port SYNC is 8 kHz

IC0, IC1 **Interrupt Port Configuration**

These bits define the function of the interrupt output stage (pin INT):

IC1	IC0	Function
X	0	Open drain output
0	1	Push/pull output, active low
1	1	Push/pull output, active high

Common Configuration Register 1 (Read/Write)

Value after reset: 00_H

	7							0	
CCR1		XTS16RA	CASM	EITS	ITF	XMFA	RFT1	RFT0	(x09)

XTS16RA **Send Remote Alarm in Time Slot 16**

Sending of remote alarm in time slot 16 towards remote end by setting bit 'Y' in the CAS multiframe alignment word. If XS registers are used for CAS (instead of XSIG), bit XS1.2 ('Y') is logically ored with XTS16RA. If XSIG is used for CAS, Y-data received on XSIG is logically ored with XTS16RA.

0 no remote alarm insertion
1 remote alarm insertion

CASM **CAS Synchronization Mode**

Determines the synchronization mode of the channel associated signaling multiframe alignment.

0 Synchronization is done in accordance to ITU-T G. 732

1 Synchronization is established when two consecutively correct multiframe alignment pattern are found.

EITS **Enable Internal Time Slot (31:0) Signaling**

0 Internal signaling in time slots (31:0) defined by registers RTR(4:1) or TTR(4:1) is disabled.

1 Internal signaling in time slots (31:0) defined by registers RTR(4:1) or TTR(4:1) is enabled.

ITF **Interframe Time Fill**

Determines the idle (= no data to be sent) state of the transmit data coming from the signaling controller.

0 Continuous logical ’1’ is output

1 Continuous flag sequences are output (’01111110’ bit patterns)

XMFA **Transmit Multiframe Aligned**

Determines the synchronization between the framer and the corresponding signaling controller.

0 The contents of the XFIFO is transmitted without multiframe alignment.

1 The contents of the XFIFO is transmitted multiframe aligned.
The first byte in XFIFO is transmitted in the first time slot selected by TTR(4:1) and so on.
After reception of a complete multiframe in the time slot mode (RTR(4:1)) an ISR0.RME interrupt is generated, if no HDLC mode is enabled
In S_a4...8-bit access mode XMFA is not valid.

Note: During the transmission of the XFIFO content, the $\overline{SYPX}$ or XMFS interval time should not be changed, otherwise the XFIFO data has to be retransmitted.

RFT(1:0) **RFIFO Threshold Level**

The size of the accessible part of RFIFO can be determined by programming these bits. The number of valid bytes after a RPF interrupt is given in the following table:

RFT1	RFT0	Size of Accessible Part of RFIFO
0	0	32 bytes (reset value)
0	1	16 bytes
1	0	4 bytes
1	1	2 bytes

The value of RFT1, 0 can be changed dynamically.

– If reception is not running or

– after the current data block has been read, but before the command CMDR.RMC is issued (interrupt controlled data transfer).

Note: It is seen that changing the value of RFT1, 0 is possible even during the reception of one frame. The total length of the received frame can be always read directly in RBCL, RBCH after a RPF interrupt, except when the threshold is increased during reception of that frame. The real length can then be inferred by noting which bit positions in RBCL are reset by a RMC command (see table below):

RFT1	RFT0	Bit Positions in RBCL Reset by a CMDR.RMC Command
0	0	RBC(4:0)
0	1	RBC(3:0)
1	0	RBC(1:0)
1	1	RBC0

Common Configuration Register 2 (Read/Write)

Value after reset: 00_H

	7							0	
CCR2				RADD		RCRC	XCRC		(x0A)

Note: Unused bits have to be cleared.

RADD **Receive Address Pushed to RFIFO**

If this bit is set, the received HDLC address information (1 or 2 bytes, depending on the address mode selected by MODE.MDS0) is pushed to RFIFO. This function is applicable in non-auto mode and transparent mode 1. RADD must be set, if SS7 mode is selected.

RCRC **Receive CRC on/off**

Only applicable in non-auto mode.

If this bit is set, the received CRC checksum is written to RFIFO (CRC-ITU-T: 2 bytes). The checksum, consisting of the 2 last bytes in the received frame, is followed by the status information byte (contents of register RSIS). The received CRC checksum is additionally checked for correctness. If non-auto mode is selected, the limits for “valid frame” check are modified (refer to RSIS.VFR).

XCRC **Transmit CRC on/off**

If this bit is set, the CRC checksum is not generated internally. It has to be written to the transmit FIFO as the last two bytes. The transmitted frame is closed automatically with a closing flag.

Note: The QuadFALC does not check whether the length of the frame, i.e. the number of bytes to be transmitted makes sense or not.

Receive Time Slot Register (4:1) (Read/Write)

Value after reset: 00_H, 00_H, 00_H, 00_H

	7							0	
RTR1	TS0	TS1	TS2	TS3	TS4	TS5	TS6	TS7	(x0C)
RTR2	TS8	TS9	TS10	TS11	TS12	TS13	TS14	TS15	(x0D)
RTR3	TS16	TS17	TS18	TS19	TS20	TS21	TS22	TS23	(x0E)
RTR4	TS24	TS25	TS26	TS27	TS28	TS29	TS30	TS31	(x0F)

TS(31:0) **Time Slot**

These bits define the received time slots on the system highway port RDO to be extracted to RFIFO and marked. Additionally these registers control the RSIGM marker which can be forced high during the corresponding time slots independently of bit CCR1.EITS.
A one in the RTR(4:1) bits samples the corresponding time slots and

send their data to the RFIFO of the signaling controller if bit CCR1.EITS is set.

Assignments:
TS0→time slot 0

...

TS31 → time slot 31

0 The corresponding time slot is not extracted and stored into the RFIFO.

1 The contents of the selected time slot is stored in the RFIFO. Although the idle time slots can be selected. This function is activated, if bit CCR1.EITS is set.
The corresponding time slot is forced high on marker pin RSIGM.

Transmit Time Slot Register (4:1) (Read/Write)

Value after reset: 00_H, 00_H, 00_H, 00_H

	7							0	
TTR1	TS0	TS1	TS2	TS3	TS4	TS5	TS6	TS7	(x10)
TTR2	TS8	TS9	TS10	TS11	TS12	TS13	TS14	TS15	(x11)
TTR3	TS16	TS17	TS18	TS19	TS20	TS21	TS22	TS23	(x12)
TTR4	TS24	TS25	TS26	TS27	TS28	TS29	TS30	TS31	(x13)

TS(31:0) **Time Slot**

These bits define the transmit time slots on the system highway to be inserted. Additionally these registers control the XSIGM marker which can be forced high during the corresponding time slots independently of bit CCR1.EITS.
A one in the TTR(4:1) bits inserts the corresponding time slot sourced by the XFIFO in the data received on pin XDI, if bit CCR1.EITS is set. If SIC3.TTRF is set and CCR1.EITS is cleared insertion of data received on port XSIG is controlled by this registers.

Assignments:
TS0→time slot 0

...
TS31 → time slot 31

0 The selected time slot is not inserted into the outgoing data stream.

1 The contents of the selected time slot is inserted into the outgoing data stream from XFIFO. This function is active only if bit CCR1.EITS is set.
The corresponding time slot is forced high on marker pin XSIGM.

Interrupt Mask Register (4:0) (Read/Write)

Value after reset: FF_H, FF_H, FF_H, FF_H, FF_H

	7							0	
IMR0	RME	RFS	T8MS	RMB	CASC	CRC4	SA6SC	RPF	(x14)
IMR1	LLBSC	RDO	ALLS	XDU	XMB	SUEX	XLSC	XPR	(x15)
IMR2	FAR	LFA	MFAR	T400MS	AIS	LOS	RAR	RA	(x16)
IMR3	ES	SEC	LMFA16	AIS16	RA16		RSN	RSP	(x17)
IMR4	XSP	XSN							(x18)

IMR(4:0) **Interrupt Mask Register**

Each interrupt source can generate an interrupt signal on port INT (characteristics of the output stage are defined by register IPC). A “1” in a bit position of IMR(4:0) sets the mask active for the interrupt status in ISR(4:0). Masked interrupt statuses neither generate a signal on INT, nor are they visible in register GIS. Moreover, they are
- not displayed in the interrupt status register if bit GCR.VIS is cleared
- displayed in the interrupt status register if bit GCR.VIS is set

*Note: After reset, all interrupts are **dis**abled.*

Single Bit Defect Insertion Register (Read/Write)

Value after reset: 00_H

IERR			IFASE	IMFE	ICRCE	ICASE	IPE	IBV	(x1B)

After setting the corresponding bit, the selected defect is inserted into the transmit data stream at the next possible position. After defect insertion is completed, the bit is reset automatically.

IFASE **Insert single FAS defect**

IMFE **Insert single multiframe defect**

ICRCE **Insert single CRC defect**

ICASE **Insert single CAS defect**

IPE **Insert single PRBS defect**

IBV **Insert bipolar violation**

Note:Except for CRC defects, CRC checksum calculation is done after defect insertion.

Framer Mode Register 0 (Read/Write)

Value after reset: 00_H

	7							0	
FMR0	XC1	XC0	RC1	RC0	EXZE	ALM	FRS	SIM	(x1C)

XC(1:0) **Transmit Code**

Serial line code for the transmitter, independent of the receiver.

00 NRZ (optical interface)

01 CMI (1T2B+HDB3), (optical interface)

10 AMI (ternary or digital dual rail interface)

11 HDB3 Code (ternary or digital dual rail interface)

After changing XC1/0, a transmitter software reset is required (CMDR.XRES = 1).

RC(1:0) **Receive Code**

Serial line code for the receiver, independent of the transmitter.

00 NRZ (optical interface)

01 CMI (1T2B+HDB3), (optical interface)

10 AMI (ternary or digital dual rail interface)

11 HDB3 Code (ternary or digital dual rail interface)

After changing RC1/0, a receiver software reset is required (CMDR.RRES = 1).

EXZE **Extended HDB3 Error Detection**

Selects error detection mode.

0 Only double violations are detected.

1 Extended code violation detection: 0000 strings are detected additionally. Incrementing of the code violation counter CVC is done after receiving four zeros. Errors are indicated by FRS1.EXZD = 1.

ALM **Alarm Mode**

Selects the AIS alarm detection mode.

0 The AIS alarm is detected according to ETS300233.
Detection: An AIS alarm is detected if the incoming data stream contains less than 3 zeros within a period of 512 bits and a loss of frame alignment is indicated.
Recovery: The alarm is cleared if 3 or more zeros within 512 bits are detected or the FAS word is found.

1 The AIS alarm is detected according to ITU-T G.775
Detection: An AIS alarm is detected if the incoming data stream contains less than 3 zeros in each doubleframe period of two consecutive doubleframe periods (1024 bits).
Recovery: The alarm is cleared if 3 or more zeros are detected within two consecutive doubleframe periods.

FRS **Force Resynchronization**

A transition from low to high initiates a resynchronization procedure of the pulse frame and the CRC-multiframe (if enabled by bit FMR2.RFS1) starting directly after the old framing candidate.

SIM **Alarm Simulation**

0 Normal operation.

1 Initiates internal error simulation of AIS, loss of signal, loss of synchronization, remote alarm, slip, framing errors, CRC errors, and code violations. The error counters FEC, CVC, CEC1 are incremented.

SIM has to be held stable at high or low level for at least one receive clock period before changing it again.

Framer Mode Register 1 (Read/Write)

Value after reset: 00_H

	7						0	
FMR1	MFCS	AFR	ENSA	PMOD	XFS	ECM	SSD0	XAIS	(x1D)

MFCS **Multiframe Force Resynchronization**

Only valid if CRC multiframe format is selected (FMR2.RFS1/0 = 10).

A transition from low to high initiates the resynchronization procedure for CRC-multiframe alignment without influencing doubleframe synchronous state. In case, “Automatic Force Resynchronization” (FMR1.AFR) is enabled and multiframe alignment can not be regained, a new search of doubleframe (and CRC multiframe) is automatically initiated.

AFR **Automatic Force Resynchronization**

Only valid if CRC multiframe format is selected (FMR2.RFS1/0 = 10).

If this bit is set, a search of doubleframe alignment is automatically initiated if two multiframe patterns with a distance of n × 2 ms have not been found within a time interval of 8 ms after doubleframe alignment has been regained or command FMR1.MFCS has been issued.

ENSA **Enable S_a-Bit Access through Register XSA4-8**

Only applicable if FMR1.XFS is set.

0 Normal operation. The S_a-bit information is taken from bits XSW.XY(4:0) and written to bits RSW.RY(4:0).

1 S_a-bit register access. The S_a-bit information is taken from the registers XSA(4:8). In addition, the received information is written to registers RSA(4:8). Transmitting of the contents of registers XSA(4:8) is disabled if one of time slot 0 transparent modes is enabled (XSP.TT0 or TSWM.SA(4:8)).

PMOD **PCM Mode**

For E1 application this bit must be set low. Switching from E1 to T1 or vice versa the device needs up to 20 µs to settle up to the internal clocking.

0= PCM 30 or E1 mode.

1= PCM 24 or T1/J1 mode (see RC0.SJR for T1/J1 selection).

XFS **Transmit Framing Select**

Selection of the transmit framing format can be done independently of the receive framing format.

0 Doubleframe format enabled.

1 CRC4-multiframe format enabled.

ECM **Error Counter Mode**

The function of the error counters is determined by this bit.

0= Before reading an error counter the corresponding bit in the Disable Error Counter register (DEC) has to be set. In 8 bit access the low byte of the error counter should always be read before the high byte. The error counters are reset with the rising edge of the corresponding bits in the DEC register.

1= Every second the error counter is latched and then automatically reset. The latched error counter state should be read within the next second. Reading the error counter during updating should be avoided (do not access an error counter within 1 µs after the one-second interrupt occurs).

SSD0 **Select System Data Rate 0**

FMR1.SSD0 and SIC1.SSD1 define the data rate on the system highway. Programming is done with SSD1/SSD0 in the following table.

00= 2.048 Mbit/s

01= 4.096 Mbit/s

10= 8.192 Mbit/s

11= 16.384 Mbit/s

XAIS **Transmit AIS Towards Remote End**

Sends AIS on ports XL1, XL2, XOID towards the remote end. The outgoing data stream which can be looped back through the local loop to the system interface is not affected.

Framer Mode Register 2 (Read/Write)

Value after reset: 00_H

	7							0	
FMR2	RFS1	RFS0	RTM	DAIS	SAIS	PLB	AXRA	ALMF	(x1E)

RFS(1:0) **Receive Framing Select**

00 Doubleframe format

01 Doubleframe format

10 CRC4 Multiframe format

11 CRC4 Multiframe format with modified CRC4 Multiframe alignment algorithm (Interworking according to ITU-T G.706 Annex B). Setting of FMR3.EXTIW changes the reaction after the 400 ms time-out.

RTM **Receive Transparent Mode**

Setting this bit disconnects control of the internal elastic store from the receiver. The elastic store is now in a “free running” mode without any possibility to actualize the time slot assignment to a new frame position in case of resynchronization of the receiver. This function can be used together with the “disable AIS to system interface” feature (FMR2.DAIS) to realize undisturbed transparent reception.
This bit should be enabled in case of unframed data reception mode.

DAIS **Disable AIS to System Interface**

0 AIS is automatically inserted into the data stream to RDO if QuadFALC is in asynchronous state.

1 Automatic AIS insertion is disabled. Furthermore, AIS insertion can be initiated by programming bit FMR2.SAIS.

SAIS **Send AIS Towards System Interface**

Sends AIS on output RDO towards system interface. This function is not influenced by bit FMR2.DAIS.

PLB **Payload Loopback**

0 Normal operation. Payload loop is disabled.

1 The payload loopback loops the data stream from the receiver section back to transmitter section. Looped data is output on pin RDO. Data received on port XDI, XSIG, $\overline{\text{SYPX}}$ and XMFS is ignored. With XSP.TT0 = 1 time slot 0 is also looped back. If XSP.TT0 = 0 time slot 0 is generated internally. AIS is sent

immediately on port RDO by setting the FMR2.SAIS bit. It is recommended to write the actual value of XC1 into this register once again, because a write access to register XC1 sets the read/write pointer of the transmit elastic buffer into its optimal position to ensure a maximum wander compensation (the write operation forces a slip).

AXRA **Automatic Transmit Remote Alarm**

0 Normal operation

1 The remote alarm bit is set automatically in the outgoing data stream if the receiver is in asynchronous state (FRS0.LFA bit is set). In synchronous state the remote alarm bit is reset. Additionally in multiframe format FMR2.RFS1 = 1 and FMR3.EXTIW = 1 and the 400 ms time-out has elapsed, the remote alarm bit is active in the outgoing data stream. In multiframe synchronous state the outgoing remote alarm bit is cleared.

ALMF **Automatic Loss of Multiframe**

0 Normal operation

1 The receiver searches a new basic- and multiframing if more than 914 CRC errors have been detected in a time interval of one second. The internal 914 CRC error counter is reset if the multiframe synchronization is found. Incrementing the counter is only enabled in the multiframe synchronous state.

Channel Loop Back (Read/Write)

Value after reset: 00_H

	7							0	
LOOP			ECLB	CLA4	CLA3	CLA2	CLA1	CLA0	(x1F)

ECLB **Enable Channel Loop Back**

0 Disables the channel loop back.

1 Enables the channel loop back selected by this register.

CLA(4:0) **Channel Address For Loop Back**

CLA = 31 to 0 selects the channel.

During looped back the contents of the assigned outgoing channel on ports XL1/XDOP/XOID and XL2/XDON is equal to the idle channel code programmed at register IDLE.

Transmit Service Word Pulseframe (Read/Write)

Value after reset: 00_H

	7							0	
XSW	XSIS	XTM	XRA	XY0	XY1	XY2	XY3	XY4	(x20)

XSIS **Spare Bit For International Use**

First bit of the service word. Only significant in doubleframe format. If not used, this bit should be fixed to '1'. If one of the time slot 0 transparent modes is enabled (bit XSP.TT0, or TSWM.TSIS), bit XSW.XSIS is ignored.

XTM **Transmit Transparent Mode**

0= Ports $\overline{\text{SYPX}}$/XMFS define the frame/multiframe begin on the transmit system highway. The transmitter is usually synchronized on this externally sourced frame boundary and generates the FAS-bits according to this framing. Any change of the transmit time slot assignment subsequently produces a change of the FAS-bit positions.

1= Disconnects the control of the transmit system interface from the transmitter. The transmitter is now in a free running mode without any possibility to actualize the multiframe position. The framing (FAS-bits) generated by the transmitter is not "disturbed" (in case of changing the transmit time slot assignment) by the transmit system highway unless register XC1 is written. Useful in loop-timed applications. For proper operation the transmit elastic buffer (2 frames, SIC1.XBS1/0 = 10) has to be enabled.

XRA **Transmit Remote Alarm**

0 Normal operation.

1 Sends remote alarm towards remote end by setting bit 3 of the service word. If time slot 0 transparent mode is enabled by bit XSP.TT0 or TSWM.TRA bit is set, bit XSW.XRA is ignored.

XY(4:0) **Spare Bits For National Use (Y-Bits, S_n-Bits, S_a-Bits)**

These bits are inserted in the service word of every other pulseframe if S_a-bit register access is disabled (FMR1.ENSA = 0). If not used, they should be fixed to "1".

If one of the time slot 0 transparent modes is enabled (bit XSP.TT0 or TSWM.TSA(8:4)), bits XSW.XY(4:0) are ignored.

Transmit Spare Bits (Read/Write)

Value after reset: 00_H

	7							0	
XSP		CASEN	TT0	EBP	AXS	XSIF	XS13	XS15	(x21)

CASEN **Channel Associated Signaling Enable**

0 Normal operation.

1 A one in this bit position causes the transmitter to send the CAS information stored in the XS(16:1) registers or serial CAS data in the corresponding time slots.

TT0 **Time slot 0 Transparent Mode**

0 Normal operation.

1 All information for time slot 0 at port XDI is inserted in the outgoing pulseframe. All internal information of the QuadFALC (framing, CRC, S_a/S_i-bit signaling, remote alarm) is ignored. This function is mainly useful for system test applications (test loops). Priority sequence of transparent modes: XSP.TTO > TSWM.

EBP **E-Bit Polarity**

0 In the basic- and multiframe asynchronous state the E-bit is cleared.

1 In the basic- and multiframe asynchronous state the E-bit is set.

If automatic transmission of submultiframe status is enabled by setting bit XSP.AXS and the receiver has lost synchronization, the E-bit with the programmed polarity is inserted automatically in S_i-bit position of every outgoing CRC multiframe (under the condition that time slot 0 transparent mode and transparent S_i bit in service word are both disabled).

AXS **Automatic Transmission of Submultiframe Status**

Only applicable to CRC multiframe.

0 Normal operation.

1 Information of submultiframe status bits RSP.SI1 and RSP.SI2 are inserted automatically in S_i -bit positions of the outgoing CRC multiframe (RSP.SI1 $\rightarrow$ S_i -bit of frame 13; RSP.SI2 $\rightarrow$ S_i-bit of frame 15). Contents of XSP.XS13 and XSP.XS15 is

ignored. If one of the time slot 0 transparent modes XSP.TT0 or TSWM.TSIS is enabled, bit XSP.AXS has no function.

XSIF **Transmit Spare Bit For International Use (FAS Word)**

First bit in the FAS word. Only significant in doubleframe format. If not used, this bit should be fixed to '1'. If one of the time slot 0 transparent modes is enabled (bits XSP.TT0, or TSWM.TSIF), bit XSP.XSIF is ignored.

XS13 **Transmit Spare Bit (Frame 13, CRC-Multiframe)**

First bit in the service word of frame 13 for international use. Only significant in CRC-multiframe format. If not used, this bit should be fixed to '1'. The information of XSP.XS13 is shifted into internal transmission buffer with beginning of the next following transmitted CRC multiframe.

If automatic transmission of submultiframe status is enabled by bit XSP.AXS, or, if one of the time slot 0 transparent modes XSP.TT0 or TSWM.TSIS is enabled, bit XSP.XS13 is ignored.

XS15 **Transmit Spare Bit (Frame 15, CRC-Multiframe)**

First bit in the service word of frame 15 for international use. Only significant in CRC-multiframe format. If not used, this bit should be fixed to '1'. The information of XSP.XS15 is shifted into the internal transmission buffer with beginning of the next following transmitted CRC multiframe.

If automatic transmission of submultiframe status is enabled by bit XSP.AXS, or, if one of the time slot 0 transparent modes XSP.TT0 or TSWM.TSIF is enabled, bit XSP.XS15 is ignored.

Transmit Control 0 (Read/Write)

Value after reset: 00_H

	7							0	
XC0	SA8E	SA7E	SA6E	SA5E	SA4E	XCO10	XCO9	XCO8	(x22)

SA(8:4)E **S_a-Bit Signaling Enable**

0 Standard operation.

1 Setting this bit makes it possible to send/receive a LAPD protocol in any combination of the S_a8...S_a4-bit positions in the outgoing/incoming data stream. The on chip signaling controller

has to be configured in the HDLC/LAPD mode. In transmit direction together with these bits the TSWM.TSA(4:8) bits must be set to enable transmission to the remote end transparently through the QuadFALC.

XCO(10:8) **Transmit Offset**

Initial value loaded into the transmit bit counter at the trigger edge of SCLKX when the synchronous pulse at port $\overline{\text{SYPX}}$/XMFS is active Refer to register XC1.

Transmit Control 1 (Read/Write)

Value after reset: $9C_H$

	7		0	
XC1	XCO7		XCO0	(x23)

A write access to this address resets the transmit elastic buffer to its basic starting position. Therefore, updating the value should only be done when the QuadFALC is initialized or when the buffer should be centered. As a consequence a transmit slip will occur.

XCO(7:0) **Transmit Offset**

Calculation of delay time T (SCLKX cycles) depends on the value X of the “Transmit Offset” register XC1/0:

$0 \leq T \leq 4$: X = 4 - T

$5 \leq T \leq$ maximum delay:X = 256 $\times$ SC/SD - T + 4

with maximum delay = (256 $\times$ SC/SD) -1
with SC = system clock defined by SIC1.SSC1/0
with SD = 2.048 Mbit/s

Delay time T = time between beginning of time slot 0 (bit 0, channel phase 0) at XDI/XSIG and the initial edge of SCLKX after $\overline{\text{SYPX}}$/XMFS goes active.

See **page 116** for further description.

Receive Control 0 (Read/Write)

Value after reset: 00_H

	7							0	
RC0	SWD	ASY4	CRCI	XCRCI	RDIS	RCO10	RCO9	RCO8	(x24)

SWD **Service Word Condition Disable**

0 Standard operation. Three or four consecutive incorrect service words (depending on bit RC0.ASY4) causes loss of synchronization.

1 Errors in service words have no influence when in synchronous state. However, they are used for the resynchronization procedure.

ASY4 **Select Loss of Sync Condition**

0 Standard operation. Three consecutive incorrect FAS words or three consecutive incorrect service words causes loss of synchronization.

1 Four consecutive incorrect FAS words or four consecutive incorrect service words causes loss of synchronization. The service word condition is disabled by bit RC0.SWD.

CRCI **Automatic CRC4 Bit Inversion**

If set, all CRC bits of one outgoing submultiframe are inverted in case a CRC error is flagged for the previous received submultiframe. This function is logically ored with RC0.XCRCI.

XCRCI **Transmit CRC4 Bit Inversion**

If set, the CRC bits in the outgoing data stream are inverted before transmission. This function is logically ored with RC0.CRCI.

RDIS **Receive Data Input Sense**

Digital interface, dual rail:

0 Inputs RDIP/RDIN are active low

1 Inputs RDIP/RDIN are active high

Digital Interface, CMI:

0 Input ROID is active high

1 Input ROID is active low

RCO(10:8) **Receive Offset/Receive Frame Marker Offset**

Depending on the RP(A to D) pin function different offsets can be programmed. The $\overline{\text{SYPR}}$ and the RFM pin function can not be selected in parallel.

Receive Offset (PC(4:1).RPC(2:0) = 000)
Initial value loaded into the receive bit counter at the trigger edge of SCLKR when the synchronous pulse at port $\overline{\text{SYPR}}$ is active.

Calculation of delay time T (SCLKR cycles) depends on the value X of the 'Receive Offset" register RC1/0. For programing refer to register RC1.

Receive Frame Marker Offset (PC(4:1).RPC(2:0) = 001)

Offset programming of the receive frame marker which is output on port $\overline{\text{SYPR}}$. The receive frame marker can be activated during any bit position of the current frame.

Calculation of the value X of the 'Receive Offset" register RC1/0 depends on the bit position which should be marked and SCLKR. Refer to register RC1.

Receive Control 1 (Read/Write)

Value after reset: $9C_H$

	7		0	
RC1	RCO7		RCO0	(x25)

RCO(7:0) **Receive Offset/Receive Frame Marker Offset**

Depending on the RP(A to D) pin function different offsets can be programmed. The $\overline{\text{SYPR}}$ and the RFM pin function can not be selected in parallel.

Receive Offset (PC(4:1).RPC(2:0) = 000)
Initial value loaded into the receive bit counter at the trigger edge of SCLKR when the synchronous pulse at port $\overline{\text{SYPR}}$ is active.

Calculation of delay time T (SCLKR cycles) depends on the value X of the 'Receive Offset" register RC1/0:

$0 \leq T \leq 4$: X = 4 - T
$5 \leq T \leq$ maximum delay:X = 2052 - T

with maximum delay = (256×SC/SD) -1
with SC = system clock defined by SIC1.SSC1/0
with SD = system data rate

Delay time T = time between beginning of time slot 0 at RDO and the initial edge of SCLKR after $\overline{\text{SYPR}}$ goes active.

Receive Frame Marker Offset (PC(4:1).RPC(2:0) = 001)

Offset programming of the receive frame marker which is output on multifunction port RFM. The receive frame marker can be activated during any bit position of the entire frame and depends on the selected system clock rate.
Calculation of the value X of the 'Receive Offset' register RC1/0 depends on the bit position which should be marked at marker position MP:

0 ≤ MP ≤ 2045:X = MP + 2
2046 ≤ MP ≤ 2047: X = MP - 2046

e.g: 2.048 MHz: MP = 0 to 255; ... 16.384 MHz: MP = 0 to 2047

See **page 111** for further description.

Transmit Pulse Mask (2:0) (Read/Write)
Value after reset: $7B_H$, 03_H, 40_H

	7							0	
XPM0	XP12	XP11	XP10	XP04	XP03	XP02	XP01	XP00	(x26)
XPM1	XP30	XP24	XP23	XP22	XP21	XP20	XP14	XP13	(x27)
XPM2	0	XLT	DAXLT	0	XP34	XP33	XP32	XP31	(x28)

The transmit pulse shape which is defined in ITU-T G.703 is output on pins XL1 and XL2. The level of the pulse shape can be programmed by registers XPM(2:0) to create a custom waveform. In order to get an optimized pulse shape for the external transformers each pulse shape is internally divided into four sub pulse shapes. In each sub pulse shape a programmed 5 bit value defines the level of the analog voltage on pins XL1/2. Together four 5 bit values have to be programmed to form one complete transmit pulse shape. The four 5 bit values are sent in the following sequence:

XP0(4:0): First pulse shape level
XP1(4:0): Second pulse shape level
XP2(4:0): Third pulse shape level
XP3(4:0): Fourth pulse shape level

Changing the LSB of each subpulse in registers XPM(2:0) changes the amplitude of the differential voltage on XL1/2 by approximately 80 mV.
Example:120 Ω interface and wired as shown in **Figure 55** on **page 160**.

XPM0(4:0): $1C_H$ or 27 decimal
XPM1(4:0): $1C_H$ or 27 decimal
XPM2(4:0): 00_H
XPM3(4:0): 00_H

Programming values for XPM(2:0): $9C_H$, 03_H, 00_H

XLT **Transmit Line Tristate**

0 Normal operation

1 Transmit line XL1/XL2 or XDOP/XDON are switched into high impedance state. If this bit is set the transmit line monitor status information is frozen (default value after hardware reset).

DAXLT **Disable Automatic Tristating of XL1/2**

0 Normal operation. If a short is detected on pins XL1/2 the transmit line monitor sets the XL1/2 outputs into a high impedance state.

1 If a short is detected on XL1/2 pins automatic setting these pins into a high impedance (by the XL-monitor) state is disabled.

Transparent Service Word Mask (Read/Write)

Value after reset: 00_H

	7							0	
TSWM	TSIS	TSIF	TRA	TSA4	TSA5	TSA6	TSA7	TSA8	(x29)

TSWM(7:0) **Transparent Service Word Mask**

TSIS **Transparent S_i-Bit in Service Word**

0 The S_i-Bit is generated internally.

1 The S_i-Bit in the service word is taken from port XDI and transparently passed through the QuadFALC without any changes. The internal information of the QuadFALC (register XSW) is ignored.

TSIF **Transparent S_i-Bit in FAS Word**

0 The S_i-Bit is generated internally.

1 The S_i-Bit in the FAS word is taken from port XDI and routed transparently through the QuadFALC without any changes. The internal information of the QuadFALC (register XSW) is ignored.

TRA **Transparent Remote Alarm**

0 The remote alarm bit is generated internally.

1 The A-Bit is taken from port XDI and routed transparently through the QuadFALC without any changes. The internal information of the QuadFALC (register XSW) is ignored.

TSA(4:8) **Transparent S_a4...8-Bit**

0 The S_a4...8-bits are generated internally.

1 The S_a4...8-bits are taken from port XDI or from the internal signaling controller if enabled and transparently passed through the QuadFALC without any changes. The internal information of the QuadFALC (registers XSW and XSA(8:4)) are ignored.

Idle Channel Code Register (Read/Write)

Value after reset: 00_H

	7							0	
IDLE	IDL7							IDL0	(x2B)

IDL(7:0) **Idle Channel Code**

If channel loop back is enabled by programming LOOP.ECLB = 1, the contents of the assigned outgoing channel on ports XL1/XL2 or XDOP/XDON is set equal to the idle channel code selected by this register.

Additionally, the specified pattern overwrites the contents of all channels selected by the idle channel registers ICB(4:1). IDL7 is transmitted first.

Transmit S_a4...8 Register (Read/Write)

Value after reset: 00_H, 00_H, 00_H, 00_H, 00_H

	7							0	
XSA4	XS47	XS46	XS45	XS44	XS43	XS42	XS41	XS40	(x2C)
XSA5	XS57	XS56	XS55	XS54	XS53	XS52	XS51	XS50	(x2D)
XSA6	XS67	XS66	XS65	XS64	XS63	XS62	XS61	XS60	(x2E)
XSA7	XS77	XS76	XS75	XS74	XS73	XS72	XS71	XS70	(x2F)
XSA8	XS87	XS86	XS85	XS84	XS83	XS82	XS81	XS80	(x30)

XS **Transmit S_a-Bit Data**

The S_a-bit register access is enabled by setting bit FMR1.ENSA = 1. With the transmit multiframe begin an interrupt ISR1.XMB is generated and the contents of these registers XSA(8:4) is copied into a shadow register. The contents is subsequently sent out in the service words of the next outgoing CRC multiframe (or doubleframes) if none of the time slot 0 transparent modes is enabled. XS40 is sent out in bit position 4 in frame 1, XS47 in frame 15. The transmit multiframe begin interrupt XMB request that these registers should be serviced. If requests for new information are ignored, current contents is repeated.

Framer Mode Register 3 (Read/Write)

Value after reset: 00_H

	7							0	
FMR3			XLD	XLU	CMI	SA6SY		EXTIW	(x31)

XLD **Transmit LLB Down Code**

0 Normal operation.

1 A one in this bit position causes the transmitter to replace normal transmit data with the LLB down (deactivate) Code continuously until this bit is reset. The LLB down Code is optionally overwritten by the time slot 0 depending on bit LCR1.FLLB.

XLU **Transmit LLB UP Code**

0 Normal operation.

1 A one in this bit position causes the transmitter to replace normal transmit data with the LLB UP Code continuously until this bit is reset. The LLB UP Code is overwritten by the time slot 0 depending on bit LCR1.FLLB. For proper operation bit FMR3.XLD must be cleared.

CMI **Select CMI Precoding**

Only valid if CMI code (FMR0.XC1/0 = 01) is selected. This bit defines
the CMI precoding and influences transmit and receive data.

0 CMI with HDB3 precoding

1 CMI without HDB3 precoding

Note: Before local loop is selected, HDB3 precoding has to be disabled.

SA6SY **Receive S_a6-Access Synchronous Mode**

Only valid if multiframe format (FMR2.RFS1/0 = 1x) is selected.

0 The detection of the predefined S_a6-bit pattern (refer to chapter S_a6-bit detection according to ETS 300233) is done independently of the multiframe synchronous state.

1 The detection of the S_a6-bit pattern is done synchronously to the multiframe.

EXTIW **Extended CRC4 to Non-CRC4 Interworking**

Only valid in multiframe format. This bit selects the reaction of the synchronizer after the 400 ms time-out has been elapsed and starts transmitting a remote alarm if FMR2.AXRA is set.

0 The CRC4 to Non CRC4 interworking is done as described in ITU-T G. 706 Annex B.

1 The interworking is done according to ITU-T G. 706 with the exception that the synchronizer still searches the multiframing even if the 400 ms timer is expired. Switching into doubleframe format is disabled. If FMR2.AXRA is set the remote alarm bit is active in the outgoing data stream until the multiframe is found.

Idle Channel Register (Read/Write)

Value after reset: 00_H, 00_H, 00_H, 00_H

	7							0	
ICB1	IC0	IC1	IC2	IC3	IC4	IC5	IC6	IC7	(x32)
ICB2	IC8	IC9	IC10	IC11	IC12	IC13	IC14	IC15	(x33)
ICB3	IC16	IC17	IC18	IC19	IC20	IC21	IC22	IC23	(x34)
ICB4	IC24	IC25	IC26	IC27	IC28	IC29	IC30	IC31	(x35)

IC(31:0) **Idle Channel Selection Bits**

These bits define the channels (time slots) of the outgoing PCM frame to be altered.
Assignments:
IC0 → time slot 0
IC1 → time slot 1
...
IC31 → time slot 31

0 Normal operation.

1 Idle channel mode. The contents of the selected time slot is overwritten by the idle channel code defined by register IDLE.

Note: Although time slot 0 can be selected by bit IC0, its contents is only altered if the transparent mode is selected (XSP.TT0).

Line Interface Mode 0 (Read/Write)

Value after reset: 00_H

	7							0	
LIM0	XFB	XDOS			EQON	RLM	LL	MAS	(x36)

XFB **Transmit Full Bauded Mode**

Only applicable for dual rail mode (bit LIM1.DRS = 1).

0 Output signals XDOP/XDON are half bauded.

1 Output signals XDOP/XDON are full bauded.

Note: If CMI coding is selected (FMR0.XC1/0 = 01) this bit has to be cleared.

XDOS **Transmit Data Out Sense**

0 Output signals XDOP/XDON are active low. Output XOID is active high (normal operation).

1 Output signals XDOP/XDON are active high. Output XOID is active low.

Note: If CMI coding is selected (FMR0.XC1/0 = 01) this bit has to be cleared.
The transmit frame marker XFM is independent of this bit.

EQON **Receive Equalizer On**

0 -10 dB Receiver: short haul mode

1 -43 dB Receiver, long haul mode

Note: By setting EQON = 1 the QuadFALC is able to adjust short haul or long haul mode automatically. After changing the EQON value a receiver reset is required (CMDR.RRES). Please note sequence as specified in **Table 49** *on* **Page 195**.

Note: When using EQON = 1 together with RLM = 1, LIM1.RIL(2:0) has to be set to 001_B.

RLM **Receive Line Monitoring**

0 normal receiver mode

1 receiver mode for receive line monitoring;
the receiver sensitivity is increased to detect resistively attenuated signals of -20 dB (short haul mode only)

Note: When using EQON = 1 together with RLM = 1, LIM1.RIL(2:0) has to be set to 001_B.

LL **Local Loop**

0 Normal operation

1 Local loop active. The local loopback mode disconnects the receive lines RL1/RL2 or RDIP/RDIN from the receiver. Instead of the signals coming from the line the data provided by system interface are routed through the analog receiver back to the system interface. The unipolar bit stream is transmitted undisturbedly on the line. Receiver and transmitter coding must be identical. Operates in analog and digital line interface mode. In analog line interface mode data is transferred through the complete analog receiver.

MAS **Master Mode**

0 Slave mode

1 Master mode on. Setting this bit the DCO-R circuitry is frequency synchronized to the clock (2.048 MHz or 8 kHz, see IPC.SSYF) supplied by SYNC. If this pin is connected to V_{SS} or V_{DD} (or left open and pulled up to V_{DD} internally) the DCO-R circuitry is centered and no receive jitter attenuation is performed (only if 2.048 MHz clock is selected). The generated clocks are stable.

Line Interface Mode 1 (Read/Write)

Value after reset: 00_H

	7							0	
LIM1	CLOS	RIL2	RIL1	RIL0		JATT	RL	DRS	(x37)

CLOS **Clear data in case of LOS**

0 normal receiver mode, receive data stream is transferred normally

1 received data is cleared (driven to low level), as soon as LOS is detected

RIL(2:0) **Receive Input Threshold**

Only valid if analog line interface is selected (LIM1.DRS = 0).

“No signal” is declared if the voltage between pins RL1 and RL2 drops below the limits programmed by bits RIL(2:0) and the received data stream has no transition for a period defined in the PCD register.

The threshold where “no signal” is declared is programmable by the RIL(2:0) bits depending on bit LIM0.EQON.

Note: LIM1.RIL(2:0) must be programmed before LIM0.EQON = 1 is set.

See DC characteristics for detail.

JATT, RL **Remote Loop Transmit Jitter Attenuator**

00 = Normal operation. The remote loop transmit jitter attenuator is disabled. Transmit data bypasses the remote loop jitter attenuator buffer.

01 = Remote loop active without remote loop transmit jitter attenuator enabled. Transmit data bypasses the remote loop jitter attenuator buffer.

10 = not defined

11 = Remote loop and remote loop jitter attenuator active. Received data from pins RL1/2 or RDIP/N or ROID is sent “jitter-free” on ports XL1/2 or XDOP/N or XOID. The de-jittered clock is generated by the DCO-X circuitry.

Note: JATT is only used to define the jitter attenuation during remote loop operation. Jitter attenuation during normal operation is not affected.

DRS **Dual Rail Select**

0 The ternary interface is selected. Multifunction ports RL1/2 and XL1/2 become analog in/outputs.

1 The digital dual rail interface is selected. Received data is latched on multifunction ports RDIP/RDIN while transmit data is output on pins XDOP/XDON.

Note: LIM0.EQON must be set to 0 when DRS = 1

Pulse Count Detection Register (Read/Write)

Value after reset: 00_H

	7		0	
PCD	PCD7		PCD0	(x38)

PCD(7:0) **Pulse Count Detection**

A LOS alarm is detected if the incoming data stream has no transitions for a programmable number T consecutive pulse positions. The number T is programmable by the PCD register and can be calculated as follows:
$T = 16 \times (N+1)$; with $0 \leq N \leq 255$.

The maximum time is: $256 \times 16 \times 488$ ns = 2 ms. Every detected pulse resets the internal pulse counter. The counter is clocked with the receive clock RCLK.

Pulse Count Recovery (Read/Write)

Value after reset: 00_H

	7							0	
PCR	PCR7							PCR0	(x39)

PCR(7:0) **Pulse Count Recovery**

A LOS alarm is cleared if a pulse density is detected in the received bit stream. The number of pulses M which must occur in the predefined PCD time interval is programmable by the PCR register and can be calculated as follows:

M = N+1; with $0 \leq N \leq 255$.

The time interval starts with the first detected pulse transition. With every received pulse a counter is incremented and the actual counter is compared to the contents of PCR register. If the pulse number is higher or equal to the PCR value the LOS alarm is reset otherwise the alarm stays active. In this case the next detected pulse transition starts a new time interval.

Line Interface Mode 2 (Read/Write)

Value after reset: 20_H

	7							0	
LIM2			SLT1	SLT0	SCF	ELT			(x3A)

SLT(1:0) **Receive Slicer Threshold**

00 The receive slicer generates a mark (digital one) if the voltage at RL1/2 exceeds 55% of the peak amplitude.

01 The receive slicer generates a mark (digital one) if the voltage at RL1/2 exceeds 67% of the peak amplitude (recommended in some T1/J1 applications).

10 The receive slicer generates a mark (digital one) if the voltage at RL1/2 exceeds 50% of the peak amplitude (default, recommended in E1 mode).

11 The receive slicer generates a mark (digital one) if the voltage at RL1/2 exceeds 45% of the peak amplitude.

SCF **Select Corner Frequency of DCO-R**

Setting this bit reduces the corner frequency of the DCO-R circuit by the factor of ten to 0.2 Hz.

Note: Reducing the corner frequency of the DCO-R circuitry increases the synchronization time before the frequencies are synchronized.

ELT **Enable Loop-Timed**

0 normal operation

1 Transmit clock is generated from the clock supplied by MCLK which is synchronized to the extracted receive route clock. In this configuration the transmit elastic buffer has to be enabled. Refer to register XSW.XTM. For correct operation of loop timed the remote loop (bit LIM1.RL = 0) must be inactive and bit CMR1.DXSS must be cleared.

Loop Code Register 1 (Read/Write)

Value after reset: 00_H

	7							0	
LCR1	EPRM	XPRBS	LDC1	LDC0	LAC1	LAC0	FLLB	LLBP	(x3B)

EPRM **Enable Pseudo Random Bit Sequence Monitor**

0 Pseudo random bit sequence (PRBS) monitor is disabled.

1 PRBS is enabled. Setting this bit enables incrementing the CEC2 error counter with each detected PRBS bit error. With any change of state of the PRBS internal synchronization status an interrupt ISR1.LLBSC is generated. The current status of the PRBS synchronizer is indicated by bit RSP.LLBAD.

XPRBS **Transmit Pseudo Random Bit Sequence**

A one in this bit position enables transmission of a pseudo random bit sequence to the remote end. Depending on bit LLBP the PRBS is generated according to 2^{15}-1 or 2^{20}-1 with a maximum-14-zero restriction (ITU-T O. 151).

LDC(1:0) **Length Deactivate (Down) Code**

These bits defines the length of the LLB deactivate code which is programmable in register LCR2.

00 length: 5 bit

01 length: 6 bit, 2 bit, 3 bit

10 length: 7 bit

11 length: 8 bit, 2 bit, 4bit

LAC(1:0) **Length Activate (Up) Code**

These bits defines the length of the LLB activate code which is programmable in register LCR3.

00 length: 5 bit

01 length: 6 bit, 2 bit, 3 bit

10 length: 7 bit

11 length: 8 bit, 2 bit, 4 bit

FLLB **Framed Line Loopback/Invert PRBS**

Depending on bit LCR1.XPRBS this bit enables different functions:

LCR1.XPRBS = 0:

0 The line loopback code is transmitted including framing bits. LLB code overwrites the FS/DL-bits.

1 The line loopback code is transmitted unframed. LLB code does not overwrite the FS/DL-bits.

Invert PRBS

LCR1.XPRBS = 1:

0 The generated PRBS is transmitted not inverted.

1 The PRBS is transmitted inverted.

LLBP **Line Loopback Pattern**

LCR1.XPRBS = 0

0 Fixed line loopback code according to ANSI T1. 403.

1 Enable user programmable line loopback code by register LCR2/3.

LCR1.XPRBS = 1 or LCR1.EPRM = 1

0 2^{15} -1

1 2^{20} -1

Loop Code Register 2 (Read/Write)

Value after reset: 00_H

	7						0	
LCR2	LDC7						LDC0	(x3C)

LDC(7:0) **Line Loopback Deactivate Code**

If enabled by bit FMR3.XLD = 1 the LLB deactivate code automatically repeats until the LLB generator is stopped. Transmit data is overwritten by the LLB code. LDC0 is transmitted last. For correct operations bit LCR1.XPRBS has to cleared.

If LCR2 is changed while the previous deactivate code has been detected and is still received, bit RSP.LLBDD will stay active until the incoming signal changes or a receiver reset is initiated (CMDR.RRES = 1).

Loop Code Register 3 (Read/Write)

Value after reset: 00_H

	7						0	
LCR3	LAC7						LAC0	(x3D)

LAC(7:0) **Line Loopback Activate Code**

If enabled by bit FMR3.XLU = 1 the LLB activate code automatically repeats until the LLB generator is stopped. Transmit data is overwritten by the LLB code. LAC0 is transmitted last. For correct operations bit LCR1.XPRBS has to cleared.

If LCR3 is changed while the previous activate code has been detected and is still received, bit RSP.LLBAD will stay active until the incoming signal changes or a receiver reset is initiated (CMDR.RRES = 1).

System Interface Control 1 (Read/Write)

Value after reset: 00_H

	7							0	
SIC1	SSC1	SSD1	RBS1	RBS0	SSC0	BIM	XBS1	XBS0	(x3E)

SSC(1:0) **Select System Clock**

SIC1.SSC1/0 define the clocking rate on the system highway.

00 2.048 MHz

01 4.096 MHz

10 8.192 MHz

11 16.384 MHz

SSD1 **Select System Data Rate 1**

SIC1.SSD1 and FMR1.SSD0 define the data rate on the system highway. Programming SSD1/SSD0 and corresponding data rate is shown below.

00 2.048 Mbit/s

01 4.096 Mbit/s

10 8.192 Mbit/s

11 16.384 Mbit/s

RBS(1:0) **Receive Buffer Size**

00 buffer size: 2 frames

01 buffer size: 1 frame

10 buffer size: 96 bits

11 bypass of receive elastic store

BIM **Bit Interleaved Mode**

0 byte interleaved mode

1 bit interleaved mode

XBS(1:0) **Transmit Buffer Size**

00 bypass of transmit elastic store

01 buffer size: 1 frame

10 buffer size: 2 frames

11 buffer size: 96 bits

System Interface Control 2 (Read/Write)

Value after reset: 00_H

	7							0	
SIC2	FFS	SSF	CRB		SICS2	SICS1	SICS0		(x3F)

FFS **Force Freeze Signaling**

Setting this bit disables updating of the receive signaling buffer and current signaling information is frozen. After resetting this bit and receiving a complete superframe updating of the signaling buffer is started again. The freeze signaling status can also be automatically generated by detecting the loss of signal alarm or a loss of CAS frame alignment or a receive slip (only if external register access on pin RSIG is enabled). This automatic freeze signaling function is logically ored with this bit.
The current internal freeze signaling status is output on pin RP(A to D)/pin function FREEZE which is selected by PC(4:1).RPC(2:0) = 110. Additionally this status is also available in register SIS.SFS.

SSF **Serial Signaling Format**

Only applicable if pin function RSIG/XSIG and SIC3.TTRF = 0 is selected.

0 Bits (4:1) in all time slots except time slots 0 and16 are cleared.

1 Bits (4:1) in all time slots except time slots 0 and16 are set high.

CRB **Center Receive Elastic Buffer**

Only applicable if the time slot assigner is disabled (PC(4:1).RPC(2:0) = 001), no external or internal synchronous pulse receive is generated.
A transition from low to high forces a receive slip and the read- pointer of the receive elastic buffer is centered. The delay through the buffer is set to one half of the current buffer size. It should be hold high for at least two 2.048 MHz periods before it is cleared.

SICS(2:0) **System Interface Channel Select**

Only applicable if the system clock rate is greater than 2.048 MHz.

Received data is transmitted on pin RDO/RSIG or received on XDI/XSIG with the selected system data rate. If the data rate is greater than 2.048 Mbit/s the data is output or sampled in half, a quarter or one eighth of the time slot. Data is not repeated. The time while data is active during a 8×488 ns time slot is called a channel phase. RDO/RSIG are cleared (driven to low level) while XDI/XSIG are ignored for the remaining time of the 8×488 ns or for the remaining channel phases. The channel phases are selectable with these bits.

000 data active in channel phase 1, valid if system data rate is 16⁄8⁄4 Mbit/s

001 data active in channel phase 2, valid if system data rate is 16⁄8⁄4 Mbit/s

010 data active in channel phase 3, valid if data rate is 16/8 Mbit/s

011 data active in channel phase 4, valid if data rate is 16/8 Mbit/s

100 data active in channel phase 5, valid if data rate is 16 Mbit/s

101 data active in channel phase 6, valid if data rate is 16 Mbit/s

110 data active in channel phase 7, valid if data rate is 16 Mbit/s

111 data active in channel phase 8, valid if data rate is 16 Mbit/s

System Interface Control 3 (Read/Write)

Value after reset: 00_H

	7							0	
SIC3	CASMF				RESX	RESR	TTRF	DAF	(x40)

CASMF **CAS Multiframe Begin Marker**

0 The time slot 0 multiframe begin is asserted on pin RP(A to D)/ pin function RMFB.

1 The time slot 16 CAS multiframe begin is asserted on pin RP(A to D)/pin function RMFB.

RESX **Rising Edge Synchronous Pulse Transmit**

Depending on this bit all transmit system interface data and markers are clocked or sampled with the selected active edge.

CMR2.IRSC = 0 or CMR2.IRSP = 0:

0 latched with the first falling edge of the selected PCM highway clock.

1 latched with the first rising edge of the selected PCM highway clock.

CMR2.IRSC = 1 or CMR2.IRSP = 1:

0 latched with the first rising edge of the selected PCM highway clock.

1 latched with the first falling edge of the selected PCM highway clock.

RESR **Rising Edge Synchronous Pulse Receive**

Depending on this bit all receive system interface data and marker are clocked with the selected active edge.

0 latched with the first falling edge of the selected PCM highway clock.

1 latched with the first rising edge of the selected PCM highway clock.

If CMR2.IRSP = 1, the behavior is inverse:

0 latched with the first rising edge of the selected PCM highway clock.

1 latched with the first falling edge of the selected PCM highway clock.

TTRF **TTR Register Function (Fractional E1 Access)**

Setting this bit the function of the TTR(4:1) registers is changed. A one in each TTR register forces the XSIGM marker high for the corresponding time slot and controls sampling of the time slots provided on pin XSIG. XSIG is selected by PC(4:1).XPC(3:0).

DAF **Disable Automatic Freeze**

0 Signaling is automatically frozen if one of the following alarms occurred: Loss of Signal (FRS0.LOS), Loss of CAS Frame Alignment (FRS1.TS16LFA), or receive slips (ISR3.RSP/N).

1 Automatic freezing of signaling data is disabled. Updating of the signaling buffer is also done if one of the above described alarm conditions is active. However, updating of the signaling buffer is stopped if SIC2.FFS is set. Significant only if the serial signaling access is enabled.

Clock Mode Register 1 (Read/Write)

Value after reset: 00_H

	7							0	
CMR1	DRSS1	DRSS0	RS1	RS0	DCS	STF	DXJA	DXSS	(x44)

DRSS(1:0) **Select RCLK Source**

These bits select the reference clock source for the DCO-R circuit.

00 receive reference clock generated by the DPLL of channel 1

01 receive reference clock generated by the DPLL of channel 2

10 receive reference clock generated by the DPLL of channel 3

11 receive reference clock generated by the DPLL of channel 4

RS(1:0) **Select RCLK Source**

These bits select the source of RCLK.

00 clock recovered from the line through the DPLL drives RCLK

01 clock recovered from the line through the DPLL drives RCLK and in case of an active LOS alarm RCLK pin is set high.

10 clock recovered from the line is dejittered by DCO-R to drive a 2.048-MHz clock on RCLK.

11 clock recovered from the line is dejittered by DCO-R to drive a 8.192-MHz clock on RCLK.

DCS **Disable Clock Switching**

In Slave mode (LIM0.MAS = 0) the DCO-R is synchronized on the recovered route clock. In case of loss of signal LOS the DCO-R switches automatically to the clock sourced by port SYNC. Setting this bit automatic switching from RCLK to SYNC is disabled.

STF **Select TCLK Frequency**

Only applicable if the pin function TCLK port XP(A to D) is selected by PC(4:1).XPC(3:0) = 0011. Data on XL1/2 (XDOP/N / XOID) are clocked with TCLK.

0 2.048 MHz

1 8.192 MHz

DXJA **Disable Internal Transmit Jitter Attenuation**

Setting this bit disables the transmit jitter attenuation. Reading the data out of the transmit elastic buffer and transmitting on XL1/2 (XDOP/N/XOID) is done with the clock provided on pin TCLK. In transmit elastic buffer bypass mode the transmit clock is taken from SCLKX, independent of this bit.

DXSS **DCO-X Synchronization Clock Source**

0 The DCO-X circuitry synchronizes to the internal reference clock which is sourced by SCLKX/R or RCLK. Since there are many reference clock opportunities the following internal prioritizing in descending order from left to right is realized: LIM1.RL > CMR1.DXSS > LIM2.ELT > current working clock of transmit system interface.
If one of these bits is set the corresponding reference clock is taken.

1 DCO-X synchronizes to an external reference clock provided by pin XP(A to D) pin function TCLK, if no remote loop is active. TCLK is selected by PC(4:1).XPC(3:0) = 0011.

Clock Mode Register 2 (Read/Write)

Value after reset: 00_H

	7							0	
CMR2			DCOXC	DCF	IRSP	IRSC	IXSP	IXSC	(x45)

DCOXC **DCO-X Center-Frequency Enable**

0 The center function of the DCO-X circuitry is disabled.

1 The center function of the DCO-X circuitry is enabled.
DCO-X centers to 2.048 MHz related to the master clock reference (MCLK), if reference clock (e.g. SCLKX) is missing.

DCF **DCO-R Center- Frequency Disabled**

0 The DCO-R circuitry is frequency centered
- in master mode if no 2.048-MHz reference clock on pin SYNC is provided or
- in slave mode if a loss of signal occurs in combination with no 2.048-MHz clock on pin SYNC or
- a gapped clock is provided at pin RCLKI and this clock is inactive or stopped.

1 The center function of the DCO-R circuitry is disabled. The generated clock (DCO-R) is frequency frozen in that moment when no clock is available at pin SYNC or pin RCLKI. The DCO-R circuitry starts synchronization as soon as a clock appears on pins SYNC or RCLKI.

IRSP **Internal Receive System Frame Sync Pulse**

0 The frame sync pulse for the receive system interface is sourced by $\overline{\text{SYPR}}$ (if $\overline{\text{SYPR}}$ is applied). If $\overline{\text{SYPR}}$ is not applied, the frame sync pulse is derived from the RDO output signal internally (free running). The use of IRSP = 0 is recommended.

1 The frame sync pulse for the receive system interface is internally sourced by the DCO-R circuitry. This internally generated frame sync signal can be output (active low) on multi function ports RP(A to D) (RPC(2:0) = 001).

Note: This is the only exception where the use of RFM and $\overline{\text{SYPR}}$ is allowed at the same time. Because only one set of offset registers (RC1/0) is available, programming is done by using the $\overline{\text{SYPR}}$ calculation formula in the same way as for the external $\overline{\text{SYPR}}$ pulse. Bit IRSC must be set for correct operation.

IRSC **Internal Receive System Clock**

0 The working clock for the receive system interface is sourced by SCLKR or in receive elastic buffer bypass mode from the corresponding extracted receive clock RCLK.

1 The working clock for the receive system interface is sourced internally by DCO-R or in bypass mode by the extracted receive clock. SCLKR is ignored.

IXSP **Internal Transmit System Frame Sync Pulse**

0 The frame sync pulse for the transmit system interface is sourced by $\overline{\text{SYPX}}$.

1 The frame sync pulse for the transmit system interface is internally sourced by the DCO-R circuitry. Additionally, the external XMFS signal defines the transmit multiframe begin. XMFS is enabled or disabled by the multifunction port configuration. For correct operation bits CMR2.IXSC/IRSC must be set. $\overline{\text{SYPX}}$ is ignored.

IXSC **Internal Transmit System Clock**

0 The working clock for the transmit system interface is sourced by SCLKX.

1 The working clock for the transmit system interface is sourced internally by the working clock of the receive system interface. SCLKX is ignored.

Global Configuration Register (Read/Write)

Value after reset: 00_H

	7							0	
GCR	VIS	SCI	SES	ECMC				PD	(x46)

VIS **Masked Interrupts Visible**

0 Masked interrupt status bits are not visible in registers ISR(4:0).

1 Masked interrupt status bits are visible in ISR(4:0), but they are not visible in register GIS.

SCI **Status Change Interrupt**

0 Interrupts are generated either on activation or deactivation of the internal interrupt source.

1 The following interrupts are activated both on activation and deactivation of the internal interrupt source:
ISR2.LOS, ISR2.AIS, ISR3.LMFA16

SES **Select External Second Timer**

0 internal second timer selected

1 external second timer selected

ECMC **Error Counter Mode COFA**

0 The S_a6-bit error indications are accumulated in the error counter CEC3L/H.

1 A Change of Frame or Multiframe Alignment COFA is detected since the last resynchronization. The events are accumulated in the error counter CEC3L.(1:0).
Multiframe periods received in the asynchronous state are accumulated in the error counter CEC3L.7-2.
An overflow of each counter is disabled.

PD **Power Down**

Switches between power up and power down mode.

0 Power Up

1 Power Down
All outputs are driven inactive; multifunction ports are driven high by the weak internal pullup device.

Errored Second Mask (Read/Write)

Value after reset: FF_H

	7							0	
ESM	LFA	FER	CER	AIS	LOS	CVE	SLIP	EBE	(x47)

ESM **Errored Second Mask**

This register functions as an additional mask register for the interrupt status bit Errored Second (ISR3.ES). A ’1’ in a bit position of ESM deactivates the related second interrupt.

Disable Error Counter (Write)

Value after reset: 00_H

	7							0	
DEC	DRBD		DCEC3	DCEC2	DCEC1	DEBC	DCVC	DFEC	(x60)

DRBD **Disable Receive Buffer Delay**

This bit has to be set before reading the register RBD. It is reset automatically if RBD has been read.

DCEC3 **Disable CRC Error Counter 3**

DCEC2 **Disable CRC Error Counter 2**

DCEC1 **Disable CRC Error Counter**

DEBC **Disable Errored Block Counter**

DCVC **Disable Code Violation Counter**

DFEC **Disable Framing Error Counter**

These bits are only valid if FMR1.ECM is cleared. They have to be set before reading the error counters. They are reset automatically if the corresponding error counter high byte has been read. With the rising edge of these bits the error counters are latched and then cleared.

Note: Error counters and receive buffer delay can be read 1 µs after setting the according bit in bit DEC.

Transmit CAS Register (Write)

Value after reset: not defined

Table 60 Transmit CAS Registers (E1)

	7							0	
XS1	0	0	0	0	X	Y	X	X	(x70)
XS2	A1	B1	C1	D1	A16	B16	C16	D16	(x71)
XS3	A2	B2	C2	D2	A17	B17	C17	D17	(x72)
XS4	A3	B3	C3	D3	A18	B18	C18	D18	(x73)
XS5	A4	B4	C4	D4	A19	B19	C19	D19	(x74)
XS6	A5	B5	C5	D5	A20	B20	C20	D20	(x75)
XS7	A6	B6	C6	D6	A21	B21	C21	D21	(x76)
XS8	A7	B7	C7	D7	A22	B22	C22	D22	(x77)
XS9	A8	B8	C8	D8	A23	B23	C23	D23	(x78)
XS10	A9	B9	C9	D9	A24	B24	C24	D24	(x79)
XS11	A10	B10	C10	D10	A25	B25	C25	D25	(x7A)
XS12	A11	B11	C11	D11	A26	B26	C26	D26	(x7B)
XS13	A12	B12	C12	D12	A27	B27	C27	D27	(x7C)
XS14	A13	B13	C13	D13	A28	B28	C28	D28	(x7D)
XS15	A14	B14	C14	D14	A29	B29	C29	D29	(x7E)
XS16	A15	B15	C15	D15	A30	B30	C30	D30	(x7F)

Transmit CAS Register (16:1)

The transmit CAS register access is enabled by setting bit XSP.CASEN = 1. Each register except XS1 contains the CAS bits for two time slots. With the transmit multiframe begin ISR1.XMB the contents of these registers is copied into a shadow register. The contents is sent out subsequently in the time slots 16 of the outgoing data stream.

Note: If ISR1.XMB is not used and the write access to these registers is done exact in the moment when this interrupt is generated, data is lost.

XS1.7 is sent out first and XS16.0 is sent last. The transmit multiframe begin interrupt (XMB) requests that these registers should be serviced. If requests for new information are ignored, current contents is repeated. XS1 has to be programmed with the multiframe pattern. This pattern should always stay low otherwise the remote end loses its synchronization. With setting the Y-bit a remote alarm is transmitted to the far end. The X bits (spare bits) should be set if they are not used.

If access to these registers is done without control of the interrupt ISR1.XMB the registers should be written twice to avoid an internal data transfer error.

Note: A software reset (CMDR.XRES) resets these registers.

Port Configuration (4:1) (Read/Write)

Value after reset: 00_H

	7							0	
PC1		RPC12	RPC11	RPC10	XPC13	XPC12	XPC11	XPC10	(x80)
PC2		RPC22	RPC21	RPC20	XPC23	XPC22	XPC21	XPC20	(x81)
PC3		RPC32	RPC31	RPC30	XPC33	XPC32	XPC31	XPC30	(x82)
PC4		RPC42	RPC41	RPC40	XPC43	XPC42	XPC41	XPC40	(x83)

RPC(2:0) **Receive multifunction port configuration**

The multifunction ports RP(A to D) are bidirectional. After Reset these ports are configured as inputs. With the selection of the pin function the In/Output configuration is also achieved. The input function $\overline{\text{SYPR}}$ may only be selected once, it must not be selected twice or more. Register PC1 configures port RPA, while PC2 → port RPB,
PC3 → port RPC and PC4 → port RPD.

000 $\overline{\text{SYPR}}$: Synchronous Pulse Receive (Input)
Together with register RC1/0 $\overline{\text{SYPR}}$ defines the frame begin on the receive system interface. Because of the offset programming the $\overline{\text{SYPR}}$ and the RFM pin function can not be selected in parallel.

001 RFM: Receive Frame Sync (Output)
CMR2.IRSP = 0: The Receive Frame Marker is active high for one 2.048-MHz period during any bit position of the current frame. Programming of the bit position is done by using registers RC1/0. The internal time slot assigner is disabled. The RFM offset calculation formula has to be used.

CMR2.IRSP = 1: Internally generated frame synchronization pulse sourced by the DCO-R circuitry. The pulse is active low for one 2.048-MHz period.

010 RMFB: Receive Multiframe Begin (Output)
Marks the beginning of every received multiframe or optionally the begin of every CAS multiframe begin (active high).

011 RSIGM: Receive Signaling Marker (Output)
Marks the time slots which are defined by register RTR(4:1) of every frame at port RDO.

100 RSIG: Receive Signaling Data (Output)
The received CAS multiframe is transmitted on this pin. Time Slots on RSIG correlates directly to the time slot assignment on RDO. In system interface multiplex mode all four received signaling data streams are merged into a single rail data stream byte or bit interleaved on RSIG1.

101 DLR: Data Link Bit Receive (Output)
Marks the S_a8...4-bits within the data stream on RDO.

110 FREEZE: Freeze Signaling (Output)
The freeze signaling status is active high by detecting a loss of signal alarm, or a loss of CAS frame alignment or a receive slip (positive or negative). It stays high for at least one complete multiframe after the alarm disappears. Setting SIC2.FFS enforces a high on pin FREEZE.

111 $\overline{\text{RFSP}}$: Receive Frame Synchronous Pulse (Output)
Marks the frame begin in the receivers synchronous state. This marker is active low for 488 ns with a frequency of 8 kHz.

XPC(3:0) Transmit multifunction Port Configuration

The multifunction ports XP(A to D) are bidirectional. After Reset these ports are configured as inputs. With the selection of the pin function the In/Output configuration is also achieved. Each of the four different input functions ($\overline{\text{SYPX}}$, XMFS, XSIG, TCLK) may only be selected once. No input function must be selected twice or more. $\overline{\text{SYPX}}$ and XMFS should not be selected in parallel. Register PC1 configures port XPA, while PC2 → port XPB, PC3 → port XPC and PC4 → port XPD.

0000 $\overline{\text{SYPX}}$: Synchronous Pulse Transmit (Input)
Together with register XC1/0 $\overline{\text{SYPX}}$ defines the frame begin on the transmit system interface ports XDI and XSIG.

0001 XMFS: Transmit Multiframe Synchronization (Input)
Together with register XC1/0 XMFS defines the frame and multiframe begin on the transmit system interface ports XDI and XSIG. Depending on PC5.CXMFS the signal on XMFS is active high or low.

0010 XSIG: Transmit Signaling Data (Input)
Input for transmit signaling data received from the signaling highway. In system interface multiplex mode latching of the data stream containing the 4 signaling multiframes is done byte or bit interleaved on port XDI1. Optionally sampling of XSIG data is controlled by the active high XSIGM marker.

0011 TCLK: Transmit Clock (Input)
A 2.048/8.192 MHz clock has to be sourced by the system if the internal generated transmit clock (DCO-X) is not used. Optionally this input is used as a synchronization clock for the DCO-X circuitry with a frequency of 2.048 MHz.

0100 XMFB: Transmit Multiframe Begin (Output)
Marks the beginning of every transmit multiframe.

0101 XSIGM: Transmit Signaling Marker (Output)
Marks the time slots which are defined by register TTR(4:1) of every frame at port XDI.

0110 DLX: Data Link Bit Transmit (Output)
Marks the S_a8...4-bits within the data stream on XDI.

0111 XCLK: Transmit Line Clock (Output)
Frequency: 2.048 MHz

1000 XLT: Transmit Line Tristate (Input)
With a high level on this port the transmit lines XL1/2 or XDOP/N are set directly into tristate. This pin function is logically ored with register XPM2.XLT.

Port Configuration 5 (Read/Write)

Value after reset: 00_H

	7							0	
PC5					CXMFS	CSXP	CSRP	CRP	(x84)

CXMFS **Configure XMFS Port**

0 Port XMFS is active low.

1 Port XMFS is active high.

CSXP **Configure SCLKX Port**

0 SCLKX: Input

1 SCLKX: Output

Note: Must be cleared because no output function is defined.

CSRP **Configure SCLKR Port**

0 SCLKR: Input

1 SCLKR: Output

CRP **Configure RCLK Port**

0 RCLK: Input

1 RCLK: Output

Global Port Configuration 1 (Read/Write)

Value after reset: 00_H

	7							0	
GPC1	SMM	CSFP1	CSFP0		FSS1	FSS0	R1S1	R1S0	(85)

SMM **System Interface Multiplex Mode**

Setting this bit enables a single data stream of 16.384 or 8.192 Mbit/s containing all the E1 frames of all four channels.

0 System multiplex mode disabled

1 System multiplex mode enabled

The receive system interface for all four channels is running with the clock provided on SCLKR1 and the frame sync pulse provided on $\overline{\text{SYPR1}}$. The transmit system interface is running with SCLKX1 and $\overline{\text{SYPX1}}$. Data will be transmitted/accepted in a byte or bit interleaved format. In the system interface multiplex mode the following pin configuration has to be fulfilled and **must be identical for all for 4 channels**:

- $\overline{\text{SYPR1}}$ has to be provided on pin RPA1
- $\overline{\text{SYPX1}}$ has to be provided on pin XPA1 or
- XMFS has to be provided on pin XPB1
- XSIG has to be provided on pin XPC1
- RSIG will be output on pin RPB1

Each of the four channels have to be configured equally:

- clocking rate : 16.384 or 8.192 MHz, SIC1.SSC1/0
- data rate : 16.384 or 8.192 Mbit/s, SIC1.SSD, FMR1.SSD0
- time-slot offset programming : RC1/0, XC1/0
- receive buffer size : SIC1.RBS1/0 = 00 (2 frames)

e.g.: system clock rate = 8.192 MHz: SIC1.SSC1/0 = 10 and system data rate = 8.192 Mbit/s: SIC1.SSD1 = 1, FMR1.SSD0 = 0

The multiplexed data stream is internal logically ored. Therefore the selection of the active channel phase have to be configured different for each single channel (4:1). Programming is done with SIC2.SICS(2:0).
for channel 1: SIC2.SICS(2:0) = 000, selects the first channel phase
for channel 2: SIC2.SICS(2:0) = 001, selects the second channel phase
for channel 3: SIC2.SICS(2:0) = 010, selects the third channel phase
for channel 4: SIC2.SICS(2:0) = 011, selects the fourth channel phase

byte interleaved data format: SIC1.BIM = 0

XDI/RDO: F1-TS0, F2-TS0, F3-TS0, F4-TS0, F1-TS1,... F4-TS31

X/RSIG: F1-STS0, F2-STS0, F3-STS0, F4-STS0, F1-... F4-STS31

or : bit interleaved data format: SIC1.BIM = 1

XDI/RDO: F1-TS0-B1, F2-TS0-B1, F3-TS0-B1, F4-TS0-B1, F1-TS0-B2,... F4-TS31-B8

X/RSIG: F1-STS0-B1, F2-STS0-B1, F3-STS0-B1, F4-STS0-B1, F1-STS0-B2,... F4-STS31-B8

with : F = Framer, TS = Time-Slot, STS = Signaling Time-Slot, B = Bit

In system interface multiplex mode signals on RDO(4:2) and RSIG(4:2) are undefined, while signals on SCLKR(4:2), $\overline{\text{SYPR}}$(4:2), SCLKX(4:2), $\overline{\text{SYPX}}$(4:2), XDI(4:2) and XSIG(4:2) are ignored.

CSFP(1:0) **Configure SEC/FSC Port**

The FSC pulse is generated if the DCO-R circuitry of the selected channel is active (CMR2.IRSC = 1 or CMR1.RS1/0 = 10 or 11).

00 SEC: Input, active high

01 SEC: Output, active high

10 FSC: Output, active high

11 FSC: Output, active low

FSS(1:0) **SEC/FSC Source**

One of the four internally generated dejittered 8-kHz clocks or second timers are output on pin SEC/FSC.

GPC1.CSFP1 = 1:

00 FSC: 8 kHz sourced by channel 1

01 FSC: 8 kHz sourced by channel 2

10 FSC: 8 kHz sourced by channel 3

11 FSC: 8 kHz sourced by channel 4

GPC1.CSFP1 = 0:

00 SEC: second timer sourced by channel 1

01 SEC: second timer sourced by channel 2

10 SEC: second timer sourced by channel 3

11 SEC: second timer sourced by channel 4

R1S(1:0) **RCLK Source**

One of the four internally generated receive route clocks is output on pin RCLK1. Outputs RCLK(4:2) are valid independent of these bits. Refer also to CMR1.RS(1:0).

00 extracted receive clock of channel 1

01 extracted receive clock of channel 2

10 extracted receive clock of channel 3

11 extracted receive clock of channel 4

Command Register 2 (Write)

Value after reset: 00_H

CMDR2							RSUC		(x87)

RSUC **Reset Signaling Unit Counter**

1 After setting this bit the SS7 signaling unit counter and error counter are reset.The bit is cleared automatically after execution.

Note: The maximum time between writing to the CMDR2 register and the execution of the command takes 2.5 periods of the current system data rate. Therefore, if the CPU operates with a very high clock rate in comparison with the QuadFALC's clock, it is recommended that bit SIS.CEC should be checked before writing to the CMDR2 register to avoid any loss of commands.

Common Configuration Register 5 (Read/Write)

Value after reset: 00_H

	7							0	
CCR5		CSF2	SUET	CSF	AFX				(x8D)

Note: These bits are only valid, if SS7 mode is selected.

CSF2 **Compare Status Field - Mode 2**
If the status fields of consecutive LSSUs are equal, only the first is stored and every following is ignored.
Exception: if identical FISUs are received, *two* of them are stored,

0 Compare disabled.

1 Compare enabled.

SUET **Signaling Unit Error Threshold**
Defines the number of signaling units received in error that will cause an error rate high indication (ISR1.SUEX).

0 threshold 64 errored signaling units

1 threshold 32 errored signaling units

CSF **Compare Status Field**
If the status fields of consecutive LSSUs are equal, only the first is stored and every following is ignored.

0 Compare disabled.

1 Compare enabled.

AFX **Automatic FISU Transmission**
After the contents of the transmit FIFO (XFIFO) has been transmitted completely, FISUs are transmitted automatically. These FISUs contain the FSN and BSO of the last transmitted signaling unit (provided in XFIFO).

0 Automatic FISU transmission disabled.

1 Automatic FISU transmission enabled.

Global Clock Mode Register 1 (Read/Write)

Value after reset: 00_H

	7							0	
GCM1	PHD_E17	PHD_E16	PHD_E15	PHD_E14	PHD_E13	PHD_E12	PHD_E11	PHD_E10	(92)

PHD_E1(7:0) **Frequency Adjust for E1**

For details see calculation formulas below.

Global Clock Mode Register 2 (Read/Write)

Value after reset: 00_H

	7							0	
GCM2	0	0	0	1	PHD_E111	PHD_E110	PHD_E19	PHD_E18	(93)

PHD_E1(8:11) **Frequency Adjust for E1**

For details see calculation formulas below.

GCM2.(7:5) reserved

Must be cleared.

GCM2.(4) reserved

Must be set to 1.

Global Clock Mode Register 3 (Read/Write)

Value after reset: 00_H

	7							0	
GCM3	PHD_T17	PHD_T16	PHD_T15	PHD_T14	PHD_T13	PHD_T12	PHD_T11	PHD_T10	(94)

PHD_T1(7:0) **Frequency Adjust for T1**

For details see calculation formulas below.

Global Clock Mode Register 4 (Read/Write)

Value after reset: 00_H

	7							0	
GCM4	0	0	0	0	PHD_T1 11	PHD_T1 10	PHD_T1 9	PHD_T1 8	(95)

PHD_T1(8:11) **Frequency Adjust for T1**

For details see calculation formulas below.

GCM4.(7:4) reserved

Must be cleared.

Global Clock Mode Register 5 (Read/Write)

Value after reset: 00_H

	7							0	
GCM5	0	0	0	PLL_M 4	PLL_M 3	PLL_M 2	PLL_M 1	PLL_M 0	(96)

PLL_M(4:0) **PLL Dividing Factor M**

For details see calculation formulas below.

GCM5.(7:5) reserved

Must be cleared.

Note: Write operations to GCM5 initiate a PLL reset (see below).

Global Clock Mode Register 6 (Read/Write)

Value after reset: 00_H

	7							0	
GCM6	0	0	PLL_N 5	PLL_N 4	PLL_N 3	PLL_N 2	PLL_N 1	PLL_N 0	(97)

PLL_N(5:0) **PLL Dividing Factor N**

For details see calculation formulas below.

GCM6.(7:6) reserved

Must be cleared.

Note: Write operations to GCM6 initiate a PLL reset (see below).

Global Clock Mode Register 7 (Read/Write)

Value after reset: 00_H

	7							0	
GCM7	1	PHSX_ E12	PHSX_ E11	PHSX_ E10	PHSN_ E13	PHSN_ E12	PHSN_ E11	PHSN_ E10	(98)

GCM7.7 reserved

Must be set to 1.

PHSX_E1(2:0) Frequency adjustment value E1

PHSN_E1(3:0) Frequency adjustment value E1

Global Clock Mode Register 8 (Read/Write)

Value after reset: 00_H

	7							0	
GCM8	1	PHSX_ T12	PHSX_ T11	PHSX_ T10	PHSN_ T13	PHSN_ T12	PHSN_ T11	PHSN_ T10	(99)

GCM8.7 reserved

Must be set to 1.

PHSX_T1(2:0) Frequency adjustment value T1/J1

PHSN_T1(3:0) Frequency adjustment value T1/J1

Flexible Clock Mode Settings

The register settings for flexible master clock can be calculated as follows. For some standard frequencies see **Table 61** below. The variables used in these calculations are located in registers GCM1 to GCM8.

To support the necessary calculations, an easy-to-use PC tool is available for free (see **Chapter 13.3** on page **457** for details).

1. PLL_M and PLL_N must fulfill the equations:

a.

for PLL_M = 0 to 31:

$$f_{pdref} = \frac{f_{MCLK}}{PLL\_M + 1}$$

b.

for PLL_N = 25 to 63:

$$1.0\ MHz \leq f_{pdref} \leq 6.0\ MHz$$

for PLL_N = 0 to 24:

$$5.0\ MHz \leq f_{pdref} \leq 15.0\ MHz$$

Attention: To achieve optimum performance it is recommended to adjust f_{pdref} as high as possible.

c.

$$260\ MHz \leq f_{MCLK} \times \frac{4 \times (PLL\_N + 1)}{PLL\_M + 1} \leq\ 395.26\ MHz$$

(as high as possible within this range)

2. Selection of the dividing mode to best fulfill:

$$f_{outE1} = f_{MCLK} \times \frac{4 \times (PLL\_N + 1)}{\left(PHSN\_E1 + \frac{PHSX\_E1}{6}\right) \times (PLL\_M + 1)} \cong 2 \times 16.384\ MHz$$

$$f_{outT1} = f_{MCLK} \times \frac{4 \times (PLL\_N + 1)}{\left(PHSN\_T1 + \frac{PHSX\_T1}{6}\right) \times (PLL\_M + 1)} \cong 2 \times 12.352\ MHz$$

Though the target frequency might not be met directly, the dividing mode has to be selected to reach a frequency which is as near as possible to the target frequency.

PHSN_E1, PHSN_T1: 1 to 15; PHSX_E1, PHSX_T1: 0 to 5

3. Calculation of the correction value for frequency mismatch correction:

$$PHD\_E1 = 12288 \times \left[\left(PHSN\_E1 + \frac{PHSX\_E1}{6}\right) - \frac{4 \times (PLL\_N + 1)}{PLL\_M + 1} \times \frac{f_{MCLK}}{2 \times 16.384\ MHz}\right]$$

$$PHD\_T1 = 12288 \times \left[\left(PHSN\_T1 + \frac{PHSX\_T1}{6}\right) - \frac{4 \times (PLL\_N + 1)}{PLL\_M + 1} \times \frac{f_{MCLK}}{2 \times 12.352\ MHz}\right]$$

The result of these equations will be in the range of -2048...+2047. Negative values are represented in 2s-complement format (e.g., $-2000_D = 830_H$; $+2000_D = 7D0_H$).

To achieve optimal QuadFALC performance values < -1023 and > +1023 has to be applied. Negative values are favored.

Table 61 Clock Mode Register Settings for E1 and T1/J1

f_{MCLK}[MHz]	GCM1	GCM2	GCM3	GCM4	GCM5	GCM6	GCM7	GCM8
1.544	F0	19	00	08	00	2B	98	DA
2.048	00	18	D2	0A	00	21	A8	9B
8.192	00	18	D2	0A	03	21	A8	9B
10.000	DD	1A	3B	09	08	3C	98	DA
12.352	11	18	E9	0A	0A	3D	A8	9B
16.384	00	18	D2	0A	07	21	A8	9B

Note: All values given in hexadecimal notation.

Time Slot Even/Odd Select (Read/Write)

Value after reset: 00_H

	7							0	
TSEO							EO11	EO10	(xA0)

HDLC protocol data can be sent in even, odd or both frames of a multiframe. Even frames are frame number 2, 4,..., odd frames are frame number 1, 3,... . The selection refers to receive and transmit direction as well. Each multiframe starts with an odd frame and ends with an even frame. By default all frames are used for HDLC reception and transmission.

EO1(1:0) **Even/Odd frame selection HDLC Channel 1**
Channel 1 HDLC protocol data can be sent in even, odd or both frames of a multiframe.

00 even and odd frames

01 odd frames only

10 even frames only

11 undefined

Time Slot Bit Select 1 (Read/Write)

Value after reset: FF_H

	7							0	
TSBS1	TSB17	TSB16	TSB15	TSB14	TSB13	TSB12	TSB11	TSB10	(xA1)

TSB1(7:0) **Time Slot Bit Selection**
Only bits selected by this register are used for HDLC channel 1 in selected time slots. Time slot selection is done by setting the appropriate bits in registers TTR(4:1) and RTR(4:1) independently for receive and transmit direction. Bit selection is common to receive and transmit direction. By default all bit positions within the selected time slot(s) are enabled.

TSB1x = 0 bit position x in selected time slot(s) is not used for HDLC channel 1 reception and transmission.

TSB1x = 1 bit position x in selected time slot(s) is used for HDLC channel 1 reception and transmission.

Test Pattern Control Register 0 (Read/Write)

Value after reset: 00_H

	7							0	
TPC0		FRA							(xA8)

FRA **Framed/Unframed Selection**

0 PRBS is generated/monitored unframed.

Framing information is overwritten by the generator.

1 PRBS is generated/monitored framed.

Time slot 0 is not overwritten by the generator and not observed by the monitor.

9.3 E1 Status Register Addresses

Table 62 E1 Status Register Address Arrangement

Address[1)]	Register	Type	Comment	Page
x00	RFIFO	R	Receive FIFO	285
x01	RFIFO	R	Receive FIFO	285
x49	RBD	R	Receive Buffer Delay	285
4A	VSTR	R	Version Status Register	286
x4B	RES	R	Receive Equalizer Status	286
x4C	FRS0	R	Framer Receive Status 0	287
x4D	FRS1	R	Framer Receive Status 1	291
x4E	RSW	R	Receive Service Word	292
x4F	RSP	R	Receive Spare Bits	293
x50	FECL	R	Framing Error Counter Low	295
x51	FECH	R	Framing Error Counter High	295
x52	CVCL	R	Code Violation Counter Low	296
x53	CVCH	R	Code Violation Counter High	296
x54	CEC1L	R	CRC Error Counter 1 Low	297
x55	CEC1H	R	CRC Error Counter 1 High	297
x56	EBCL	R	E-Bit Error Counter Low	298
x57	EBCH	R	E-Bit Error Counter High	298
x58	CEC2L	R	CRC Error Counter 2 Low	299
x59	CEC2H	R	CRC Error Counter 2 High	299
x5A	CEC3L	R	CRC Error Counter 3 Low	300
x5B	CEC3H	R	CRC Error Counter 3 High	300
x5C	RSA4	R	Receive S_a4-Bit Register	301
x5D	RSA5	R	Receive S_a5-Bit Register	301
x5E	RSA6	R	Receive S_a6-Bit Register	301
x5F	RSA7	R	Receive S_a7-Bit Register	301
x60	RSA8	R	Receive S_a8-Bit Register	301
x61	RSA6S	R	Receive S_a6-Bit Status Register	302
x62	RSP1	R	Receive Signaling Pointer 1	303
x63	RSP2	R	Receive Signaling Pointer 2	303

Table 62 E1 Status Register Address Arrangement (cont'd)

Address[1)]	Register	Type	Comment	Page
x64	SIS	R	Signaling Status Register	304
x65	RSIS	R	Receive Signaling Status Register	305
x66	RBCL	R	Receive Byte Control Low	307
x67	RBCH	R	Receive Byte Control High	307
x68	ISR0	R	Interrupt Status Register 0	307
x69	ISR1	R	Interrupt Status Register 1	309
x6A	ISR2	R	Interrupt Status Register 2	311
x6B	ISR3	R	Interrupt Status Register 3	312
x6C	ISR4	R	Interrupt Status Register 4	314
x6E	GIS	R	Global Interrupt Status	314
6F	CIS	R	Channel Interrupt Status Register	315
x70	RS1	R	Receive CAS Register 1	316
x71	RS2	R	Receive CAS Register 2	316
x72	RS3	R	Receive CAS Register 3	316
x73	RS4	R	Receive CAS Register 4	316
x74	RS5	R	Receive CAS Register 5	316
x75	RS6	R	Receive CAS Register 6	316
x76	RS7	R	Receive CAS Register 7	316
x77	RS8	R	Receive CAS Register 8	316
x78	RS9	R	Receive CAS Register 9	316
x79	RS10	R	Receive CAS Register 10	316
x7A	RS11	R	Receive CAS Register 11	316
x7B	RS12	R	Receive CAS Register 12	316
x7C	RS13	R	Receive CAS Register 13	316
x7D	RS14	R	Receive CAS Register 14	316
x7E	RS15	R	Receive CAS Register 15	316
x7F	RS16	R	Receive CAS Register 16	316

1) x = 0: channel 1 register; x = 1: channel 2 register; x = 2: channel 3 register; x = 3: channel 4 register

9.4 Detailed Description of E1 Status Registers

Receive FIFO (Read)

	7							0	
RFIFO	RF7							RF0	(x00)
RFIFO	RF15							RF8	(x01)

Reading data from RFIFO can be done in an 8-bit (byte) or 16-bit (word) access depending on the selected bus interface mode. The LSB is received first from the serial interface.

The size of the accessible part of RFIFO is determined by programming the bits CCR1.RFT(1:0) (RFIFO threshold level). It can be reduced from 32 bytes (reset value) down to 2 bytes (four values: 32, 16, 4, 2 bytes).

Data Transfer

Up to 32 bytes/16 words of received data can be read from the RFIFO following an RPF or an RME interrupt.
RPF Interrupt: A fixed number of bytes/words to be read (32, 16, 4, 2 bytes). The message is not yet complete.

RME Interrupt: The message is completely received. The number of valid bytes is determined by reading the RBCL, RBCH registers.

RFIFO is released by issuing the “Receive Message Complete” command (RMC).

Receive Buffer Delay (Read)

	7							0	
RBD			RBD5	RBD4	RBD3	RBD2	RBD1	RBD0	(x49)

RBD(5:0) **Receive Elastic Buffer Delay**

These bits informs the user about the current delay (in time slots) through the receive elastic buffer. The delay is updated every 512 or 256 bits (SIC1.RBS1/0). Before reading this register the user has to set bit DEC.DRBD in order to halt the current value of this register. After reading RBD updating of this register is enabled. Not valid if the receive buffer is bypassed.

000000 = delay < 1 time slot
...
111111 = delay > 63 time slots

Version Status Register (Read)

	7						0	
VSTR	VN7						VN0	(4A)

VN(7:0) **Version Number of Chip**

05_H Version 2.1

Receive Equalizer Status (Read)

	7							0	
RES	EV1	EV0		RES4	RES3	RES2	RES1	RES0	(x4B)

EV(1:0) **Equalizer Status Valid**

These bits informs the user about the current state of the receive equalization network. Only valid if LIM1.EQON is set.

00 equalizer status not valid, still adapting

01 equalizer status valid

10 equalizer status not valid

11 equalizer status valid but high noise floor

RES(4:0) **Receive Equalizer Status**

The current line attenuation status in steps of about 1.7 dB are displayed in these bits. Only valid if bits EV1/0 = 01 and LIM1.EQON = 1. Accuracy: ± 2 digits, based on temperature influence and noise amplitude variations.

00000 minimum attenuation: 0 dB

...

11001 maximum attenuation: -43 dB

Framer Receive Status Register 0 (Read)

	7							0	
FRS0	LOS	AIS	LFA	RRA		NMF	LMFA		(x4C)

LOS **Loss of Signal**

Detection:
This bit is set when the incoming signal has “no transitions” (analog interface) or logical zeros (digital interface) in a time interval of T consecutive pulses, where T is programmable by register PCD.
Total account of consecutive pulses: 16 < T < 4096.

Analog interface: The receive signal level where “no transition” is declared is defined by the programmed value of LIM1.RIL(2:0).

Recovery:
Analog interface: The bit is reset in short haul mode when the incoming signal has transitions with signal levels greater than the programmed receive input level (LIM1.RIL(2:0)) for at least M pulse periods defined by register PCR in the PCD time interval. In long haul mode additionally bit RES.6 must be set for at least 250µsec.
Digital interface: The bit is reset when the incoming data stream contains at least M ones defined by register PCR in the PCD time interval.

With the rising edge of this bit an interrupt status bit (ISR2.LOS) is set. The bit is also set during alarm simulation and reset, if FMR0.SIM is cleared and no alarm condition exists.

AIS **Alarm Indication Signal**

The function of this bit is determined by FMR0.ALM.

FMR0.ALM = 0: This bit is set when two or less zeros in the received bit stream are detected in a time interval of 250 µs and the QuadFALC is in asynchronous state (FRS0.LFA = 1). The bit is reset when no alarm condition is detected (according to ETSI standard).

FMR0.ALM = 1: This bit is set when the incoming signal has two or less Zeros in each of two consecutive double frame period (512 bits). This bit is cleared when each of two consecutive doubleframe periods contain three or more zeros or when the frame alignment signal FAS has been found. (ITU-T G.775)

The bit is also set during alarm simulation and reset if FMR0.SIM is cleared and no alarm condition exists.

With the rising edge of this bit an interrupt status bit (ISR2.AIS) is set.

LFA **Loss of Frame Alignment**

This bit is set after detecting 3 or 4 consecutive incorrect FAS words or 3 or 4 consecutive incorrect service words (can be disabled). With the rising edge of this bit an interrupt status bit (ISR2.LFA) is set. The specification of the loss of synchronization conditions is done by bits RC0.SWD and RC0.ASY4. After loss of synchronization, the frame aligner resynchronizes automatically.

The following conditions have to be detected to regain synchronous state:

–The presence of the correct FAS word in frame n.
–The presence of the correct service word (bit 2 = 1) in frame n+1.
–For a second time the presence of a correct FAS word in frame n+2.

The bit is cleared when synchronization has been regained (directly after the second correct FAS word of the procedure described above has been received).

If the CRC-multiframe structure is enabled by setting bit FMR2.RFS1, multiframe alignment is assumed to be lost if pulseframe synchronization has been lost. The resynchronization procedure for multiframe alignment starts after the bit FRS0.LFA has been cleared.

Multiframe alignment has been regained if two consecutive CRC-multiframes have been received without a framing error (refer to FRS0.LMFA).

The bit is set during alarm simulation and reset if FMR0.SIM is cleared and no alarm condition exists.

If bit FRS0.LFA is cleared a loss of frame alignment recovery interrupt status ISR2.FAR is generated.

RRA **Receive Remote Alarm**

Set if bit 3 of the received service word is set. An alarm interrupt status ISR2.RA can be generated if the alarm condition is detected.

FRS0.RRA is cleared if no alarm is detected. At the same time a remote alarm recovery interrupt status ISR2.RAR is generated.

The bit RSW.RRA has the same function.

Both status and interrupt status bits are set during alarm simulation.

NMF **No Multiframe Alignment Found**

This bit is only valid if the CRC4 interworking is selected (FMR2.RFS1/0 = 11). Set if the multiframe pattern is not detected in a time interval of 400 ms after the framer has reached the doubleframe synchronous state. The receiver is then automatically switched to doubleframe format.

This bit is reset if the basic framing has been lost.

LMFA **Loss of Multiframe Alignment**

Not used in doubleframe format (FMR2.RFS1 = 0). In this case LMFA is set.

In CRC-multiframe mode (FMR2.RFS1 = 1), this bit is set

– if force resynchronization is initiated by setting bit FMR0.FRS, or

– if multiframe force resynchronization is initiated by setting bit FMR1.MFCS, or

– if pulseframe alignment has been lost (FRS0.LFA).

It is reset if two CRC-multiframes have been received at an interval of $n \times 2$ ms (n = 1, 2, 3…) without a framing error.

If bit FRS0.LMFA is cleared a loss of multiframe alignment recovery interrupt status ISR2.MFAR is generated.

Framer Receive Status Register 1 (Read)

	7							0	
FRS1	EXZD	TS16RA	TS16LOS	TS16AIS	TS16LFA		XLS	XLO	(X4D)

EXZD **Excessive Zeros Detected**

Significant only, if excessive zero detection has been enabled (FMR0.EXZE = 1). Set after detection of more than 3 (HDB3 code) or 15 (AMI code) contiguous zeros in the received data stream.
This bit is cleared on read.

TS16RA **Receive Time Slot 16 Remote Alarm**

This bit contains the actual information of the received remote alarm bit RS1.2 in time slot 16. Setting and resetting of this bit causes an interrupt status change ISR3.RA16.

TS16LOS **Receive Time Slot 16 Loss of Signal**

This bit is set if the incoming TS16 data stream contains always zeros for at least 16 contiguously received time slots. A one in a time slot 16 resets this bit.

TS16AIS **Receive Time Slot 16 Alarm Indication Signal**

The detection of the alarm indication signal in time slot 16 is according to ITU-T G.775.

This bit is set if the incoming TS16 contains less than 4 zeros in each of two consecutive TS16 multiframe periods. This bit is cleared if two consecutive received CAS multiframe periods contains more than 3 zeros or the multiframe pattern was found in each of them. This bit is cleared if TS0 synchronization is lost.

TS16LFA **Receive Time Slot 16 Loss of Multiframe Alignment**

0 The CAS controller is in synchronous state after frame alignment is accomplished.

1 This bit is set if the framing pattern ’0000’ in 2 consecutive CAS multiframes were not found or in all TS16 of the preceding multiframe all bits were reset. An interrupt ISR3.LMFA16 is generated.

XLS **Transmit Line Short**

Significant only if the ternary line interface is selected by LIM1.DRS = 0.

0 Normal operation. No short is detected.

1 The XL1 and XL2 are shortened for at least 3 pulses. As a reaction of the short the pins XL1 and XL2 are automatically forced into a high impedance state if bit XPM2.DAXLT is reset. After 128 consecutive pulse periods the outputs XL1/2 are activated again and the internal transmit current limiter is checked. If a short between XL1/2 is still further active the outputs XL1/2 are in high impedance state again. When the short disappears pins XL1/2 are activated automatically and this bit is reset. With any change of this bit an interrupt ISR1.XLSC is generated. In case of XPM2.XLT is set this bit is frozen.

XLO **Transmit Line Open**

0 Normal operation

1 This bit is set if at least 32 consecutive zeros were sent on pins XL1/XL2 or XDOP/XDON. This bit is reset with the first transmitted pulse. With the rising edge of this bit an interrupt ISR1.XLSC is set. In case of XPM2.XLT is set this bit is frozen.

Receive Service Word Pulseframe (Read)

	7							0	
RSW	RSI		RRA	RY0	RY1	RY2	RY3	RY4	(x4E)

RSI **Receive Spare Bit for International Use**

First bit of the received service word. It is fixed to one if CRC-multiframe mode is enabled.

RRA **Receive Remote Alarm**

Equivalent to bit FRS0.RRA.

RY(4:0) **Receive Spare Bits for National Use (Y-Bits, S_n-Bits, S_a-Bits)**

Receive Spare Bits/Additional Status (Read)

	7							0	
RSP	SI1	SI2		LLBDD	LLBAD	RSIF	RS13	RS15	(x4F)

SI(2:1) **Submultiframe Error Indication 1, 2**

Not valid if doubleframe format is enabled. In this case, both bits are set.

When using CRC-multiframe format these bits are set to

0 If multiframe alignment has been lost, or
if the last multiframe has been received with CRC error(s). SI1 flags a CRC error in last submultiframe 1, SI2 flags a CRC error in last submultiframe 2.

1 If at multiframe synchronous state last assigned submultiframe has been received without a CRC error.

Both flags are updated with the beginning of every received CRC multiframe.

If automatic transmission of submultiframe status is enabled by setting bit XSP.AXS, above status information is inserted automatically in S_i-bit position of every outgoing CRC multiframe (under the condition that time slot 0 transparent modes are both disabled):
SI1 $\rightarrow$ S_i -bit of frame 13, SI2 $\rightarrow$ S_i -bit of frame 15.

LLBDD **Line Loop Back Deactivation Signal Detected**

This bit is set in case of the LLB deactivate signal has been detected and then received over a period of more than 25 ms with a bit error rate less than 10^{-2}. The bit remains set as long as the bit error rate does not exceed 10^{-2}.

If framing is aligned, the time slot 0 is not taken into account for the error rate calculation.

Any change of this bit causes an LLBSC interrupt.

LLBAD **Line Loop Back Activation Signal Detected**

Depending on bit LCR1.EPRM the source of this status bit changed.

LCR1.EPRM = 0: This bit is set in case of the LLB activate signal is detected and then received over a period of more than 25 ms with a bit error rate less than 10^{-2}. The bit remains set as long as the bit error rate does not exceed 10^{-2}.

If framing is aligned, the time slot 0 is not taken into account for the error rate calculation.

Any change of this bit causes an LLBSC interrupt.

PRBS Status

LCR1.EPRM = 1: The current status of the PRBS synchronizer is indicated in this bit. It is set high if the synchronous state is reached even in the presence of a bit error rate of 10^{-1}. A data stream containing all zeros or all ones with/without framing bits is also a valid pseudo random bit sequence.

RSIF **Receive Spare Bit for International Use (FAS Word)**

First bit in FAS-word. Used only in doubleframe format, otherwise fixed to ’1’.

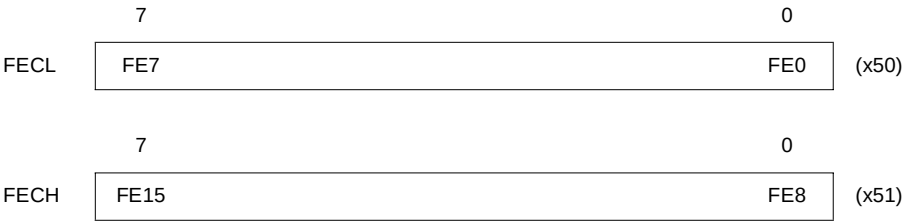
RS13 **Receive Spare Bit (Frame 13, CRC Multiframe)**

First bit in service word of frame 13. Significant only in CRC-multiframe format, otherwise fixed to ’0’. This bit is updated with beginning of every received CRC multiframe.

RS15 **Receive Spare Bit (Frame 15, CRC Multiframe)**

First bit in service word of frame 15. Significant only in CRC-multiframe format, otherwise fixed to ’0’. This bit is updated with beginning of every received CRC multiframe.

Framing Error Counter (Read)



FE(15:0) **Framing Errors**

This 16-bit counter is incremented when a FAS word has been received with an error.

Framing errors are counted during basic frame synchronous state only (but even if multiframe synchronous state is not reached yet). During alarm simulation, the counter is incremented every 250 µs up to its saturation. The error counter does not roll over.

Clearing and updating the counter is done according to bit FMR1.ECM.
If this bit is reset the error counter is permanently updated in the buffer. For correct read access of the error counter bit DEC.DFEC has to be set. With the rising edge of this bit updating the buffer is stopped and the error counter is reset. Bit DEC.DFEC is reset automatically with reading the error counter high byte.

If FMR1.ECM is set every second (interrupt ISR3.SEC) the error counter is latched and then automatically reset. The latched error counter state should be read within the next second.

Code Violation Counter (Read)

	7		0	
CVCL	CV7		CV0	(x52)

	7		0	
CVCH	CV15		CV8	(x53)

CV(15:0) **Code Violations**

No function if NRZ code has been enabled.

If the HDB3 or the CMI code with HDB3-precoding is selected, the 16-bit counter is incremented when violations of the HDB3 code are detected. The error detection mode is determined by programming the bit FMR0.EXTD.

If simple AMI coding is enabled (FMR0.RC0/1 = 10) all bipolar violations are counted. The error counter does not roll over.

During alarm simulation, the counter is incremented every four bits received up to its saturation.

Clearing and updating the counter is done according to bit FMR1.ECM.
If this bit is reset the error counter is permanently updated in the buffer. For correct read access of the error counter bit DEC.DCVC has to be set. With the rising edge of this bit updating the buffer is stopped and the error counter is reset. Bit DEC.DCVC is reset automatically with reading the error counter high byte.

If FMR1.ECM is set every second (interrupt ISR3.SEC) the error counter is latched and then automatically reset. The latched error counter state should be read within the next second.

CRC Error Counter 1 (Read)

	7		0	
CEC1L	CR7		CR0	(x54)

	7		0	
CEC1H	CR15		CR8	(x55)

CR(15:0) **CRC Errors**

No function if doubleframe format is selected.

In CRC-multiframe mode, the 16-bit counter is incremented when a CRC-submultiframe has been received with a CRC error. CRC errors are not counted during asynchronous state. The error counter does not roll over.

During alarm simulation, the counter is incremented once per submultiframe up to its saturation.

Clearing and updating the counter is done according to bit FMR1.ECM.
If this bit is reset the error counter is permanently updated in the buffer. For correct read access of the error counter bit DEC.DCEC1 has to be set. With the rising edge of this bit updating the buffer is stopped and the error counter is reset. Bit DEC.DCEC1 is reset automatically with reading the error counter high byte.

If FMR1.ECM is set every second (interrupt ISR3.SEC) the error counter is latched and then automatically reset. The latched error counter state should be read within the next second.

E-Bit Error Counter (Read)

	7		0	
EBCL	EB7		EB0	(x56)

	7		0	
EBCH	EB15		EB8	(x57)

EB(15:0) **E-Bit Errors**

If doubleframe format is selected, FEBEH/L has no function. If CRC-multiframe mode is enabled, FEBEH/L works as submultiframe error indication counter (16 bits) which counts zeros in Si-bit position of frame 13 and 15 of every received CRC multiframe. The error counter does not roll over.

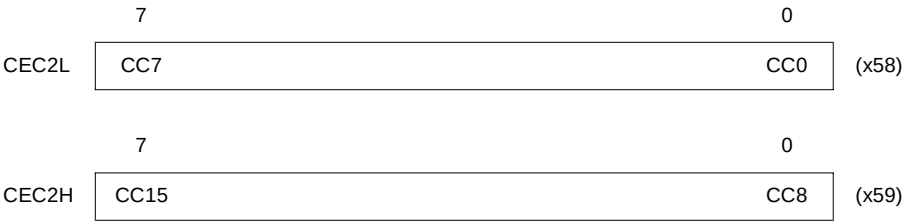
During alarm simulation, the counter is incremented once per submultiframe up to its saturation.

Clearing and updating the counter is done according to bit FMR1.ECM.

If this bit is reset the error counter is permanently updated in the buffer. For correct read access of the error counter bit DEC.DEBC has to be set. With the rising edge of this bit updating the buffer is stopped and the error counter is reset. Bit DEC.DEBC is reset automatically with reading the error counter high byte.

If FMR1.ECM is set every second (interrupt ISR3.SEC) the error counter is latched and then automatically reset. The latched error counter state should be read within the next second.

CRC Error Counter 2 (Read)



CC(15:0) **CRC Error Counter (reported from TE through S_a6 -Bit)**

Depending on bit LCR1.EPRM the error counter increment is selected:

LCR1.EPRM = 0:
If doubleframe format is selected, CEC2H/L has no function. If CRC-multiframe mode is enabled, CEC2H/L works as S_a6-bit error indication counter (16 bits) which counts the S_a6-bit sequence 0001 and 0011in every received CRC submultiframe.
Incrementing the counter is only possible in the multiframe synchronous state FRS0.LMFA = 0.

S_a6-bit sequence: SA61, SA62, SA63, SA64 = 0001 or 0011 where SA61 is received in frame 1 or 9 in every multiframe.

During alarm simulation, the counter is incremented once per submultiframe up to its saturation.

Pseudo Random Bit Sequence Error Counter

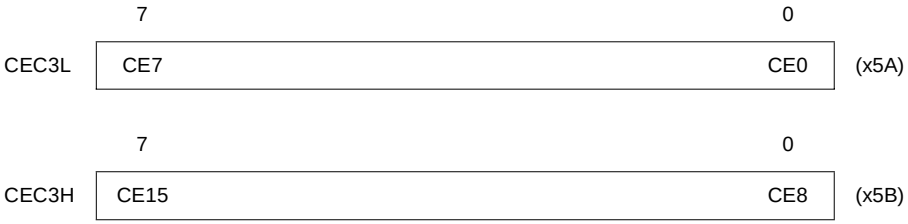
LCR1.EPRM = 1:
This 16-bit counter is incremented with every received PRBS bit error in the PRBS synchronous state RSP.LLBAD = 1. The error counter does not roll over.

During alarm simulation, the counter is incremented continuously with every second received bit.

Clearing and updating the counter is done according to bit FMR1.ECM.
If this bit is reset the error counter is permanently updated in the buffer. For correct read access of the error counter bit DEC.DCEC2 has to be set. With the rising edge of this bit updating of the buffer is stopped and the error counter is reset. Bit DEC.DCEC2 is reset automatically with reading the error counter high byte.

If FMR1.ECM is set every second (interrupt ISR3.SEC) the error counter is latched and then reset automatically. The latched error counter state should be read within the next second.

CRC Error Counter 3 (Read)



CE(15:0) **CRC Error Counter (detected at T Reference Point in S_a6 -Bit)**

GCR.ECMC = 0: If doubleframe format is selected, CEC3H/L has no function. If CRC-multiframe mode is enabled, CEC3H/L works as S_a6-bit error indication counter (16 bits) which counts the S_a6-bit sequence 0010 and 0011in every received CRC submultiframe.
Incrementing the counter is only possible in the multiframe synchronous state FRS0.LMFA = 0.

S_a6-bit sequence: SA61, SA62, SA63, SA64 = 0010 or 0011 where SA61 is received in frame 1 or 9 in every multiframe. The error counter does not roll over.
During alarm simulation, the counter is incremented once per submultiframe up to its saturation.

CE(7:2) **Multiframe Counter**

GCR.ECMC = 1: This 6 bit counter increments with each multiframe period in the asynchronous state FRS0.LFA/LMFA = 1.

During alarm simulation, the counter is incremented once per multiframe up to its saturation.

CE(1:0) **Change of Frame Alignment Counter**

GCR.ECMC = 1: This 2 bit counter increments with each detected change of frame/multiframe alignment. The error counter does not roll over.

During alarm simulation, the counter is incremented once per multiframe up to its saturation.
Clearing and updating the counter is done according to bit FMR1.ECM.

If this bit is reset the error counter is permanently updated in the buffer. For correct read access of the error counter bit DEC.DCEC3 has to be set. With the rising edge of this bit updating of the buffer is stopped and the error counter is reset. Bit DEC.DCEC3 is reset automatically with reading the error counter high byte.

If FMR1.ECM is set every second (interrupt ISR3.SEC) the error counter is latched and then automatically reset. The latched error counter state should be read within the next second.

Receive S_a4-Bit Register (Read)

	7	0	
RSA4	RS47	RS40	(x5C)
RSA5	RS57	RS50	(x5D)
RSA6	RS67	RS60	(x5E)
RSA7	RS77	RS70	(x5F)
RSA8	RS87	RS80	(x60)

RS4(7:0) **Receive S_a4-Bit Data (Y-Bits)**

RS5(7:0) **Receive S_a5-Bit Data**

RS6(7:0) **Receive S_a6-Bit Data**

RS7(7:0) **Receive S_a7-Bit Data**

RS8(7:0) **Receive S_a8-Bit Data**

This register contains the information of the eight S_ax bits (x = 4 to 8) of the previously received CRC multiframe. These registers are updated with every multiframe begin interrupt ISR0.RMB.

RS40 is received in bit-slot 4 of every service word in frame 1, RS47 in frame 15

RS50 is received in bit-slot 5, time slot 0, frame 1, RS57 in frame 15

RS60 is received in bit-slot 6, time slot 0, frame 1, RS67 in frame 15

RS70 is received in bit-slot 7, time slot 0, frame 1, RS77 in frame 15

RS80 is received in bit-slot 8, time slot 0, frame 1, RS87 in frame 15

Valid if CRC multiframe format is enabled by setting bits FMR2.RFS1 = 1 or FMR2.RFS1/0 = 01 (Doubleframe format).

Receive S_a6-Bit Status (Read)

	7							0	
RSA6S			S_X	S_F	S_E	S_C	S_A	S_8	(x61)

Four consecutive received S_a6-bits are checked on the by ETS300233 defined S_a6-bit combinations. The QuadFALC detects the following “fixed” S_a6-bit combinations:
SA61,SA62,SA63,SA64 = 1000; 1010; 1100; 1110; 1111. All other possible 4 bit combinations are grouped to status “X”.

A valid S_a6-bit combination must occur three times in a row. The corresponding status bit in this register is set. Even if the detected status is active for a short time the status bit remains active until this register is read. Reading the register resets all pending status information.
With any change of state of the S_a6-bit combinations an interrupt status ISR0.SA6SC is generated.
During the basic frame asynchronous state updating of this register and interrupt status ISR0.SA6SC is disabled. In multiframe format the detection of the S_a6-bit combinations can be done either synchronous or asynchronous to the submultiframe (FMR3.SA6SY). In synchronous detection mode updating of register RSA6S is done in the multiframe synchronous state (FRS0.LMFA = 0). In asynchronous detection mode updating is independent to the multiframe synchronous state.

S_X **Receive S_a6-Bit Status_X**

If none of the fixed S_a6-bit combinations are detected this bit is set.

S_F **Receive S_a6-Bit Status: ’1111’**

Receive S_a6-bit status “1111” is detected for three times in a row in the S_a6-bit positions.

S_E **Receive S_a6-Bit Status: ’1110’**

Receive S_a6-bit status “1110” is detected for three times in a row in the S_a6-bit positions.

S_C **Receive S_a6-Bit Status: ’1100’**

Receive S_a6-bit status “1100” is detected for three times in a row in the S_a6bit positions.

S_A **Receive S_a6-Bit Status: ’1010’**

Receive S_a6-bit status “1010” is detected for three times in a row in the S_a6-bit positions.

S_8 **Receive S_a6-Bit Status: ’1000’**

Receive S_a6-bit status “1000” is detected for three times in a row in the S_a6-bit positions.

Receive Signaling Pointer 1 (Read)

Value after reset: 00_H

	7							0	
RSP1	RS8C	RS7C	RS6C	RS5C	RS4C	RS3C	RS2C	RS1C	(x62)

RS(8:1)C **Receive Signaling Register RS1 to 8 Changed**

A one in each bit position indicates that the received signaling data in the corresponding RS(8:1) registers are updated. Bit RS1C is the pointer for register RS1,... while RS8C points to RS8.

Receive Signaling Pointer 2 (Read)

Value after reset: 00_H

	7							0	
RSP2	RS16C	RS15C	RS14C	RS13C	RS12C	RS11C	RS10C	RS9C	(x63)

RS(16:9)C **Receive Signaling Register RS9 to 16 Changed**

A one in each bit position indicates that the received signaling data in the corresponding RS(16:9) registers are updated. Bit RS9C is the pointer for register RS9,... while RS16C points to RS16.

Signaling Status Register (Read)

	7							0	
SIS	XDOV	XFW	XREP		RLI	CEC	SFS		(x64)

XDOV **Transmit Data Overflow**

More than 32 bytes have been written to the XFIFO.
This bit is reset by:

– a transmitter reset command XRES

– or when all bytes in the accessible half of the XFIFO have been moved in the inaccessible half.

XFW **Transmit FIFO Write Enable**

Data can be written to the XFIFO.

XREP **Transmission Repeat**

Status indication of CMDR.XREP.

RLI **Receive Line Inactive**

Neither flags as interframe time fill nor frames are received through the signaling time slot.

CEC **Command Executing**

0 No command is currently executed, the CMDR register can be written to.

1 A command (written previously to CMDR) is currently executed, no further command can be temporarily written in CMDR register.

Note: CEC is active for about 2.5 periods of the current system data rate.

SFS **Status Freeze Signaling**

0 freeze signaling status inactive.

1 freeze signaling status active

Receive Signaling Status Register (Read)

	7							0	
RSIS	VFR	RDO	CRC16	RAB	HA1	HA0		LA	(x65)

RSIS relates to the last received HDLC frame; it is copied into RFIFO when end-of-frame is recognized (last byte of each stored frame).

VFR **Valid Frame**

Determines whether a valid frame has been received.

1 valid

0 invalid

An invalid frame is either

– a frame which is not an integer number of 8 bits (n×8 bits) in length (e.g. 25 bits), or

– a frame which is too short taking into account the operation mode selected by MODE (MDS(2:0)) and the selection of receive CRC on/off (CCR2.RCRC) as follows:

- MDS(2:0) = 011 (16 bit Address),
  RCRC = 0: 4 bytes; RCRC = 1: 3 to 4 bytes
- MDS(2:0) = 010 (8 bit Address),
  RCRC = 0: 3 bytes; RCRC = 1: 2 to 3 bytes

Note: Shorter frames are not reported.

RDO **Receive Data Overflow**

A RFIFO data overflow has occurred during reception of the frame.

Additionally, an interrupt can be generated (refer to ISR1.RDO/ IMR1.RDO).

CRC16 **CRC16 Compare/Check**

0 CRC check failed; received frame contains errors.

1 CRC check o.k.; received frame is error-free.

RAB **Receive Message Aborted**

This bit is set in SS7 mode, if the maximum number of octets (272+7) is exceeded. The received frame was aborted from the transmitting station. According to the HDLC protocol, this frame must be discarded by the receiver station.

HA1, HA0 **High Byte Address Compare**

Significant only if 2-byte address mode or SS7 mode has been selected.

In operating modes which provide high byte address recognition, the QuadFALC compares the high byte of a 2-byte address with the contents of two individually programmable registers (RAH1, RAH2) and the fixed values FE_H and FC_H (broadcast address).

Depending on the result of this comparison, the following bit combinations are possible (SS7 support not active):

00 RAH2 has been recognized

01 Broadcast address has been recognized

10 RAH1 has been recognized C/R = 0 (bit 1)

11 RAH1 has been recognized C/R = 1 (bit 1)

Note: If RAH1, RAH2 contain identical values, a match is indicated by '10' or '11'.

If Signaling System 7 support is activated (see MODE register), the bit functions are defined as follows:

00 not valid

01 Fill in signaling unit (FISU) detected

10 Link status signaling unit (LSSU) detected

11 Message signaling unit (MSU) detected

LA **Low Byte Address Compare**

Significant in HDLC modes only.

The low byte address of a 2-byte address field, or the single address byte of a 1-byte address field is compared to two registers. (RAL1, RAL2).

0 RAL2 has been recognized

1 RAL1 has been recognized

Receive Byte Count Low(Read)

	7							0	
RBCL	RBC7							RBC0	(x66)

Together with RBCH (bits RBC(11:8)), indicates the length of a received frame (1 to 4095 bytes). Bits RBC(4:0) indicate the number of valid bytes currently in RFIFO. These registers must be read by the CPU following a RME interrupt.

Received Byte Count High (Read)

Value after reset: 000_{xxxxx}

	7							0	
RBCH				OV	RBC11	RBC10	RBC9	RBC8	(x67)

OV **Counter Overflow**

More than 4095 bytes received.

RBC(11:8) **Receive Byte Count (most significant bits)**

Together with RBCL (bits RBC(7:0)) indicates the length of the received frame.

Interrupt Status Register 0 (Read)

Value after reset: 00_H

	7							0	
ISR0	RME	RFS	T8MS	RMB	CASC	CRC4	SA6SC	RPF	(x68)

All bits are reset when ISR0 is read.

If bit GCR.VIS is set, interrupt statuses in ISR0 are flagged although they are masked by register IMR0. However, these masked interrupt statuses neither generate a signal on INT, nor are visible in register GIS.

RME **Receive Message End**

One complete message of length less than 32 bytes, or the last part of a frame at least 32 bytes long is stored in the receive FIFO, including the status byte.

The complete message length can be determined reading the RBCH, RBCL registers, the number of bytes currently stored in RFIFO is given by RBC(4:0). Additional information is available in the RSIS register.

RFS **Receive Frame Start**

This is an early receiver interrupt activated after the start of a valid frame has been detected, i.e. after an address match (in operation modes providing address recognition), or after the opening flag (transparent mode 0) is detected, delayed by two bytes. After an RFS interrupt, the contents of

- RAL1
- RSIS bits (3:1)

are valid and can be read by the CPU.

T8MS **Receive Time Out 8 ms**

Only active if multiframing is enabled.

The framer has found the double framing (basic framing) FRS0.LFA = 0 and is searching for the multiframing. This interrupt is set to indicate that no multiframing was found within a time window of 8 ms. In multiframe synchronous state this interrupt is not generated. Refer also to floating multiframe alignment window.

RMB **Receive Multiframe Begin**

This bit is set with the beginning of a received CRC multiframe related to the internal receive line timing.

In CRC multiframe format FMR2.RFS1 = 1 or in doubleframe format FMR2.RFS1/0 = 01 this interrupt occurs every 2 ms. If FMR2.RFS1/0 = 00 this interrupt is generated every doubleframe (512 bits).

CASC **Received CAS Information Changed**

This bit is set with the updating of a received CAS multiframe information in the registers RS(16:1). If the last received CAS information is different to the previous received one, this interrupt is generated after update has been completed. This interrupt only occurs only in TS0 and TS16 synchronous state. The registers RS(16:1) should be read within the next 2 ms otherwise the contents is lost.

CRC4 **Receive CRC4 Error**

0 No CRC4 error occurs.

1 The CRC4 check of the last received submultiframe failed.

SA6SC **Receive S_a6-Bit Status Changed**

With every change of state of the received S_a6-bit combinations this interrupt is set.

RPF **Receive Pool Full**

32 bytes of a frame have arrived in the receive FIFO. The frame is not yet completely received.

Interrupt Status Register 1 (Read)

	7							0	
ISR1	LLBSC	RDO	ALLS	XDU	XMB	SUEX	XLSC	XPR	(x69)

All bits are reset when ISR1 is read.

If bit GCR.VIS is set, interrupt statuses in ISR1 are flagged although they are masked by register IMR1. However, these masked interrupt statuses neither generate a signal on INT, nor are visible in register GIS.

LLBSC **Line Loop Back Status Change**

Depending on bit LCR1.EPRM the source of this interrupt status changed:

LCR1.EPRM = 0: This bit is set, if the LLB activate signal or the LLB deactivate signal, respectively, is detected over a period of 25 ms with a bit error rate less than 10^{-2}.

The LLBSC bit is also set, if the current detection status is left, i.e., if the bit error rate exceeds 10^{-2}.

The actual detection status can be read from the RSP.LLBAD and RSP.LLBDD, respectively.

PRBS Status Change

LCR1.EPRM = 1: With any change of state of the PRBS synchronizer this bit is set. The current status of the PRBS synchronizer is indicated in RSP.LLBAD.

RDO **Receive Data Overflow**

This interrupt status indicates that the CPU did not respond fast enough to an RPF or RME interrupt and that data in RFIFO has been lost. Even when this interrupt status is generated, the frame continues to be received when space in the RFIFO is available again.

Note: Whereas the bit RSIS.RDO in the frame status byte indicates whether an overflow occurred when receiving the frame

currently accessed in the RFIFO, the ISR1.RDO interrupt status is generated as soon as an overflow occurs and does not necessarily pertain to the frame currently accessed by the processor.

ALLS **All Sent**

This bit is set if the last bit of the current frame has been sent completely and XFIFO is empty. This bit is valid in HDLC mode only.

XDU **Transmit Data Underrun**

Transmitted frame was terminated with an abort sequence because no data was available for transmission in XFIFO and no XME was issued.

Note: Transmitter and XFIFO are reset and deactivated if this condition occurs. They are reactivated not before this interrupt status register has been read. Thus, XDU should not be masked by register IMR1.

XMB **Transmit Multiframe Begin**

This bit is set every 2 ms with the beginning of a transmitted multiframe related to the internal transmit line interface timing.
Just before setting this bit registers XS(16:1) are copied in the transmit shift registers. The registers XS(16:1) are empty and has to be updated otherwise the contents is retransmitted.

SUEX **Signaling Unit Error Threshold Exceeded**

Masks the indication by interrupt that the selected error threshold for SS7 signaling units has been exceeded.

0 signaling unit error count below selected threshold

1 signaling unit error count exceeded selected threshold

Note: SUEX is only valid, if SS7 mode is selected.
If SUEX is caused by an aborted/invalid frame, the interrupt will be issued regularly until a valid frame is received (e.g. a FISU).

XLSC **Transmit Line Status Change**

XLSC is set with the rising edge of the bit FRS1.XLO or with any change of bit FRS1.XLS.

The actual status of the transmit line monitor can be read from the FRS1.XLS and FRS1.XLO.

XPR **Transmit Pool Ready**

A data block of up to 32 bytes can be written to the transmit FIFO. XPR enables the fastest access to XFIFO. It has to be used for transmission of long frames, back-to-back frames or frames with shared flags.

Interrupt Status Register 2 (Read)

	7							0	
ISR2	FAR	LFA	MFAR	T400MS	AIS	LOS	RAR	RA	(x6A)

All bits are reset when ISR2 is read.

If bit GCR.VIS is set, interrupt statuses in ISR2 are flagged although they are masked by register IMR2. However, these masked interrupt statuses neither generate a signal on INT, nor are visible in register GIS.

FAR **Frame Alignment Recovery**

The framer has reached doubleframe synchronization. Set when bit FRS0.LFA is reset. It is set also after alarm simulation is finished and the receiver is still synchronous.

LFA **Loss of Frame Alignment**

The framer has lost synchronization and bit FRS0.LFA is set. It is set during alarm simulation.

MFAR **Multiframe Alignment Recovery**

Set when the framer has found two CRC-multiframes at an interval of n×2 ms (n = 1, 2, 3, ...) without a framing error. At the same time bit FRS0.LMFA is reset.

It is set also after alarm simulation is finished and the receiver is still synchronous. Only active if CRC-multiframe format is selected.

T400MS **Receive Time Out 400 ms**

Only active if multiframing is enabled.

The framer has found the doubleframes (basic framing) FRS0.LFA = 0 and is searching for the multiframing. This interrupt is set to indicate that no multiframing was found within a time window of 400 ms after basic framing has been achieved. In multiframe synchronous state this interrupt is not generated.

AIS **Alarm Indication Signal**

This bit is set when an alarm indication signal is detected and bit FRS0.AIS is set. It is set during alarm simulation.
If GCR.SCI is set high this interrupt status bit is set with every change of state of FRS0.AIS.

LOS **Loss of Signal**

This bit is set when a loss of signal alarm is detected in the received bitstream and FRS0.LOS is set. It is set during alarm simulation.
If GCR.SCI is set high this interrupt status bit is set with every change of state of FRS0.LOS.

RAR **Remote Alarm Recovery**

Set if a remote alarm in TS0 is cleared and bit FRS0.RRA is reset. It is set also after alarm simulation is finished and no remote alarm is detected.

RA **Remote Alarm**

Set if a remote alarm in TS0 is detected and bit FRS0.RRA is set. It is set during alarm simulation.

Interrupt Status Register 3 (Read)

	7							0	
ISR3	ES	SEC	LMFA16	AIS16	RA16		RSN	RSP	(x6B)

All bits are reset when ISR3 is read.

If bit GCR.VIS is set, interrupt statuses in ISR3 are flagged although they are masked by register IMR3. However, these masked interrupt statuses neither generate a signal on INT, nor are visible in register GIS.

ES **Errored Second**

This bit is set if at least one enabled interrupt source by ESM is set during the time interval of one second. Interrupt sources of ESM register:
LFA = Loss of frame alignment detected (FRS0.LFA)
FER = Framing error received
CER = CRC error received
AIS = Alarm indication signal (FRS0.AIS)
LOS = Loss of signal (FRS0.LOS)
CVE = Code violation detected
SLIP = Receive Slip positive/negative detected
EBE = E-Bit error detected (RSP.RS13/15)

SEC **Second Timer**

The internal one second timer has expired. The timer is derived from clock RCLK or external pin SEC/FSC.

LMFA16 **Loss of Multiframe Alignment TS 16**

Multiframe alignment of time slot 16 has been lost if two consecutive multiframe pattern are not detected or if in 16 consecutive time slot 16 all bits are reset.
If register GCR.SCI is high this interrupt status bit is set with every change of state of FRS1.TS16LFA.

AIS16 **Alarm Indication Signal TS 16 Status Change**

The alarm indication signal AIS in time slot 16 for the 64 kbit/s channel associated signaling is detected or cleared. A change in bit FRS1.TS16AIS sets this interrupt. (This bit is set if the incoming TS 16 signal contains less than 4 zeros in each of two consecutive TS16-multiframe periods.)

RA16 **Remote Alarm Time Slot 16 Status Change**

A change in the remote alarm bit in CAS multiframe alignment word is detected.

RSN **Receive Slip Negative**

The frequency of the receive route clock is greater than the frequency of the receive system interface working clock based on 2.048 MHz. A frame is skipped. It is set during alarm simulation.

RSP **Receive Slip Positive**

The frequency of the receive route clock is less than the frequency of the receive system interface working clock based on 2.048 MHz. A frame is repeated. It is set during alarm simulation.

Interrupt Status Register 4 (Read)

	7							0	
ISR4	XSP	XSN							(x6C)

All bits are reset when ISR4 is read.

If bit GCR.VIS is set, interrupt statuses in ISR4 are flagged although they are masked by register IMR4. However, these masked interrupt statuses neither generate a signal on INT, nor are visible in register GIS.

XSP **Transmit Slip Positive**

The frequency of the transmit clock is less than the frequency of the transmit system interface working clock based on 2.048 MHz. A frame is repeated. After a slip has performed writing of register XC1 is not necessary.

XSN **Transmit Slip Negative**

The frequency of the transmit clock is greater than the frequency of the transmit system interface working clock based on 2.048 MHz. A frame is skipped. After a slip has performed writing of register XC1 is not necessary.

Global Interrupt Status Register (Read)

Value after reset: 00_H

	7							0	
GIS				ISR4	ISR3	ISR2	ISR1	ISR0	(x6E)

This status register points to pending interrupts sourced by ISR(4:0).

Channel Interrupt Status Register (Read)

Value after reset: $x0000000_B$

	7							0	
CIS	PLLL	0	0	0	GIS4	GIS3	GIS2	GIS1	(6F)

This status register points to pending interrupts sourced by the GIS registers of each channel

PLLL: PLL locked status: 1 if PLL is locked, 0 if PLL is unlocked

GIS4 register GIS of channel 4

GIS3 register GIS of channel 3

GIS2 register GIS of channel 2

GIS1 register GIS of channel 1

Undefined bit positions CIS(6:4) shall be ignored.

Receive CAS Register (Read)

Value after reset: not defined

Table 63 Receive CAS Registers (E1)

	7							0	
RS1	0	0	0	0	X	Y	X	X	(x70)
RS2	A1	B1	C1	D1	A16	B16	C16	D16	(x71)
RS3	A2	B2	C2	D2	A17	B17	C17	D17	(x72)
RS4	A3	B3	C3	D3	A18	B18	C18	D18	(x73)
RS5	A4	B4	C4	D4	A19	B19	C19	D19	(x74)
RS6	A5	B5	C5	D5	A20	B20	C20	D20	(x75)
RS7	A6	B6	C6	D6	A21	B21	C21	D21	(x76)
RS8	A7	B7	C7	D7	A22	B22	C22	D22	(x77)
RS9	A8	B8	C8	D8	A23	B23	C23	D23	(x78)
RS10	A9	B9	C9	D9	A24	B24	C24	D24	(x79)
RS11	A10	B10	C10	D10	A25	B25	C25	D25	(x7A)
RS12	A11	B11	C11	D11	A26	B26	C26	D26	(x7B)
RS13	A12	B12	C12	D12	A27	B27	C27	D27	(x7C)
RS14	A13	B13	C13	D13	A28	B28	C28	D28	(x7D)
RS15	A14	B14	C14	D14	A29	B29	C29	D29	(x7E)
RS16	A15	B15	C15	D15	A30	B30	C30	D30	(x7F)

Receive CAS Register (16:1)

Each register except RS1 contains the received CAS bits for two time slots. The received CAS multiframe is compared to the previously received one. If the contents changed a CAS multiframe changed interrupt (ISR0.CASC) is generated and informs the user that a new multiframe has to be read within the next 2 ms. If requests for reading the RS(16:1) register are ignored, the received data is lost. RS1 contains frame 0 of the CAS multiframe. MSB is received first.

Additionally a receive signaling data change pointer indicates an update of register RS(16:1). Refer also to register RSP1/2.
Access to RS(16:1) registers is only valid if the serial receive signaling access on the system highway is disabled.

10 T1/J1 Registers

10.1 T1/J1 Control Register Addresses

Table 64 T1/J1 Control Register Address Arrangement

Address[1)]	Register	Type	Comment	Page
x00	XFIFO	W	Transmit FIFO	320
x01	XFIFO	W	Transmit FIFO	320
x02	CMDR	W	Command Register	321
x03	MODE	R/W	Mode Register	323
x04	RAH1	R/W	Receive Address High 1	324
x05	RAH2	R/W	Receive Address High 2	324
x06	RAL1	R/W	Receive Address Low 1	324
x07	RAL2	R/W	Receive Address Low 2	324
08	IPC	R/W	Interrupt Port Configuration	325
x09	CCR1	R/W	Common Configuration Register 1	325
x0A	CCR2	R/W	Common Configuration Register 2	328
x0C	RTR1	R/W	Receive Time Slot Register 1	329
x0D	RTR2	R/W	Receive Time Slot Register 2	329
x0E	RTR3	R/W	Receive Time Slot Register 3	329
x0F	RTR4	R/W	Receive Time Slot Register 4	329
x10	TTR1	R/W	Transmit Time Slot Register 1	330
x11	TTR2	R/W	Transmit Time Slot Register 2	330
x12	TTR3	R/W	Transmit Time Slot Register 3	330
x13	TTR4	R/W	Transmit Time Slot Register 4	330
x14	IMR0	R/W	Interrupt Mask Register 0	331
x15	IMR1	R/W	Interrupt Mask Register 1	331
x16	IMR2	R/W	Interrupt Mask Register 2	331
x17	IMR3	R/W	Interrupt Mask Register 3	331
x18	IMR4	R/W	Interrupt Mask Register 4	331
x1B	IERR	R/W	Single Bit Error Insertion Register	332
x1C	FMR0	R/W	Framer Mode Register 0	332
x1D	FMR1	R/W	Framer Mode Register 1	334

Table 64 T1/J1 Control Register Address Arrangement (cont'd)

Address[1)]	Register	Type	Comment	Page
x1E	FMR2	R/W	Framer Mode Register 2	337
x1F	LOOP	R/W	Channel Loop Back	339
x20	FMR4	R/W	Framer Mode Register 4	340
x21	FMR5	R/W	Framer Mode Register 5	342
x22	XC0	R/W	Transmit Control 0	343
x23	XC1	R/W	Transmit Control 1	344
x24	RC0	R/W	Receive Control 0	345
x25	RC1	R/W	Receive Control 1	347
x26	XPM0	R/W	Transmit Pulse Mask 0	349
x27	XPM1	R/W	Transmit Pulse Mask 1	349
x28	XPM2	R/W	Transmit Pulse Mask 2	349
x2B	IDLE	R/W	Idle Channel Code	351
x2C	XDL1	R/W	Transmit DL-Bit Register 1	351
x2D	XDL2	R/W	Transmit DL-Bit Register 2	351
x2E	XDL3	R/W	Transmit DL-Bit Register 3	351
x2F	CCB1	R/W	Clear Channel Register 1	352
x30	CCB2	R/W	Clear Channel Register 2	352
x31	CCB3	R/W	Clear Channel Register 3	352
x32	ICB1	R/W	Idle Channel Register 1	352
x33	ICB2	R/W	Idle Channel Register 2	352
x34	ICB3	R/W	Idle Channel Register 3	352
x36	LIM0	R/W	Line Interface Mode 0	353
x37	LIM1	R/W	Line Interface Mode 1	355
x38	PCD	R/W	Pulse Count Detection	357
x39	PCR	R/W	Pulse Count Recovery	357
x3A	LIM2	R/W	Line Interface Register 2	358
x3B	LCR1	R/W	Loop Code Register 1	360
x3C	LCR2	R/W	Loop Code Register 2	361
x3D	LCR3	R/W	Loop Code Register 3	362
x3E	SIC1	R/W	System Interface Control 1	362

Table 64 T1/J1 Control Register Address Arrangement (cont'd)

Address[1)]	Register	Type	Comment	Page
x3F	SIC2	R/W	System Interface Control 2	364
x40	SIC3	R/W	System Interface Control 3	366
x44	CMR1	R/W	Clock Mode Register 1	368
x45	CMR2	R/W	Clock Mode Register 2	370
x46	GCR	R/W	Global Configuration Register 1	372
x47	ESM	R/W	Errored Second Mask	373
x60	DEC	W	Disable Error Counter	373
x70	XS1	W	Transmit Signaling Register 1	374
x71	XS2	W	Transmit Signaling Register 2	374
x72	XS3	W	Transmit Signaling Register 3	374
x73	XS4	W	Transmit Signaling Register 4	374
x74	XS5	W	Transmit Signaling Register 5	374
x75	XS6	W	Transmit Signaling Register 6	374
x76	XS7	W	Transmit Signaling Register 7	374
x77	XS8	W	Transmit Signaling Register 8	374
x78	XS9	W	Transmit Signaling Register 9	374
x79	XS10	W	Transmit Signaling Register 10	374
x7A	XS11	W	Transmit Signaling Register 11	374
x7B	XS12	W	Transmit Signaling Register 12	374
x80	PC1	R/W	Port Configuration 1	375
x81	PC2	R/W	Port Configuration 2	375
x82	PC3	R/W	Port Configuration 3	375
x83	PC4	R/W	Port Configuration 4	375
x84	PC5	R/W	Port Configuration 5	377
85	GPC1	R/W	Global Port Configuration 1	378
x87	CMDR2	W	Command Register 2	381
x8D	CCR5	R/W	Common Control Register 5	381
92	GCM1	R/W	Global Counter Mode 1	383
93	GCM2	R/W	Global Counter Mode 2	383
94	GCM3	R/W	Global Counter Mode 3	383

Table 64 T1/J1 Control Register Address Arrangement (cont'd)

Address[1)]	Register	Type	Comment	Page
95	GCM4	R/W	Global Counter Mode 4	384
96	GCM5	R/W	Global Counter Mode 5	384
97	GCM6	R/W	Global Counter Mode 6	384
98	GCM7	R/W	Global Counter Mode 7	385
99	GCM8	R/W	Global Counter Mode 8	385
xA0	TSEO	R/W	Time Slot Even/Odd Select	388
xA1	TSBS1	R/W	Time Slot Bit Select 1	388
xA8	TPC0	R/W	Test Pattern Control Register 0	389

1) x = 0: channel 1 register; x = 1: channel 2 register; x = 2: channel 3 register; x = 3: channel 4 register

After reset all control registers except the XFIFO and XS(12:1) are initialized to defined values.

Unused bits have to be cleared.

10.2 Detailed Description of T1/J1 Control Registers

Transmit FIFO (Write)

	7		0	
XFIFO	XF7		XF0	(x00)
XFIFO	XF15		XF8	(x01)

Writing data to XFIFO can be done in 8-bit (byte) or 16-bit (word) access. The LSB is transmitted first.

Up to 32 bytes/16 words of transmit data can be written to the XFIFO following an XPR interrupt.

Command Register (Write)

Value after reset: 00_H

	7							0	
CMDR	RMC	RRES	XREP	XRES	XHF	XTF	XME	SRES	(x02)

RMC **Receive Message Complete**

Confirmation from CPU to QuadFALC that the current frame or data block has been fetched following an RPF or RME interrupt, thus the occupied space in the RFIFO can be released. If RMC is given while RFIFO is already cleared, the next incoming data block is cleared instantly, although interrupts are generated.

RRES **Receiver Reset**

The receive line interface except the clock and data recovery unit (DPLL), the receive framer, the one second timer and the receive signaling controller are reset. However the contents of the control registers is not deleted.

XREP **Transmission Repeat**

If XREP is set together with XTF (write 24H to CMDR), the QuadFALC repeatedly transmits the contents of the XFIFO (1 to 32 bytes) without HDLC framing fully transparently, i.e. without flag, CRC.

The cyclic transmission is stopped with an SRES command or by resetting XREP.

Note: During cyclic transmission the XREP-bit has to be set with every write operation to CMDR.

XRES **Transmitter Reset**

The transmit framer and transmit line interface excluding the system clock generator and the pulse shaper are reset. However the contents of the control registers is not deleted.

XHF **Transmit HDLC Frame**

After having written up to 32 bytes to the XFIFO, this command initiates the transmission of a HDLC frame.

XTF **Transmit Transparent Frame**

Initiates the transmission of a transparent frame without HDLC framing.

XME **Transmit Message End**

Indicates that the data block written last to the transmit FIFO completes the current frame. The QuadFALC can terminate the transmission operation properly by appending the CRC and the closing flag sequence to the data.

SRES **Signaling Transmitter Reset**

The transmitter of the signaling controller is reset. XFIFO is cleared of any data and an abort sequence (seven 1s) followed by interframe time fill is transmitted. In response to SRES an XPR interrupt is generated.

This command can be used by the CPU to abort a frame currently in transmission.

Note: The maximum time between writing to the CMDR register and the execution of the command takes 2.5 periods of the current system data rate. Therefore, if the CPU operates with a very high clock rate in comparison with the QuadFALC's clock, it is recommended that bit SIS.CEC should be checked before writing to the CMDR register to avoid any loss of commands.

Note: If SCLKX is used to clock the transmission path, commands to the HDLC transmitter should only be sent while this clock is available. If SCLKX is missing, the command register is blocked after an HDLC command is given.

Mode Register (Read/Write)

Value after reset: 00_H

	7							0	
MODE	MDS2	MDS1	MDS0	BRAC	HRAC	DIV			(x03)

MDS(2:0) **Mode Select**

The operating mode of the HDLC controller is selected.

000 Reserved
001 Signaling System 7 (SS7) support[1)]
010 1 byte address comparison mode (RAL1, 2)
011 2 byte address comparison mode (RAH1, 2 and RAL1, 2)
100 No address comparison
101 1 byte address comparison mode (RAH1, 2)
110 Reserved
111 No HDLC framing mode 1

BRAC **BOM Receiver Active**

Switches the BOM receiver to operational or inoperational state.

0 Receiver inactive
1 Receiver active

HRAC **Receiver Active**

Switches the HDLC receiver to operational or inoperational state.

0 Receiver inactive
1 Receiver active

DIV **Data Inversion**

Setting this bit inverts the internal generated HDLC data stream.

0 normal operation, HDLC data stream not inverted
1 HDLC data stream inverted

1) CCR2.RADD must be set, if SS7 mode is selected

Receive Address Byte High Register 1 (Read/Write)
Value after reset: FD_H

	7	1	0	
RAH1		0		(x04)

In operating modes that provide high byte address recognition, the high byte of the received address is compared to the individually programmable values in RAH1 and RAH2.

RAH1 **Value of the First Individual High Address Byte**

Bit 1 (C/R-bit) is excluded from address comparison.

Receive Address Byte High Register 2 (Read/Write)
Value after reset: FF_H

	7	0	
RAH2			(x05)

RAH2 **Value of Second Individual High Address Byte**

Receive Address Byte Low Register 1 (Read/Write)
Value after reset: FF_H

	7	0	
RAL1			(x06)

RAL1 **Value of First Individual Low Address Byte**

Receive Address Byte Low Register 2 (Read/Write)
Value after reset: FF_H

	7	0	
RAL2			(x07)

RAL2 **Value of the second individually programmable low address byte.**

Interrupt Port Configuration (Read/Write)

Value after reset: 00_H

	7							0	
IPC						SSYF	IC1	IC0	(08)

Unused bits have to be cleared.

SSYF **Select SYNC Frequency**

Only applicable in master mode (LIM0.MAS = 1) and bit CMR2.DCF is cleared.

0 Reference clock at port SYNC is 1.544/2.048 MHz (see LIM1.DCOC)
1 Reference clock at port SYNC is 8 kHz

IC0, IC1 **Interrupt Port Configuration**

These bits define the function of the interrupt output stage (pin INT):

IC1	IC0	Function
X	0	Open drain output
0	1	Push/pull output, active low
1	1	Push/pull output, active high

Common Configuration Register 1 (Read/Write)

Value after reset: 00_H

	7							0	
CCR1		BRM	EDLX	EITS	ITF	XMFA	RFT1	RFT0	(x09)

BRM **BOM Receive Mode** (significant in BOM mode only)

0 10 byte packets
1 Continuous reception

EDLX **Enable DL-Bit Access through the Transmit FIFO**

A one in this bit position enables the internal DL-bit access through the receive/transmit FIFO of the signaling controller. FMR1.EDL has to be cleared.

EITS **Enable Internal Time Slot (31:0) Signaling**

0 Internal signaling in time slots (31:0) defined by registers RTR(4:1) or TTR(4:1) is disabled.

1 Internal signaling in time slots (31:0) defined by registers RTR(4:1) or TTR(4:1) is enabled.

ITF **Interframe Time Fill**

Determines the idle (= no data to be sent) state of the transmit data coming from the signaling controller.

0 Continuous logical 1 is output

1 Continuous flag sequences are output (01111110 bit patterns)

XMFA **Transmit Multiframe Aligned**

Determines the synchronization between the framer and the corresponding signaling controller.

0 The contents of the XFIFO is transmitted without multiframe alignment.

1 The contents of the XFIFO is transmitted multiframe aligned. If CCR1.EDLXis set, transmission of DL-bits is started in F72 format with frame 26. The first byte in XFIFO is transmitted in the first time slot selected by TTR(4:1) and so on.
After receiving a complete multiframe in the time slot mode (RTR(4:1)) an ISR0.RME interrupt is generated, if no HDLC or BOM mode is enabled. In DL-bit access (CCR1.EDLX/ EITS = 10) XMFA is not valid.

Note: During the transmission of the XFIFO content, the $\overline{SYPX}$ or XMFS interval time should not be changed, otherwise the XFIFO data has to be retransmitted.

RFT(1:0) **RFIFO Threshold Level**

The size of the accessible part of RFIFO can be determined by programming these bits. The number of valid bytes after an RPF interrupt is given in the following table:

RFT1	RFT0	Size of Accessible Part of RFIFO
0	0	32 bytes (reset value)
0	1	16 bytes
1	0	4 bytes
1	1	2 bytes

The value of RFT 1,0 can be changed dynamically

– If reception is not running or

– after the current data block has been read, but before the command CMDR.RMC is issued (interrupt controlled data transfer).

*Note: It is seen that changing the value of RFT1,0 is possible even during the reception of one frame. The total length of the received frame can be always read directly in RBCL, RBCH after an RPF interrupt, except when the threshold is increased during reception of that frame. The real length can then be inferred by noting which bit positions in RBCL are reset by an RMC command (see **table below**):*

RFT1	RFT0	Bit Positions in RBCL Reset by a CMDR.RMC Command
0	0	RBC(4:0)
0	1	RBC(3:0)
1	0	RBC(1:0)
1	1	RBC0

Common Configuration Register 2 (Read/Write)

Value after reset: 00_H

	7							0	
CCR2				RADD	RBFE	RCRC	XCRC		(x0A)

Unused bits have to be cleared.

RADD **Receive Address Pushed to RFIFO**

If this bit is set, the received HDLC address information (1 or 2 bytes, depending on the address mode selected by MODE.MDS0) is pushed to RFIFO. This function is applicable in non-auto mode and transparent mode 1. RADD must be set, if SS7 mode is selected.

RBFE **Receive BOM Filter Enable**

Setting this bit the bit oriented message (BOM) receiver only accepts BOM frames after detecting 7 out of 10 equal BOM pattern. The BOM pattern is stored in the RFIFO adding a receive status byte marking a BOM frame (RSIS.HFR) and an interrupt ISR0.RME is generated. The current state of the BOM receiver is indicated in register SIS.IVB. When the valid BOM pattern disappears an interrupt ISR0.BIV is generated.

RCRC **Receive CRC on/off**

Only applicable in non-auto mode.

If this bit is set, the received CRC checksum is written to RFIFO (CRC-ITU-T: 2 bytes). The checksum, consisting of the 2 last bytes in the received frame, is followed in the RFIFO by the status information byte (contents of register RSIS). The received CRC checksum is additionally checked for correctness. If non-auto mode is selected, the limits for “Valid Frame” check are modified (refer to RSIS.VFR).

XCRC **Transmit CRC on/off**

If this bit is set, the CRC checksum is not generated internally. It has to be written as the last two bytes in the transmit FIFO (XFIFO). The transmitted frame is closed automatically with a closing flag.

Note: The QuadFALC does not check whether the length of the frame, i.e. the number of bytes to be transmitted makes sense or not.

Receive Time Slot Register (4:1) (Read/Write)

Value after reset: 00_H, 00_H, 00_H, 00_H

	7							0	
RTR1	TS0	TS1	TS2	TS3	TS4	TS5	TS6	TS7	(x0C)
RTR2	TS8	TS9	TS10	TS11	TS12	TS13	TS14	TS15	(x0D)
RTR3	TS16	TS17	TS18	TS19	TS20	TS21	TS22	TS23	(x0E)
RTR4	TS24	TS25	TS26	TS27	TS28	TS29	TS30	TS31	(x0F)

TS(31:0) **Time Slot Register**

These bits define the received time slots on the system highway port RDO to be extracted. Additionally these registers control the RSIGM marker which can be forced high during the corresponding time slots independently of bit CCR1.EITS.
A one in the RTR(4:1) bits samples the corresponding time slot in the RFIFO of the signaling controller, if bit CCR1.EITS is set.

Assignments:

SIC2.SSC2 = 0: (32 time slots/frame)
TS0 → time slot 0,...TS31 → time slot 31
SIC2.SSC2 = 1: (24 time slots/frame)
TS0 → time slot 0,...TS23 → time slot 23

0 The corresponding time slot is not extracted and stored in the RFIFO.

1 The contents of the selected time slot is stored in the RFIFO. Although the idle time slots can be selected. This function is only active, if bits CCR1.EITS is set.
The corresponding time slot is forced high on pin RSIGM.

Transmit Time Slot Register (4:1) (Read/Write)

Value after reset: 00_H, 00_H, 00_H, 00_H

	7							0	
TTR1	TS0	TS1	TS2	TS3	TS4	TS5	TS6	TS7	(x10)
TTR2	TS8	TS9	TS10	TS11	TS12	TS13	TS14	TS15	(x11)
TTR3	TS16	TS17	TS18	TS19	TS20	TS21	TS22	TS23	(x12)
TTR4	TS24	TS25	TS26	TS27	TS28	TS29	TS30	TS31	(x13)

TS(31:0) **Transmit Time Slot Register**

These bits define the transmit time slots on the system highway to be inserted. Additionally these registers control the XSIGM marker which can be forced high during the corresponding time slots independently of bit CCR1.EITS.
A one in the TTR(4:1) bits inserts the corresponding time slot sourced by the XFIFO in the data received on pin XDI, if bit CCR1.EITS is set. If SIC3.TTRF is set and CCR1.EDLX/EITS = 00, insertion of data received on port XSIG is controlled by this registers.

Assignments:
SIC2.SSC2 = 0: (32 time slots/frame)
TS0 → time slot 0,... TS31 → time slot 31
SIC2.SSC2 = 1: (24 time slots/frame)
TS0 → time slot 0,... TS23 → time slot 23

0 The selected time slot is not inserted into the outgoing data stream.

1 The contents of the selected time slot is inserted into the outgoing data stream from XFIFO. This function is only active, if bits CCR1.EITS is set.
The corresponding time slot are forced high on marker pin XSIGM.

Interrupt Mask Register (4:0)

Value after reset: FF_H, FF_H, FF_H, FF_H,FF_H

	7							0	
IMR0	RME	RFS	ISF	RMB	RSC	CRC6	PDEN	RPF	(x14)
IMR1	CASE	RDO	ALLS	XDU	XMB	SUEX	XLSC	XPR	(x15)
IMR2	FAR	LFA	MFAR	LMFA	AIS	LOS	RAR	RA	(x16)
IMR3	ES	SEC			LLBSC		RSN	RSP	(x17)
IMR4	XSP	XSN							(x18)

IMR(4:0) **Interrupt Mask Register**

Each interrupt source can generate an interrupt signal at port INT (characteristics of the output stage are defined by register IPC). A “1” in a bit position of IMR(4:0) sets the mask active for the interrupt status in ISR(4:0). Masked interrupt statuses neither generate a signal on INT, nor are they visible in register GIS. Moreover, they are

– not displayed in the Interrupt Status Register if bit GCR.VIS is cleared

– displayed in the Interrupt Status Register if bit GCR.VIS is set

After reset, all interrupts are **dis**abled.

Single Bit Defect Insertion Register (Read/Write)

Value after reset: 00_H

IERR			IFASE	IMFE	ICRCE	ICASE	IPE	IBV	(x1B)

After setting the corresponding bit, the selected defect is inserted into the transmit data stream at the next possible position. After defect insertion is completed, the bit is reset automatically.

IFASE **Insert single FAS defect**

IMFE **Insert single multiframe defect**

ICRCE **Insert single CRC defect**

ICASE **Insert single CAS defect**

IPE **Insert single PRBS defect**

IBV **Insert bipolar violation**

Note: Except for CRC defects, CRC checksum calculation is done after defect insertion.

Framer Mode Register 0 (Read/Write)

Value after reset: 00_H

	7							0	
FMR0	XC1	XC0	RC1	RC0	FRS	SRAF	EXLS	SIM	(x1C)

XC(1:0) **Transmit Code**

Serial line code for the transmitter, independent of the receiver.

00 NRZ (optical interface)

01 CMI (1T2B+B8ZS), (optical interface)

10 AMI coding with Zero Code Suppression (ZCS, B7-stuffing). Disabling of the ZCS is done by activating the clear channel mode by register CCB(3:1). (ternary or digital interface)

11 B8ZS Code (ternary or digital dual rail interface).

After changing XC1/0, a transmitter software reset is required (CMDR.XRES = 1).

RC(1:0) **Receive Code**

Serial code receiver is independent to the transmitter.

00 NRZ (optical interface)
01 CMI (1T2B+B8ZS), (optical interface)
10 AMI coding with Zero Code Suppression (ZCS, B7-stuffing), (ternary or digital dual rail interface)
11 B8ZS Code (ternary or digital dual rail interface)

After changing RC1/0, a receiver software reset is required (CMDR.RRES = 1).

FRS **Force Resynchronization**

A transition from low to high forces the frame aligner to execute a resynchronization of the pulse frame. In the asynchronous state, a new frame position is assumed at the next candidate if there is one. Otherwise, a new frame search with the meaning of a general reset is started. In the synchronous state this bit has the same meaning as bit FMR0.EXLS except if FMR2.MCSP = 1.

SRAF **Select Remote (Yellow) Alarm Format for F12 and ESF Format**

0 F12: bit2 = 0 in every channel. ESF: pattern “1111 1111 0000 0000…” in data link channel.
1 F12: FS-bit of frame 12. ESF: bit2 = 0 in every channel

EXLS **External Loss Of Frame**

With a low to high transition a new frame search is started. This has the meaning of a general reset of the internal frame alignment unit. Synchronous state is reached only if there is one definite framing candidate. In the case of multiple candidates, the setting of the bit FMR0.FRS forces the receiver to lock onto the next available framing position.

SIM **Alarm Simulation**

Setting/resetting this bit initiates internal error simulation of: AIS (blue alarm), loss of signal (red alarm), loss of frame alignment, remote (yellow) alarm, slip, framing errors, CRC errors, code violations. The error counters FEC, CVC, CEC, EBC are incremented.

The selection of simulated alarms is done by the error simulation counter: FRS2.ESC(2:0) which is incremented with each setting of bit FMR0.SIM. For complete checking of the alarm indications eight simulation steps are necessary (FRS2.ESC(2:0) = 0 after a complete simulation).

SIM has to be held stable at high or low level for at least one receive clock period before changing it again.

Framer Mode Register 1 (Read/Write)
Value after reset: 00_H

	7							0	
FMR1	CTM		EDL	PMOD	CRC	ECM	SSD0	XAIS	(x1D)

CTM **Channel Translation Mode**

0 Channel translation mode 0

1 Channel translation mode 1

The different channel translation modes are described in **Table 31** on **Page 136**.

EDL **Enable DL-Bit Access through Register XDL(3:1)**

Only applicable in F4, F24 or F72 frame format.

0 Normal operation. The DL-bits are taken from system highway or if enabled by CCR1.EDLX from the XFIFO of the signaling controller.

1 DL-bit register access. The DL-bit information are taken from the registers XDL(3:1) and overwrite the DL-bits received on the system highway (pin XDI) or from the internal XFIFO of the signaling controller. However, transmission of the contents of registers XDL(3:1) is disabled if transparent mode is enabled (FMR4.TM).

PMOD **PCM Mode**

For E1 application this bit must be set low. Switching from E1 to T1 or vice versa the device needs up to 20 µs to settle up to the internal clocking.

0 PCM 30 or E1 mode.

1 PCM 24 or T1/J1 mode (see RC0.SJR for T1/J1 selection).

CRC **Enable CRC6**

This bit is only significant when using the ESF format.

0 CRC6 check/generation disabled. For transmit direction, all CRC bit positions are set.

1 CRC6 check/generation enabled.

ECM **Error Counter Mode**

The function of the error counters (FEC,CEC,CVC,EBC) is determined by this bit.

0 Before reading an error counter the corresponding bit in the Disable Error Counter register (DEC) has to be set. In 8 bit access the low byte of the error counter should always be read before the high byte. The error counters are reset with the rising edge of the corresponding bits in the DEC register.

1 Every second the error counter is latched and then automatically reset. The latched error counter state should be read within the next second. Reading the error counter during updating should be avoided (do not access an error counter within 1 µs after the one-second interrupt occurs).

SSD0 **Select System Date Rate 0**

SIC1.SSD1, FMR1.SSD0 and SIC2.SSC2 define the data rate on the system highway. Programming SSD1/SSD0 and corresponding data rate is shown below.

SIC2.SSC2 = 0:

00 2.048 Mbit/s

01 4.096 Mbit/s

10 8.192 Mbit/s

11 16.384 Mbit/s

SIC2.SSC2 = 1:

00 1.544 Mbit/s

01 3.088 Mbit/s

10 6.176 Mbit/s

11 12.352 Mbit/s

XAIS **Transmit AIS Towards Remote End**

Sends AIS (blue alarm) on ports XL1, XL2 towards the remote end.

If Local Loop Mode is enabled the transmitted data is looped back to the system internal highway without any changes.

Framer Mode Register 2 (Read/Write)

Value after reset: 00_H

	7							0	
FMR2	AFRS	MCSP	SSP	DAIS	SAIS	PLB	AXRA	EXZE	(x1E)

AFRS **Automatic Force Resynchronization**

Search for next candidate automatically, if multiple candidates are present and the current candidate is incorrect.

MCSP **Multiple Candidates Synchronization Procedure**

SSP **Select Synchronization/Resynchronization Procedure**

Together with bit FMR2.SSP the synchronization mode of the receive framer is defined:

MCSP/SSP:

00 F12/F72 format:
Specified number of errors in both FT framing and FS framing lead to loss of sync (FRS0.LFA is set). In the case of FS-bit framing errors, bit FRS0.LMFA is set additionally. A complete new synchronization procedure is initiated to regain pulseframe alignment and then multiframe alignment.

F24:
normal operation: synchronization is achieved only on verification the framing pattern.

01 F12/F72:
Specified number of errors in FT framing has the same effect as above. Specified number of errors in FS framing only initiates a new search for multiframe alignment without influencing pulseframe synchronous state (FRS0.LMFA is set).

F24:
Synchronous state is reached when three consecutive multiframe pattern are correctly found independent of the occurrence of CRC6 errors.

10 F12/F24:
A one enables a synchronization mode which is able to choose multiple framing pattern candidates step by step. I.e. if in synchronous state the CRC error counter indicates that the synchronization might have been based on an alias framing pattern, setting of FMR0.FRS leads to synchronization on the next candidate available. However,

only the previously assumed candidate is discarded in the internal framing pattern memory. The latter procedure can be repeated until the framer locks on the right pattern (no extensive CRC errors). Therefore bit FMR1.CRC must be set.

11 F24:
Synchronization is achieved on verification the framing pattern **and** the CRC6 bits. Synchronous state is reached when framing pattern and CRC6 checksum are correctly found. For correct operation the CRC check must be enabled by setting bit FMR1.CRC.

DAIS **Disable AIS to System Interface**

0 AIS is automatically inserted into the data stream to RDO if QuadFALC is in asynchronous state.

1 Automatic AIS insertion is disabled. Furthermore, AIS insertion can be initiated by programming bit FMR2.SAIS.

SAIS **Send AIS Towards System Interface**

Sends AIS (blue alarm) on output RDO towards system interface. This function is not influenced by bit FMR2.DAIS.

PLB **Payload Loop Back**

0 Normal operation. Payload loop is disabled.

1 The payload loopback loops the data stream from the receiver section back to transmitter section. Looped data is output on pin RDO. Data received on port XDI, XSIG, $\overline{\text{SYPX}}$ and XMFS is ignored. With FMR4.TM = 1 all 193 bits per frame are looped back. If FMR4.TM = 0 the DL- or FS- or CRC-bits are generated internally. AIS is sent immediately on port RDO by setting the FMR2.SAIS bit. During payload loop is active the receive time slot offset (registers RC1/0) should not be changed. It is recommended to write the actual value of XC1 into this register once again, because a write access to register XC1 sets the read/write pointer of the transmit elastic buffer into its optimal position to ensure a maximum wander compensation (the write operation forces a slip).

AXRA **Automatic Transmit Remote Alarm**

0 Normal operation

1 The remote alarm (yellow alarm) bit is set automatically in the outgoing data stream if the receiver is in asynchronous state (FRS0.LFA bit is set). In synchronous state the remote alarm bit is reset.

EXZE **Excessive Zeros Detection Enable**

Selects error detection mode in the bipolar receive bit stream.

0 Only bipolar violations are detected.

1 Bipolar violations and zero strings of 8 or more contiguous zeros in B8ZS code or more than 15 contiguous zeros in AMI code are detected additionally and counted in the code violation counter CVC.

LOOP (Read/Write)

Value after reset: 00_H

	7							0	
LOOP		RTM	ECLB	CLA4	CLA3	CLA2	CLA1	CLA0	(x1F)

RTM **Receive Transparent Mode**

Setting this bit disconnects control of the internal elastic store from the receiver. The elastic store is now in a “free running” mode without any possibility to actualize the time slot assignment to a new frame position in case of resynchronization of the receiver. This function can be used together with the “disable AIS to system interface” feature (FMR2.DAIS) to realize undisturbed transparent reception.
This bit should be enabled in case of unframed data reception mode.

ECLB **Enable Channel Loop Back**

0 Disables the channel loop back.

1 Enables the channel loop back selected by this register.

CAS-BR must be switched off (FMR5.EIBR = 0) while channel loop back is enabled.

CLA(4:0) **Channel Address For Loop Back**

CLA = 1 to 24 selects the channel.

During loop back, the contents of the associated outgoing channel at ports XL1/XDOP/XOID and XL2/XDON is equal to the idle channel code programmed in register IDLE.

Framer Mode Register 4 (Read/Write)

Value after reset: 00_H

	7							0	
FMR4	AIS3	TM	XRA	SSC1	SSC0	AUTO	FM1	FM0	(x20)

AIS3 **Select AIS Condition**

0 AIS (blue alarm) is indicated (FRS0.AIS) when two or less zeros in the received bit stream are detected in a time interval of 12 frames (F4, F12, F72) or 24 frames (ESF).

1 AIS (blue alarm) detection is only enabled when QuadFALC is in asynchronous state. The alarm is indicated (FRS0.AIS) when

– three or less zeros within a time interval of 12 frames (F4, F12, F72), or

– five or less zeros within a time interval of 24 frames (ESF)
are detected in the received bit stream.

TM **Transparent Mode**

Setting this bit enables the transparent mode:

In transmit direction bit 8 of every FS/DL time slot from the system internal highway (XDI) is inserted in the F-bit position of the outgoing frame. Internal framing generation, insertion of CRC and DL data is disabled.

XRA **Transmit Remote Alarm (Yellow Alarm)**

If high, remote alarm is sent on the PCM route. Clearing the bit removes the remote alarm pattern. Remote alarm indication depends on the multiframe structure as follows:

F4: bit2 = 0 in every speech channel
F12:– FMR0.SRAF = 0: bit2 = 0 in every speech channel
– FMR0.SRAF = 1: FS-bit of frame 12 is forced to “1”
ESF:– FMR0.SRAF = 0: pattern
“1111111100000000 11111111000…”
in data link channel
– FMR0.SRAF = 1: bit2 = 0 in every speech channel
F72:bit2 = 0 in every speech channel

SSC(1:0) **Select Sync Conditions**

Loss of Frame Alignment (FRS0.LFA or opt. FRS0.LMFA) is declared if:
00 = 2 out of 4 framing bits
01 = 2 out of 5 framing bits
10 = 2 out of 6 framing bits in F4/12/72 format
10 = 2 out of 6 framing bits per multiframe period in ESF format
11 = 4 consecutive multiframe pattern in ESF format
are incorrect. It depends on the selected multiframe format and optionally on bit FMR2.SSP which framing bits are observed:

F4:FT-bits → FRS0.LFA
F12, F72:SSP = 0:
FT-bits→ FRS0.LFA
FS-bits → FRS0.LFA and FRS0.LMFA
F12, F72:SSP = 1:
FT → FRS0.LFA
FS → FRS0.LMFA
ESF: ESF framing bits → FRS0.LFA

AUTO **Enable Auto Resynchronization**

0 The receiver does not resynchronize automatically. Starting a new synchronization procedure is possible by the bits FMR0.EXLS or FMR0.FRS.

1 Auto-resynchronization is enabled.

FM(1:0) **Select Frame Mode**

FM = 0: 12-frame multiframe format (F12, D3/4)
FM = 1: 4-frame multiframe format (F4)
FM = 2: 24-frame multiframe format (ESF)
FM = 3: 72-frame multiframe format (F72, remote switch mode)

Framer Mode Register 5 (Read/Write)

Value after reset: 00_H

	7							0	
FMR5		EIBR	XLD	XLU		XTM	SSC2		(x21)

EIBR **Enable Internal Bit Robbing Access**

0 Normal operation.

1 A one in this bit position causes the transmitter to send the bit robbing signaling information stored in the XS(12:1) (ESF, F12, 72) registers or serial CAS in the corresponding time slots.

XLD **Transmit Line Loopback (LLB) Down Code**

0 Normal operation.

1 A one in this bit position causes the transmitter to replace normal transmit data with the LLB down (deactivate) Code continuously until this bit is reset. The LLB down code is overwritten by the framing/DL/CRC bits optionally.

XLU **Transmit LLB UP Code**

0 Normal operation.

1 A one in this bit position causes the transmitter to replace normal transmit data with the LLB up (activate) code continuously until this bit is reset. The LLB up code is optionally overwritten by the framing/DL/CRC bits. For proper operation bit FMR5.XLD must be cleared.

XTM **Transmit Transparent Mode**

0 Ports $\overline{\text{SYPX}}$/XMFS define the frame/multiframe begin on the transmit system highway. The transmitter is usually synchronized on this externally sourced frame boundary and generates the FS/DL-bits according to this framing. Any change of the transmit time slot assignment subsequently produces a change of the FS/DL-bit positions.

1 Disconnects the control of the transmit system interface from the transmitter. The transmitter is now in a free running mode without any possibility to actualize the multiframe position. The framing (FS/DL-bits) generated by the transmitter are not “disturbed“ (in case of changing the transmit time slot assignment) by the transmit system highway unless register XC1 is written. This bit should be set if loop-

timed application is selected. For proper operation the transmit elastic buffer (2 frames, SIC1.XBS1/0 = 10) has to be enabled.

SSC2 **Select Sync Conditions**

Only valid in ESF framing format.
Loss of Frame Alignment FRS0.LFA is declared if more than 320 CRC6 errors per second interval are detected.

Transmit Control 0 (Read/Write)

Value after reset: 00_H

	7							0	
XC0	BRM	MFBS			BRFO	XCO10	XCO9	XCO8	(x22)

BRM **Enable Bit Robbing Marker**

A one in this bit marks the robbed bit positions on the system highway. RSIGM marks the receive and XSIGM marks the transmit robbed bits.

MFBS **Enable pure Multiframe Begin Signals**

Only valid if ESF or F72 format is selected.

0 RMFB marks the beginning of every received superframe. Additional pulses are provided every 12 frames when using ESF/F24 or F72 format.

1 RMFB marks the beginning of every received multiframe.

BRFO **Bit Robbing Force One**

Setting this bit forces the robbed bits high transmitted on port RDO. The received signaling data stream for the signaling controller is not influenced by this bit.

XCO(10:8) **Transmit Offset**

Initial value loaded into the transmit bit counter at the trigger edge of SCLKX when the synchronous pulse at port $\overline{\text{SYPX}}$ or XMFS is active Refer to register XC1.

Transmit Control 1 (Read/Write)

Value after reset: $9C_H$

	7	0	
XC1	XCO7	XCO0	(x23)

A write access to this address resets the transmit elastic buffer to its basic starting position. Therefore, updating the value should only be done when the QuadFALC is initialized or when the buffer should be centered. As a consequence a transmit slip will occur.

XCO(7:0) **Transmit Offset**

Initial value loaded into the transmit bit counter at the trigger edge of SCLKX when the synchronous pulse at port $\overline{\text{SYPX}}$/XMFS is active.

Calculation of delay time T (SCLKX cycles) depends on the value X of the 'Transmit Offset" register XC1/0:

system clocking rate: modulo 2.048 MHz (SIC2.SSC2 = 0)
$0 \leq T \leq 4$: X = 4 - T
$5 \leq T \leq$ maximum delay:X = 256 $\times$ SC/SD - T + 4

with maximum delay = (256 $\times$ SC/SD) -1
with SC = system clock defined by SIC1.SSC1/0+SIC2.SSC2
with SD = 2.048 Mbit/s

or

system clocking rate: modulo 1.544 MHz (SIC2.SSC2 = 1)
$0 \leq T \leq 4$: X = 4 - T + 7 $\times$ SC/SD
$5 \leq T \leq$ maximum delay:X = 200 $\times$ SC/SD - T + 4

with maximum delay = (200$\times$SC/SD) - (7*SC/SD) -1
with SC = system clock defined by SIC1.SSC1/0+SIC2.SSC2
with SD = 1.544 Mbit/s

Delay time T = time between beginning of time slot 0 (bit 0, channel phase 0) at XDI/XSIG and the initial edge of SCLKX after $\overline{\text{SYPX}}$/XMFS goes active.

See **page 183** for further description.

Receive Control 0 (Read/Write)

Value after reset: 00_H

	7							0	
RC0	SJR	RRAM	CRCI	XCRCI	RDIS	RCO10	RCO9	RCO8	(x24)

SJR **Select Japanese ITU-T Requirements**

0 T1: Alarm handling is done according ITU-T G. 704+706

1 J1: Alarm handling is done according ITU-T JG. 704+706

RRAM **Receive Remote Alarm Mode**

The conditions for remote (yellow) alarm (FRS0.RRA) detection can be selected by this bit to allow detection even in the presence of a bit error rate of up to 10^{-3}:

RRAM = 0

Detection

F4: bit2 = 0 in every speech channel per frame.

F12: – FMR0.SRAF = 0: bit2 = 0 in every speech channel per frame.

– FMR0.SRAF = 1: S-bit of frame 12 is forced to “1”

ESF: – FMR0.SRAF = 0: pattern “1111 1111 0000 0000…” in data link channel

– FMR0.SRAF = 1: bit2 = 0 in every speech channel

F72:bit2 = 0 in every speech channel per frame.

Release: The alarm is reset when above conditions are no longer detected.

RRAM = 1 (bit error rate 10^{-3})

Detection

F4:bit2 = 0 in 255 consecutive speech channels.

F12:– FMR0.SRAF = 0: bit 2 = 0 in 255 consecutive speech channels.

– FMR0.SRAF = 1: S-bit of frame 12 is forced to “1”

ESF:– FMR0.SRAF = 0: pattern “1111 1111 0000 0000…” in data link channel

– FMR0.SRAF = 1: bit 2 = 0 in 255 consecutive speech channels

F72: bit 2 = 0 in 255 consecutive speech channels.

Release

Depending on the selected multiframe format the alarm is reset when QuadFALC does not detect

– the “bit 2 = 0’ condition for three consecutive pulse frames (all formats if selected),
– the ’FS-bit’ condition for three consecutive multiframes (F12),
– the ’DL pattern’ for three times in a row (ESF).

CRCI **Automatic CRC6 Bit Inversion**

If set, all CRC bits of one outgoing extended multiframe are inverted in case a CRC error is flagged for the previous received multiframe. This function is logically ored with RC0.XCRCI.

XCRCI **Transmit CRC6 Bit Inversion**

If set, the CRC bits in the outgoing data stream are inverted before transmission. This function is logically ored with RC0.CRCI.

RDIS **Receive Data Input Sense**

Digital interface, dual rail:

0 Inputs RDIP/RDIN are active low

1 Inputs RDIP/RDIN are active high

Digital Interface, CMI:

0 Input ROID is active high

1 Input ROID is active low

RCO(10:8) **Receive Offset/Receive Frame Marker Offset**

Depending on the RP(A to D) pin function different offsets can be programmed. The $\overline{\text{SYPR}}$ and the RFM pin function can not be selected in parallel.

Receive Offset (PC(4:1).RPC(2:0) = 000)
Initial value loaded into the receive bit counter at the trigger edge of SCLKR when the synchronous pulse at port $\overline{\text{SYPR}}$ is active.

Calculation of delay time T (SCLKR cycles) depends on the value X of the ’Receive Offset“ register RC1/0. Refer to register RC1.

Receive Control 1 (Read/Write)

Value after reset: $9C_H$

	7			0	
RC1	RCO7		RCO5	RCO0	(x25)

RCO(7:0) **Receive Offset/Receive Frame Marker Offset**

Depending on the RP(A to D) pin function different offsets can be programmed. The $\overline{\text{SYPR}}$ and the RFM pin function can not be selected in parallel.

Receive Offset (PC(4:1).RPC(2:0) = 000)
Initial value loaded into the receive bit counter at the trigger edge of SCLKR when the synchronous pulse at port $\overline{\text{SYPR}}$ is active.

Calculation of delay time T (SCLKR cycles) depends on the value X of the 'Receive Offset" register RC1/0:

system clocking rate: modulo 2.048 MHz (SIC2.SSC2 = 0)
$0 \leq T \leq 4$:X = 4 - T
$5 \leq T \leq$ maximum delay:X = 2052 - T

with maximum delay = (256×SC/SD) -1
with SC = system clock defined by SIC1.SSC1/0+SIC2.SSC2
with SD = system data rate
or

system clocking rate: modulo 1.544 MHz (SIC2.SSC2 = 1)
$0 \leq T \leq 4$:X = 4 - T + (7 × SC/SD)
$5 \leq T \leq$ maximum delay :X = (200 × SC/SD) + 4 - T

with maximum delay = 193×SC/SD - 1
with SC = system clock defined by SIC1.SSC1/0+SIC2.SSC2
with SD = system data rate
Delay time T = time between beginning of time slot 0 at RDO and the initial edge of SCLKR after $\overline{\text{SYPR}}$ goes active.

See **page 173** for further description.

Receive Frame Marker Offset (PC(4:1).RPC(2:0) = 001)

Offset programming of the receive frame marker which is output on multifunction port RFM. The receive frame marker can be activated during any bit position of the entire frame and depends on the selected system clock rate.

Calculation of the value X of the 'Receive Offset" register RC1/0 depends on the bit position which should be marked at marker position MP:

system clocking rate: modulo 2.048 MHz (SIC2.SSC2 = 0)
0 ≤ MP ≤ 2045:X = MP + 2
2046 ≤ MP ≤ 2047:X = MP - 2046

e.g: 2.048 MHz: MP = 0 to 255; 4.096 MHz: MP = 0 to 511,
8.192 MHz: MP = 0 to 1023, 16.384 MHz: MP = 0 to 2047

system clocking rate: modulo 1.544 MHz (SIC2.SSC2 = 1)
0 ≤ MP ≤ 193 × (SC/SD) - 3:X = MP + 2 + 7 × SC/SD
193 × (SC/SD) -2 ≤ MP ≤ maximum delay:X = MP + 2 - 186 × SC/SD

with maximum delay = 193 × SC/SD - 1
with SC = system clock defined by SIC1.SSC1/0+SIC2.SSC2
with SD = system data rate

Transmit Pulse-Mask (2:0) (Read/Write)

Value after reset: $7B_H$, 03_H, 40_H

	7							0	
XPM0	XP12	XP11	XP10	XP04	XP03	XP02	XP01	XP00	(x26)
XPM1	XP30	XP24	XP23	XP22	XP21	XP20	XP14	XP13	(x27)
XPM2	0	XLT	DAXLT	0	XP34	XP33	XP32	XP31	(x28)

The transmit pulse shape which is defined in ANSI T1.102 is output on pins XL1 and XL2. The level of the pulse shape can be programmed by registers XPM(2:0) to create a custom waveform. In order to get an optimized pulse shape for the external transformers each pulse shape is internally divided into four sub pulse shapes. In each sub pulse shape a programmed 5 bit value defines the level of the analog voltage on pins XL1/2. Together four 5 bit values have to be programmed to form one complete transmit pulse shape.The four 5 bit values are sent in the following sequence:

XP0(4:0): First pulse shape level
XP1(4:0): Second pulse shape level
XP2(4:0): Third pulse shape level
XP3(4:0): Fourth pulse shape level

Changing the LSB of each subpulse in registers XPM(2:0) changes the amplitude of the differential voltage on XL1/2 by approximately 80 mV.
The XPM values in the following table are based on simulations. They are valid for the following external circuitry: transformer ratio 1:2.4, cable PULB 22AWG (100Ω), serial resistors 2Ω. Adjustment of these coefficients can be necessary for other external conditions.

Table 65 Pulse Shaper Programming (T1/J1)[1)]

Range in m	Range in ft.	XPM0	XPM1	XPM2	XP04-XP00	XP14-XP10	XP24-XP20	XP34-XP30
		hexadecimal			decimal			
0 to 40	0 to 133	95	16	01	21	20	5	2
40 to 81	133 to 266	B6	9E	01	22	21	7	3
81 to 122	266 to 399	D9	26	01	25	22	9	2
122 to 162	399 to 533	FC	36	01	28	23	13	2
162 to 200	533 to 655	3F	CB	01	31	28	18	3

1) Register values of V1.3 may also be used. For optimum results V2.1 values must be applied

XLT **Transmit Line Tristate**

0 Normal operation

1 Transmit line XL1/XL2 or XDOP/XDON are switched into high impedance state. If this bit is set the transmit line monitor status information is frozen (default value after hardware reset).

DAXLT **Disable Automatic Tristating of XL1/2**

0 Normal operation. If a short is detected on pins XL1/2 the transmit line monitor sets the XL1/2 outputs into a high impedance state.

1 If a short is detected on pins XL1/2, the automatic setting of these pins into a high impedance state (by the XL-monitor) is disabled.

Idle Channel Code Register (Read/Write)

Value after reset: 00_H

	7						0	
IDLE	IDL7						IDL0	(x2B)

IDL(7:0) **Idle Channel Code**

If channel loop back is enabled by programming the register LOOP.ECLB = 1, the contents of the assigned outgoing channel at ports XL1/XL2 or XDOP/XDON is set equal to the idle channel code selected by this register.

Additionally, the specified pattern overwrites the contents of all channels of the outgoing PCM frame selected by the idle channel registers ICB1 to ICB3. IDL7 is transmitted first.

Transmit DL-Bit Register 1-3 (Read/Write)

Value after reset: 00_H, 00_H, 00_H

	7							0	
XDL1	XDL17	XDL16	XDL15	XDL14	XDL13	XDL12	XDL11	XDL10	(x2C)
XDL2	XDL27	XDL26	XDL25	XDL24	XDL23	XDL22	XDL21	XDL20	(x2D)
XDL3	XDL37	XDL36	XDL35	XDL34	XDL33	XDL32	XDL31	XDL30	(x2E)

XDL(3:1) **Transmit FS/DL-Bit Data**

The DL-bit register access is enabled by setting bits FMR1.EDL = 1. With the transmit multiframe begin an interrupt ISR1.XMB is generated and the contents of these registers XDL(3:1) is copied into a shadow register. The contents is subsequently sent out in the data stream of the next outgoing multiframe if no transparent mode is enabled. XDL10 is sent out first.
In F4 frame format only XDL10+XDL11 are transmitted. In F24 frame format XDL10 to 23 are shifted out. In F72 frame format XDL10 to 37 are transmitted.
The transmit multiframe begin interrupt (XMB) requests that these registers should be serviced. If requests for new information are ignored, the current contents is repeated.

Clear Channel Register (Read/Write)

Value after reset: 00_H, 00_H, 00_H

	7							0	
CCB1	CH1	CH2	CH3	CH4	CH5	CH6	CH7	CH8	(x2F)
CCB2	CH9	CH10	CH11	CH12	CH13	CH14	CH15	CH16	(x30)
CCB3	CH17	CH18	CH19	CH20	CH21	CH22	CH23	CH24	(x31)

CH(24:1) **Channel Selection Bits**

0 Normal operation. Bit robbing information and zero code suppression (ZCS, B7 stuffing) can change contents of the selected speech/data channel if assigned modes are enabled by bits FMR5.EIBR and FMR0.XC1/0.

1 Clear channel mode. Contents of selected speech/data channel are not overwritten by internal or external bit robbing and ZCS information. Transmission of channel assigned signaling and control of pulse density is applied by the user.

Idle Channel Register (Read/Write)

Value after reset: 00_H, 00_H, 00_H, 00_H

	7							0	
ICB1	IC1	IC2	IC3	IC4	IC5	IC6	IC7	IC8	(x32)
ICB2	IC9	IC10	IC11	IC12	IC13	IC14	IC15	IC16	(x33)
ICB3	IC17	IC18	IC19	IC20	IC21	IC22	IC23	IC24	(x34)

IC(24:1) **Idle Channel Selection Bits**

These bits define the channels (time slots) of the outgoing PCM frame to be altered.

0 Normal operation.

1 Idle channel mode. The contents of the selected channel is overwritten by the idle channel code defined by register IDLE.

Line Interface Mode 0 (Read/Write)

Value after reset: 00_H

	7							0	
LIM0	XFB	XDOS			EQON	RLM	LL	MAS	(x36)

XFB **Transmit Full Bauded Mode**

Only applicable for dual rail mode (bit LIM1.DRS = 1).

0 Output signals XDOP/XDON are half bauded (normal operation).

1 Output signals XDOP/XDON are full bauded.

Note: If CMI coding is selected (FMR0.XC1/0 = 01) this bit has to be cleared.

XDOS **Transmit Data Out Sense**

0 Output signals XDOP/XDON are active low. Output XOID is active high (normal operation).

1 Output signals XDOP/XDON are active high. Output XOID is active low.

Note: If CMI coding is selected (FMR0.XC1/0 = 01) this bit has to be cleared.
The transmit frame marker XFM is independent of this bit.

EQON **Receive Equalizer On**

0 -10 dB Receiver: short haul mode

1 -36 dB Receiver: long haul mode

Note: By setting EQON = 1 the QuadFALC is able to adjust short haul or long haul mode automatically. After changing the EQON value a receiver reset is required (CMDR.RRES).

Note: When using EQON = 1 together with RLM = 1, LIM1.RIL(2:0) has to be set to 001_B.

RLM **Receive Line Monitoring**

0 normal receiver mode

1 receiver mode for receive line monitoring;
the receiver sensitivity is increased to detect resistively attenuated signals of -20 dB (short haul mode only)

Note: When using EQON = 1 together with RLM = 1, LIM1.RIL(2:0) has to be set to 001_B.

LL **Local Loop**

0 Normal operation

1 Local loop active. The local loopback mode disconnects the receive lines RL1/RL2 or RDIP/RDIN from the receiver. Instead of the signals coming from the line the data provided by system interface is routed through the analog receiver back to the system interface. The unipolar bit stream is transmitted undisturbedly on the line. Receiver and transmitter coding must be identical. Operates in analog and digital line interface mode. In analog line interface mode data is transferred through the complete analog receiver.

MAS **Master Mode**

0 Slave mode

1 Master mode on. Setting this bit the DCO-R circuitry is frequency synchronized to the clock (1.544, 2.048 MHz or 8 kHz, see IPC.SSYF, LIM1.DCOC) supplied by SYNC. If this pin is connected to V_{SS} or V_{DD} (or left open and pulled up to V_{DD} internally) the DCO-R circuitry is centered and no receive jitter attenuation is performed (only if 1.544 or 2.048 MHz clock is selected). The generated clocks are stable.

Line Interface Mode 1 (Read/Write)

Value after reset: 00_H

	7							0	
LIM1	CLOS	RIL2	RIL1	RIL0	DCOC	JATT	RL	DRS	(x37)

CLOS **Clear data in case of LOS**

0 normal receiver mode, receive data stream is transferred normally

1 received data is cleared as soon as LOS is detected

RIL(2:0) **Receive Input Threshold**

Only valid if analog line interface is selected (LIM1.DRS = 0).

“No signal” is declared if the voltage between pins RL1 and RL2 drops below the limits programmed by bits RIL(2:0) and the received data stream has no transition for a period defined in the PCD register. The threshold where “no signal” is declared is programmable by the RIL(2:0) bits depending on bit LIM0.EQON.

Note: LIM1.RIL(2:0) must be programmed before LIM0.EQON = 1 is set.

See the DC characteristics for detail.

DCOC **DCO-R Control**

0 1.544 MHz reference clock for the DCO-R circuitry provided on pin SYNC.

1 2.048 MHz reference clock for the DCO-R circuitry provided on pin SYNC.

Note: If IPC.SSYF = 1, external reference clock frequency is 8.0 kHz independent of DCOC.

JATT, RL **Remote Loop Transmit Jitter Attenuator**

00 = Normal operation. The remote loop transmit jitter attenuator is disabled. Transmit data bypasses the remote loop jitter attenuator buffer.

01 = Remote Loop active without transmit jitter attenuator enabled. Transmit data bypasses the remote loop jitter attenuator buffer.

10 = not assigned

11 = Remote Loop and remote loop jitter attenuator active. Received data from pins RL1/2 or RDIP/N or ROID is sent “jitter-free” on ports XL1/2 or XDOP/N or XOID. The de-jittered clock is generated by the DCO-X circuitry.

Note: JATT is only used to define the jitter attenuation during remote loop operation. Jitter attenuation during normal operation is not affected.

DRS **Dual Rail Select**

0 = The ternary interface is selected. Multifunction ports RL1/2 and XL1/2 become analog in/outputs.

1 = The digital dual rail interface is selected. Received data is latched on multifunction ports RDIP/RDIN while transmit data is output on pins XDOP/XDON.

Note: LIM0.EQON must be set to 0 when DRS = 1

Pulse Count Detection Register (Read/Write)

Value after reset: 00_H

	7						0	
PCD	PCD7						PCD0	(x38)

PCD(7:0) **Pulse Count Detection**

A LOS alarm (red alarm) is detected if the incoming data stream has no transitions for a programmable number T consecutive pulse positions. The number T is programmable by the PCD register and can be calculated as follows:
$T = 16 \times (N+1)$; with $0 \leq N \leq 255$.

The maximum time is: $256 \times 16 \times 648$ ns = 2.65 ms. Every detected pulse resets the internal pulse counter. The counter is clocked with the receive clock RCLK.

Pulse Count Recovery (Read/Write)

Value after reset: 00_H

	7						0	
PCR	PCR7						PCR0	(x39)

PCR(7:0) **Pulse Count Recovery**

A LOS alarm (red alarm) is cleared if a pulse density is detected in the received bit stream. The number of pulses M which must occur in the predefined PCD time interval is programmable by the PCR register and can be calculated as follows:

$M = N+1$; with $0 \leq N \leq 255$.

The time interval starts with the first detected pulse transition. With every received pulse a counter is incremented and the actual counter is compared to the contents of PCR register. If the pulse number reaches or exceeds the PCR value the LOS alarm is reset otherwise the alarm stays active. In this case the next detected pulse transition starts a new time interval.

An additional loss of signal recovery condition is selected by register LIM2.LOS1.

Line Interface Mode 2 (Read/Write)

Value after reset: 20_H

	7							0	
LIM2	LBO2	LBO1	SLT1	SLT0	SCF	ELT		LOS1	(x3A)

LBO(2:0) **Line Build-Out**

In long haul applications LIM0.EQON = 1 a transmit filter can be optionally placed on the transmit path to attenuate the data on pins XL1/2. Selecting the transmitter attenuation is possible in steps of 7.5 dB at 772kHz which is according to FCC68 and ANSI T1.403.

To meet the line build-out defined by ANSI T1.403 registers XPM(2:0) should be programmed as follows:

00 0 dB

01 -7.5 dB → XPM(2:0) = 00_H, 01_H, $8C_H$

10 -15 dB → XPM(2:0) = 01_H, 11_H, $8C_H$

11 -22.5 dB → XPM(2:0) = 00_H, 01_H, 07_H

SLT(1:0) **Receive Slicer Threshold**

00 The receive slicer generates a mark (digital one) if the voltage at RL1/2 exceeds 55% of the peak amplitude.

01 The receive slicer generates a mark (digital one) if the voltage at RL1/2 exceeds 67% of the peak amplitude (may be used in some T1/J1 applications).

10 The receive slicer generates a mark (digital one) if the voltage at RL1/2 exceeds 50% of the peak amplitude (default, recommended in T1/J1 mode).

11 The receive slicer generates a mark (digital one) if the voltage at RL1/2 exceeds 45% of the peak amplitude.

SCF **Select Corner Frequency of DCO-R**

Setting this bit reduces the corner frequency of the DCO-R circuit by the factor of ten to 0.6 Hz.

Note: Reducing the corner frequency of the DCO-R circuitry increases the synchronization time before the frequencies are synchronized.

ELT **Enable Loop-Timed**

0 normal operation

1 Transmit clock is generated from the clock supplied by MCLK which is synchronized to the extracted receive route clock. In this configuration the transmit elastic buffer has to be enabled. Refer to register FMR5.XTM. For correct operation of loop timed the remote loop (bit LIM1.RL = 0) must be inactive and bit CMR1.DXSS must be cleared.

LOS1 **Loss of Signal Recovery condition**

0 The LOS alarm is cleared if the predefined pulse density (register PCR) is detected during the time interval which is defined by register PCD.

1 Additionally to the recovery condition described above a LOS alarm is only cleared if the pulse density is fulfilled and no more than 15 contiguous zeros are detected during the recovery interval (according to GR-499-CORE).

Loop Code Register 1 (Read/Write)

Value after reset: 00_H

	7							0	
LCR1	EPRM	XPRBS	LDC1	LDC0	LAC1	LAC0	FLLB	LLBP	(x3B)

EPRM **Enable Pseudo Random Bit Sequence Monitor**

0 Pseudo random bit sequence (PRBS) monitor is disabled.

1 PRBS is enabled. Setting this bit enables incrementing the bit error counter BEC with each detected PRBS bit error. With any change of state of the PRBS internal synchronization status an interrupt ISR3.LLBSC is generated. The current status of the PRBS synchronizer is indicated by bit FRS1.LLBAD.

XPRBS **Transmit Pseudo Random Bit Sequence**

A one in this bit position enables transmission of a pseudo random bit sequence to the remote end. Depending on bit LLBP the PRBS is generated according to 2^{15} -1 or 2^{20}-1 (ITU-T O. 151).

LDC(1:0) **Length Deactivate (Down) Code**

These bits defines the length of the LLB deactivate code which is programmable in register LCR2.

00 length: 5 bit

01 length: 6 bit, 2 bit, 3 bit

10 length: 7 bit

11 length: 8 bit, 2 bit, 4bit

LAC(1:0) **Length Activate (Up) Code**

These bits defines the length of the LLB activate code which is programmable in register LCR3.

00 length: 5 bit

01 length: 6 bit, 2 bit, 3 bit

10 length: 7 bit

11 length: 8 bit, 2 bit, 4bit

FLLB **Framed Line Loopback/Invert PRBS**

Depending on bit LCR1.XPRBS this bit enables different functions:

LCR1.XPRBS = 0:

0 The line loopback code is transmitted including framing bits. LLB code overwrites the FS/DL-bits.

1 The line loopback code is transmitted unframed. LLB code does not overwrite the FS/DL-bits.

Invert PRBS

LCR1.XPRBS = 1:

0 The generated PRBS is transmitted not inverted.

1 The PRBS is transmitted inverted.

LLBP **Line Loopback Pattern**

LCR1.XPRBS = 0

0 Fixed line loopback code according to ANSI T1. 403.

1 Enable user programmable line loopback code by register LCR2/3.

LCR1.XPRBS = 1 or LCR1.EPRM = 1

0 2^{15} -1

1 2^{20} -1

Loop Code Register 2 (Read/Write)

Value after reset: 00_H

	7		0	
LCR2	LDC7		LDC0	(x3C)

LDC(7:0) **Line Loopback Deactivate Code**

If enabled by bit FMR5.XLD = 1 the LLB deactivate code automatically repeats until the LLB generator is stopped. Transmit data is overwritten by the LLB code. LDC0 is transmitted last. For correct operations bit LCR1.XPRBS has to cleared.

If LCR2 is changed while the previous deactivate code has been detected and is still received, bit FRS1.LLBDD will stay active until the incoming signal changes or a receiver reset is initiated (CMDR.RRES = 1).

Loop Code Register 3 (Read/Write)

Value after reset: 00_H

	7						0	
LCR3	LAC7						LAC0	(x3D)

LAC(7:0) **Line Loopback Activate Code**

If enabled by bit FMR5.XLU = 1 the LLB activate code automatically repeats until the LLB generator is stopped. Transmit data is overwritten by the LLB code. LAC0 is transmitted last. For correct operations bit LCR1.XPRBS has to cleared.

If LCR3 is changed while the previous activate code has been detected and is still received, bit FRS1.LLBAD will stay active until the incoming signal changes or a receiver reset is initiated (CMDR.RRES = 1).

System Interface Control 1 (Read/Write)

Value after reset: 00_H

	7							0	
SIC1	SSC1	SSD1	RBS1	RBS0	SSC0	BIM	XBS1	XBS0	(x3E)

SSC(1:0) **Select System Clock**

SIC1.SSC1/0 and SIC2.SSC2 define the clocking rate on the system highway.

SIC2.SSC2 = 0:

00 2.048 MHz

01 4.096 MHz

10 8.192 MHz

11 16.384 MHz

SIC2.SSC2 = 1:

00 1.544 MHz

01 3.088 MHz

10 6.176 MHz

11 12.352 MHz

SSD1 **Select System Data Rate 1**

SIC1.SSD1, FMR1.SSD0 and SIC2.SSC2 define the data rate on the system highway. Programming SSD1/SSD0 and corresponding data rate is shown below.

SIC2.SSC2 = 0:

00 2.048 Mbit/s

01 4.096 Mbit/s

10 8.192 Mbit/s

11 16.384 Mbit/s

SIC2.SSC2 = 1:

00 1.544 Mbit/s

01 3.088 Mbit/s

10 6.176 Mbit/s

11 12.352 Mbit/s

RBS(1:0) **Receive Buffer Size**

00 buffer size: 2 frames

01 buffer size: 1 frame

10 buffer size: 96 bits

11 bypass of receive elastic store

BIM **Bit Interleaved Mode**

Only applicable if bit SIC2.SSC2 is cleared. If SIC2.SSC2 is set high, the bit interleaved mode is automatically performed.

0 byte interleaved mode

1 bit interleaved mode

XBS(1:0) **Transmit Buffer Size**

00 bypass of transmit elastic store

01 buffer size: 1 frame

10 buffer size: 2 frames

11 buffer size: 96 bits

System Interface Control 2 (Read/Write)

Value after reset: 00_H

	7							0	
SIC2	FFS	SSF	CRB	SSC2	SICS2	SICS1	SICS0		(x3F)

FFS **Force Freeze Signaling**

Setting this bit disables updating of the receive signaling buffer and current signaling information is frozen. After resetting this bit and receiving a complete superframe updating of the signaling buffer is started again. The freeze signaling status can also be generated automatically by detection of a loss of signal alarm or a loss of frame alignment or a receive slip (only if external register access through RSIG is enabled). This automatic freeze signaling function is logically ored with this bit.
The current internal freeze signaling status is output on pin RP(A to D) with selected pin function FREEZE (PC(4:1).RPC(2:0) = 110). Additionally this status is also available in register SIS.SFS.

SSF **Serial Signaling Format**

Only applicable if pin function RSIG/XSIG and SIC3.TTRF = 0 is selected.

0 Bits (4:1) in all time slots except time slot 0 are cleared.

1 Bits (4:1) in all time slots except time slot 0 are set high.

CRB **Center Receive Elastic Buffer**

Only applicable if the time slot assigner is disabled (PC(4:1).RPC(2:0) = 001), no external or internal synchronous pulse receive is generated.
A transition from low to high forces a receive slip and the read pointer of the receive elastic buffer is centered. The delay through the buffer is set to one half of the current buffer size. It should be hold high for at least two 1.544 MHz periods before it is cleared.

SSC2 **Select System Clock**

This bit together with SIC1.SSC1/0 enables the system interface to run with a clock of 1.544, 3.088, 6.176 or 12.352 MHz (SSC2 = 1) or 2.048, 4.096, 8.192 or 16.384 MHz (SSC2 = 0).

See also register SIC1.SSC1/0 on **Page 362**.

SICS(2:0) **System Interface Channel Select**

Only applicable if the system clock rate is greater than 1.544/2.048MHz.

Received data is transmitted on pin RDO/RSIG or received on XDI/XSIG with the selected system data rate. If the data rate is greater than 1.544/2.048 Mbit/s the data is output or sampled in half, a quarter or one eighth of the time slot. Data is not repeated. The time while data is active during a $8 \times 488/648$ ns time slot is called a channel phase. RDO/RSIG are cleared (driven to low level) while XDI/XSIG are ignored for the remaining time of the $8 \times 488/648$ ns or for the remaining channel phases. The channel phases are selectable with these bits.

000 data active in channel phase 1, valid if system data rate is 16/8/4 or 12/6/3 Mbit/s

001 data active in channel phase 2, valid if data rate is 16/8/4 or 12/6/3 Mbit/s

010 data active in channel phase 3, valid if data rate is 16/8 or 12/6 Mbit/s

011 data active in channel phase 4, valid if data rate is 16/8 or 12/6 Mbit/s

100 data active in channel phase 5, valid if data rate is 16 or 12 Mbit/s

101 data active in channel phase 6, valid if data rate is 16 or 12 Mbit/s

110 data active in channel phase 7, valid if data rate is 16 or 12 Mbit/s

111 data active in channel phase 8, valid if data rate is 16 or 12 Mbit/s

System Interface Control 3(Read/Write)

Value after reset: 00_H

	7							0	
SIC3	CMI				RESX	RESR	TTRF	DAF	(x40)

CMI **Select CMI Precoding**

Only valid if CMI code (FMR0.XC1/0 = 01) is selected. This bit defines
the CMI precoding and influences transmit and receive data.

0 CMI with B8ZS precoding

1 CMI without B8ZS precoding

Note: Before local loop is closed, B8ZS precoding has to be switched off.

RESX **Rising Edge Synchronous Pulse Transmit**

Depending on this bit all transmit system interface data and marker are clocked or sampled with the selected active edge.

CMR2.IRSC = 0 or CMR2.IRSP = 0:

0 latched with the first falling edge of the selected PCM highway clock.

1 latched with the first rising edge of the selected PCM highway clock.

CMR2.IRSC = 1 or CMR2.IRSP = 1:

0 latched with the first rising edge of the selected PCM highway clock.

1 latched with the first falling edge of the selected PCM highway clock.

RESR **Rising Edge Synchronous Pulse Receive**

Depending on this bit all receive system interface data and marker are clocked with the selected active edge.

0 latched with the first falling edge of the selected PCM highway clock.

1 latched with the first rising edge of the selected PCM highway clock.

If bit CMR2.IRSP is set, the behavior of signal RFM (if used) is inverse:

0 latched with the first rising edge of the selected PCM highway clock.

1 latched with the first falling edge of the selected PCM highway clock.

TTRF **TTR Register Function (Fractional T1/J1 Access)**

Setting this bit the function of the TTR(4:1) registers are changed. A one in each TTR register forces the XSIGM marker high for the corresponding time slot and controls sampling of the time slots provided by pin XSIG. XSIG is selected by PC(4:1).XPC(3:0).

DAF **Disable Automatic Freeze**

0 Signaling is automatically frozen if one of the following alarms occurred: Loss of Signal (FRS0.LOS), Loss of Frame Alignment (FRS0.LFA), or receive slips (ISR3.RSP/N).

1 Automatic freezing of signaling data is disabled. Updating of the signaling buffer is also done if one of the above described alarm conditions is active. However, updating of the signaling buffer is stopped if SIC2.FFS is set. Significant only if the serial signaling access is enabled.

Clock Mode Register 1 (Read/Write)

Value after reset: 00_H

	7							0	
CMR1	DRSS1	DRSS0	RS1	RS0	DCS	STF	DXJA	DXSS	(x44)

DRSS(1:0) **Select RCLK Source**

These bits select the reference clock source for the DCO-R circuit.

00 receive reference clock generated by the DPLL of channel 1

01 receive reference clock generated by the DPLL of channel 2

10 receive reference clock generated by the DPLL of channel 3

11 receive reference clock generated by the DPLL of channel 4

RS(1:0) **Select RCLK Source**

These bits select the source of RCLK.

00 clock recovered from the line through the DPLL drives RCLK

01 clock recovered from the line through the DPLL drives RCLK and in case of an active LOS alarm RCLK pin is set high.

10 clock recovered from the line is dejittered by DCO-R to drive a 2.048-MHz (SIC2.SSC2 = 0) or 1.544-MHz (SIC2.SSC2 = 1) clock on RCLK.

11 clock recovered from the line is dejittered by DCO-R to drive a 8.192-MHz (SIC2.SSC2 = 0) or 6.176-MHz (SIC2.SSC2 = 1) clock on RCLK.

DCS **Disable Clock Switching**

In Slave mode (LIM0.MAS = 0) the DCO-R is synchronized on the recovered route clock. In case of loss of signal LOS the DCO-R switches automatically to the clock sourced by port SYNC. Setting this bit automatic switching from RCLK to SYNC is disabled.

STF **Select TCLK Frequency**

Only applicable if the pin function TCLK port XP(A to D) is selected by PC(4:1).XPC(3:0) = 0011. Data on XL1/2, XDOP/N, XOID are clocked with TCLK.

0 1.544 MHz

1 6.176 MHz

DXJA **Disable Internal Transmit Jitter Attenuation**

Setting this bit disables the transmit jitter attenuation. Reading the data out of the transmit elastic buffer and transmitting on XL1/2 (XDOP/N/XOID) is done with the clock provided on pin TCLK. In transmit elastic buffer bypass mode the transmit clock is taken from SCLKX, independent of this bit.

DXSS **DCO-X Synchronization Clock Source**

0 The DCO-X circuitry synchronizes to the internal reference clock which is sourced by SCLKX/R or RCLK. Since there are many reference clock opportunities the following internal prioritizing in descending order from left to right is realized: LIM1.RL > CMR1.DXSS > LIM2.ELT > current working clock of transmit system interface.
If one of these bits is set the corresponding reference clock is taken.

1 DCO-X synchronizes to an external reference clock provided by pin XP(A to D) pin function TCLK, if no remote loop is active. TCLK is selected by PC(4:1).XPC(3:0) = 0011.

Clock Mode Register 2 (Read/Write)

Value after reset: 00_H

	7							0	
CMR2			DCOXC	DCF	IRSP	IRSC	IXSP	IXSC	(x45)

DCOXC **DCO-X Center-Frequency Enable**

0 The center function of the DCO-X circuitry is disabled.

1 The center function of the DCO-X circuitry is enabled.
DCO-X centers to 1.544 MHz related to the master clock reference (MCLK), if reference clock (e.g. SCLKX) is missing.

DCF **DCO-R Center- Frequency Disabled**

0 The DCO-R circuitry is frequency centered
- in master mode if no 1.544 or 2.048 MHz reference clock on pin SYNC is provided or
- in slave mode if a loss of signal occurs in combination with no 1.544 or 2.048 MHz clock on pin SYNC or
- a gapped clock is provided at pin RCLKI and this clock is inactive or stopped.

1 The center function of the DCO-R circuitry is disabled. The generated clock (DCO-R) is frequency frozen in that moment when no clock is available at pin SYNC or pin RCLKI. The DCO-R circuitry starts synchronization as soon as a clock at pins SYNC or RCLKI appears.

IRSP **Internal Receive System Frame Sync Pulse**

0 The frame sync pulse for the receive system interface is sourced by $\overline{\text{SYPR}}$ (if $\overline{\text{SYPR}}$ is applied). If $\overline{\text{SYPR}}$ is not applied, the frame sync pulse is derived from the RDO output signal internally (free running). The use of IRSP = 0 is recommended.

1 The frame sync pulse for the receive system interface is internally sourced by the DCO-R circuitry. This internally generated frame sync signal can be output (active low) on multi function ports RP(A to D) (RPC(2:0) = 001).

Note: This is the only exception where the use of RFM and $\overline{\text{SYPR}}$ is allowed at the same time. Because only one set of offset registers (RC1/0) is available, programming is done by using the $\overline{\text{SYPR}}$ calculation formula in the same way as for the external $\overline{\text{SYPR}}$ pulse. Bit IRSC must be set for correct operation.

IRSC **Internal Receive System Clock**

0 The working clock for the receive system interface is sourced by SCLKR of or in receive elastic buffer bypass mode from the corresponding extracted receive clock RCLK.

1 The working clock for the receive system interface is sourced internally by DCO-R or in bypass mode by the extracted receive clock. SCLKR is ignored.

IXSP **Internal Transmit System Frame Sync Pulse**

0 The frame sync pulse for the transmit system interface is sourced by $\overline{\text{SYPX}}$.

1 The frame sync pulse for the transmit system interface is internally sourced by the DCO-R circuitry. Additionally, the external XMFS signal defines the transmit multiframe begin. XMFS is enabled or disabled by the multifunction port configuration. For correct operation bits CMR2.IXSC/IRSC must be set. $\overline{\text{SYPX}}$ is ignored.

IXSC **Internal Transmit System Clock**

0 The working clock for the transmit system interface is sourced by SCLKX.

1 The working clock for the transmit system interface is sourced internally by the working clock of the receive system interface. SCLKX is ignored.

Global Configuration Register (Read/Write)

Value after reset: 00_H

	7							0	
GCR	VIS	SCI	SES	ECMC				PD	(x46)

VIS **Masked Interrupts Visible**

0 Masked interrupt status bits are not visible in registers ISR(4:0).

1 Masked interrupt status bits are visible in ISR(4:0), but they are not visible in registers GIS.

SCI **Status Change Interrupt**

0 Interrupts are generated either on activation or deactivation of the internal interrupt source.

1 The following interrupts are activated both on activation and deactivation of the internal interrupt source:
ISR2.LOS, ISR2.AIS and ISR0.PDEN

SES **Select External Second Timer**

0 internal second timer selected

1 external second timer selected

ECMC **Error Counter Mode COFA**

0 not defined; reserved for future applications.

1 A Change of Frame or Multiframe Alignment COFA is detected since the last resynchronization. The events are accumulated in the COFA event counter COEC.(1:0).
Multiframe periods received in the asynchronous state are accumulated in the COFA event counter COEC.(7:2).
An overflow of each counter is disabled.

PD **Power Down**

Switches between power up and power down mode.

0 Power Up

1 Power Down
All outputs are driven inactive, except the multifunction ports, which are weakly driven high by the internal pullup devices.

Errored Second Mask (Read/Write)

Value after reset: FF_H

	7						0	
ESM	LFA	FER	CER	AIS	LOS	CVE	SLIP	(x47)

ESM **Errored Second Mask**

This register functions as an additional mask register for the interrupt status bit Errored Second (ISR3.ES). A ’1’ in a bit position of ESM deactivates the related second interrupt.

Disable Error Counter (Write)

Value after reset: 00_H

	7						0	
DEC	DRBD		DCOEC	DBEC	DCEC	DEBC	DCVC	DFEC	(x60)

DRBD **Disable Receive Buffer Delay**

This bit has to be set before reading the register RBD. It is automatically reset if RBD has been read.

DCOEC **Disable COFA Event Counter**

DBEC **Disable PRBS Bit Error Counter**

Only valid if LCR1.EPRM = 1 and FMR1.ECM are reset.

DCEC **Disable CRC Error Counter**

DEBC **Disable Errored Block Counter**

DCVC **Disable Code Violation Counter**

DFEC **Disable Framing Error Counter**

These bits are only valid if FMR1.ECM is cleared. They have to be set before reading the error counters. They are reset automatically if the corresponding error counter high byte has been read. With the rising edge of these bits the error counters are latched and then cleared.

Note: Error counters and receive buffer delay can be read 1 µs after setting the according bit in bit DEC.

Transmit Signaling Register (Write)

Value after reset: not defined

Table 66 Transmit Signaling Registers (T1/J1)

	7							0	
XS1	A1	B1	C1/A2	D1/B2	A2/A3	B2/B3	C2/A4	D2/B4	(x70)
XS2	A3/A5	B3/B5	C3/A6	D3/B6	A4/A7	B4/B7	C4/A8	D4/B8	(x71)
XS3	A5/A9	B5/B9	C5/A10	D5/B10	A6/A11	B6/B11	C6/A12	D6/B12	(x72)
XS4	A7/A13	B7/B13	C7/A14	D7/B14	A8/A15	B8/B15	C8/A16	D8/B16	(x73)
XS5	A9/A17	B9/B17	C9/A18	D9/B18	A10/A19	B10/B19	C10/A20	D10/B20	(x74)
XS6	A11/A21	B11/B21	C11/A22	D11/B22	A12/A23	B12/B23	C12/A24	D12/B24	(x75)
XS7	A13/A1	B13/B1	C13/A2	D13/B2	A14/A3	B14/B3	C14/A4	D14/B4	(x76)
XS8	A15/A5	B15/B5	C15/A6	D15/B6	A16/A7	B16/B7	C16/A8	D16/B8	(x77)
XS9	A17/A9	B17/B9	C17/A10	D17/B10	A18/A11	B18/B11	C18/A12	D18/B12	(x78)
XS10	A19/A13	B19/B13	C19/A14	D19/B14	A20/A15	B20/B15	C20/A16	D20/B16	(x79)
XS11	A21/A17	B21/B17	C21/A18	D21/B18	A22/A19	B22/B19	C22/A20	D22/B20	(x7A)
XS12	A23/A21	B23/B21	C23/A22	D23/B22	A24/A23	B24/B23	C24/A24	D24/B24	(x7B)

Transmit Signaling Register (12:1)

The transmit signaling register access is enabled by setting bit FMR5.EIBR = 1. Each register contains the bit robbing information for 8 DS0 channels. With the transmit CAS empty interrupt ISR1.CASE the contents of these registers is copied into a shadow register. The contents is subsequently sent out in the corresponding bit positions of the next outgoing multiframe. XS1.7 is sent out first in channel 1 frame 1 and XS12.0 is sent out last. The transmit CAS empty interrupt ISR1.CASE requests that these registers should be serviced within the next 3 ms. If requests for new information are ignored, current contents is repeated.

Note: If access to XS(12:1) registers is done without control of the interrupt ISR1.CASE and the write access to these registers is done exact in that moment when this interrupt is generated, data is lost.

A software reset (CMDR.XRES) resets these registers.

Port Configuration (4:1) (Read/Write)

Value after reset: 00_H

	7							0	
PC1		RPC12	RPC11	RPC10	XPC13	XPC12	XPC11	XPC10	(x80)
PC2		RPC22	RPC21	RPC20	XPC23	XPC22	XPC21	XPC20	(x81)
PC3		RPC32	RPC31	RPC30	XPC33	XPC32	XPC31	XPC30	(x82)
PC4		RPC42	RPC41	RPC40	XPC43	XPC42	XPC41	XPC40	(x83)

RPC(2:0) **Receive multifunction port configuration**

The multifunction ports RP(A to D) are bidirectional. After Reset these ports are configured as inputs. With the selection of the pin function the In/Output configuration is also achieved. The input function $\overline{\text{SYPR}}$ may only be selected once, it must not be selected twice or more. Register PC1 configures port RPA, while PC2 → port RPB, PC3 → port RPC and PC4 → port RPD.

000 $\overline{\text{SYPR}}$: Synchronous Pulse Receive (Input)
Together with register RC1/0 $\overline{\text{SYPR}}$ defines the frame begin on the receive system interface. Because of the offset programming the $\overline{\text{SYPR}}$ and the RFM pin function can not be selected in parallel.

001 RFM: Receive Frame Sync (Output)
CMR2.IRSP = 0: The Receive Frame Marker is active high for one 1.544-MHz period during any bit position of the current frame. Programming of the bit position is done by using registers RC1/0. The internal time slot assigner is disabled. The RFM offset calculation formula has to be used.

CMR2.IRSP = 1: Internally generated frame synchronization pulse sourced by the DCO-R circuitry. The pulse is active low for one 1.544-MHz period.

010 RMFB: Receive Multiframe Begin (Output)
Marks the beginning of every received multiframe or optionally the begin of every CAS multiframe begin (active high).

011 RSIGM: Receive Signaling Marker (Output)
Marks the time slots which are defined by register RTR(4:1) of every frame at port RDO.

100 RSIG: Receive Signaling Data (Output)
The received CAS multiframe is transmitted on this pin. Time Slots on RSIG correlates directly to the time slot assignment on RDO. In system interface multiplex mode all four received signaling data streams are merged into a single rail data stream byte or bit interleaved on RSIG1.

101 DLR: Data Link Bit Receive (Output)
Marks the S_a8...4-bits within the data stream on RDO.

110 FREEZE: Freeze Signaling (Output)
The freeze signaling status is active high by detecting a Loss of Signal alarm, or a Loss of CAS Frame Alignment or a receive slip (positive or negative). It stays high for at least one complete multiframe after the alarm disappears. Setting SIC2.FFS enforces a high on pin FREEZE.

111 $\overline{\text{RFSP}}$: Receive Frame Synchronous Pulse (Output)
Marks the frame begin in the receivers synchronous state. This marker is active low for 488 ns with a frequency of 8 kHz.

XPC(3:0) Transmit multifunction Port Configuration

The multifunction ports XP(A to D) are bidirectional. After Reset these ports are configured as inputs. With the selection of the pin function the In/Output configuration is also achieved. Each of the four different input functions ($\overline{\text{SYPX}}$, XMFS, XSIG, TCLK) may only be selected once. No input function must be selected twice or more. $\overline{\text{SYPX}}$ and XMFS should not be selected in parallel. Register PC1 configures port XPA, while PC2 → port XPB, PC3 → port XPC and PC4 → port XPD.

0000 $\overline{\text{SYPX}}$: Synchronous Pulse Transmit (Input)
Together with register XC1/0 $\overline{\text{SYPX}}$ defines the frame begin on the transmit system interface ports XDI and XSIG.

0001 XMFS: Transmit Multiframe Synchronization (Input)
Together with register XC1/0 XMFS defines the frame and multiframe begin on the transmit system interface ports XDI and XSIG. Depending on PC5.CXMFS the signal on XMFS is active high or low.

0010 XSIG: Transmit Signaling Data (Input)
Input for transmit signaling data received from the signaling highway. In system interface multiplex mode latching of the data stream containing the 4 signaling multiframes is done byte or bit interleaved on port XDI1. Optionally sampling of XSIG data is controlled by the active high XSIGM marker.

0011 TCLK: Transmit Clock (Input)
A 1.544/6.176MHz clock has to be sourced by the system if the internal generated transmit clock (DCO-X) is not used. Optionally this input is used as a synchronization clock for the DCO-X circuitry with a frequency of 1.544 or 6.176 MHz.

0100 XMFB: Transmit Multiframe Begin (Output)
Marks the beginning of every transmit multiframe.

0101 XSIGM: Transmit Signaling Marker (Output)
Marks the time slots which are defined by register TTR(4:1) of every frame at port XDI.

0110 DLX: Data Link Bit Transmit (Output)
Marks the S_a8...4-bits within the data stream on XDI.

0111 XCLK: Transmit Line Clock (Output)
Frequency: 1.544MHz

1000 XLT: Transmit Line Tristate (Input)
With a high level on this port the transmit lines XL1/2 or XDOP/N are set directly into tristate. This pin function is logically ored with register XPM2.XLT.

Port Configuration 5 (Read/Write)

Value after reset: 00_H

	7							0	
PC5					CXMFS	CSXP	CSRP	CRP	(x84)

CXMFS **Configure XMFS Port**

0 Port XMFS is active low.

1 Port XMFS is active high.

CSXP **Configure SCLKX Port**

0 SCLKX: Input

1 SCLKX: Output

Note: Must be cleared because no output function is defined.

CSRP **Configure SCLKR Port**

0 SCLKR: Input

1 SCLKR: Output

CRP **Configure RCLK Port**

0 RCLK: Input

1 RCLK: Output

Global Port Configuration 1 (Read/Write)

Value after reset: 00_H

	7							0	
GPC1	SMM	CSFP1	CSFP0		FSS1	FSS0	R1S1	R1S0	(85)

SMM **System Interface Multiplex Mode**

Setting this bit enables a single data stream of 16.384, 8.192, 12.352 or 6.176 Mbit/s containing all the T1/J1 frames of all four channels.

0 System multiplex mode disabled

1 System multiplex mode enabled

The receive system interface for all four channels is running with the clock provided on SCLKR1 and the frame sync pulse provided on $\overline{\text{SYPR1}}$. The transmit system interface is running with SCLKX1 and $\overline{\text{SYPX1}}$. Data is transmitted/accepted in a byte- or bit-interleaved format. In the system interface multiplex mode the following pin configuration has to be fulfilled and **must be identical for all for 4 channels**:

- $\overline{\text{SYPR1}}$ has to be provided on pin RPA1
- $\overline{\text{SYPX1}}$ has to be provided on pin XPA1 or
- XMFS has to be provided on pin XPB1
- XSIG has to be provided on pin XPC1
- RSIG will be output on pin RPB1

Each of the four channels has to be configured equally:

- clocking rate :

16.384 or 8.192 MHz, SIC1.SSC1/0, SIC2.SSC2 = 0 or

12.352 or 6.176 MHz, SIC1.SSC1/0, SIC2.SSC2 = 1

- data rate :

16.384 or 8.192 Mbit/s, SIC1.SSD, FMR1.SSD0; SIC2.SSC2 = 0 or

12.352 or 6.176 Mbit/s, SIC1.SSD, FMR1.SSD0; SIC2.SSC2 = 1

- time-slot offset programming : RC1/0, XC1/0

- receive buffer size : SIC1.RBS1/0 = 00 (2 frames)

for example: system clock rate = 8.192 MHz;

SIC1.SSC1/0 = 10, SIC2.SSC2 = 0 and
system data rate = 8.192 Mbit/s :

SIC1.SSD1 = 1, FMR1.SSD0 = 0, SIC2.SSC2 = 0
The multiplexed data stream is logically ored internally. Therefore the selection of the active channel phase have to be configured different for each single channel (4:1). Programming is done with SIC2.SICS(2:0).
for channel 1: SIC2.SICS(2:0) = 000, selects the first channel phase
for channel 2: SIC2.SICS(2:0) = 001, selects the second channel phase
for channel 3: SIC2.SICS(2:0) = 010, selects the third channel phase
for channel 4: SIC2.SICS(2:0) = 011, selects the fourth channel phase

byte interleaved data format: SIC1.BIM = 0

XDI/RDO: F1-TS0, F2-TS0, F3-TS0, F4-TS0, F1-TS1,... F4-TS31

X/RSIG: F1-STS0, F2-STS0, F3-STS0, F4-STS0, F1-... F4-STS31

or : bit interleaved data format: SIC1.BIM = 1

XDI/RDO: F1-TS0-B1, F2-TS0-B1, F3-TS0-B1, F4-TS0-B1, F1-TS0-B2,... F4-TS31-B8

X/RSIG: F1-STS0-B1, F2-STS0-B1, F3-STS0-B1, F4-STS0-B1, F1-STS0-B2,... F4-STS31-B8

with : F = Framer, TS = Time-Slot, STS = Signaling Time-Slot, B = Bit

In system interface multiplex mode signals on RDO(2:4) and RSIG(2:4) are undefined, while signals on SCLKR(2:4), $\overline{\text{SYPR}}$(2:4), SCLKX(2:4), $\overline{\text{SYPX}}$(2:4)4, XDI(2:4) and XSIG(2:4) are ignored.

CSFP(1:0) **Configure SEC/FSC Port**

The FSC pulse is generated if the DCO-R circuitry of the selected channel is active (CMR2.IRSC = 1 or CMR1.RS1/0 = 10 or 11).

00 SEC: Input, active high

01 SEC: Output, active high

10 FSC: Output, active high

11 FSC: Output, active low

FSS(1:0) **SEC/FSC Source**

One of the four internally generated dejittered 8-kHz clocks or second timers are output on pin SEC/FSC.

GPC1.CSFP1 = 1:

00 FSC: 8 kHz sourced by channel 1

01 FSC: 8 kHz sourced by channel 2

10 FSC: 8 kHz sourced by channel 3

11 FSC: 8 kHz sourced by channel 4

GPC1.CSFP1 = 0:

00 SEC: second timer sourced by channel 1

01 SEC: second timer sourced by channel 2

10 SEC: second timer sourced by channel 3

11 SEC: second timer sourced by channel 4

R1S(1:0) **RCLK Source**

One of the four internally generated receive route clocks is output on pin RCLK1. Outputs RCLK(2:4) are valid independent of these bits. Refer also to CMR1.RS(1:0).

00 extracted receive clock of channel 1

01 extracted receive clock of channel 2

10 extracted receive clock of channel 3

11 extracted receive clock of channel 4

Command Register 2 (Write)

Value after reset: 00_H

CMDR2							RSUC	XPPR	(x87)

RSUC **Reset Signaling Unit Counter**

1 After setting this bit the SS7 signaling unit counter and error counter are reset.The bit is cleared automatically after execution.

Note: The maximum time between writing to the CMDR2 register and the execution of the command takes 2.5 periods of the current system data rate. Therefore, if the CPU operates with a very high clock rate in comparison with the QuadFALC's clock, it is recommended that bit SIS.CEC should be checked before writing to the CMDR register to avoid any loss of commands.

XPPR **Transmit Periodical Performance Report (PPR)**

After setting this bit the last PPR is sent once. The bit is cleared automatically after completion. Applies to HDLC channel 1 only.

Common Configuration Register 5 (Read/Write)

Value after reset: 00_H

	7							0	
CCR5		CSF2	SUET	CSF	AFX		CR	EPR	(x8D)

Note: SUET, CSF, CSF2 and AFX are only valid, if SS7 mode is selected.
CR and EPR are only valid, if PPR mode is selected.

CSF2 **Compare Status Field - Mode 2**

If the status fields of consecutive LSSUs are equal, only the first is stored and every following is ignored.
Exception: if identical FISUs are received, *two* of them are stored,

0 Compare disabled.

1 Compare enabled.

SUET **Signaling Unit Error Threshold**

Defines the number of signaling units received in error that will cause an error rate high indication (ISR1.SUEX).

0 threshold 64 errored signaling units

1 threshold 32 errored signaling units

CSF **Compare Status Field**

If the status fields of consecutive LSSUs are equal, only the first is stored and every following is ignored.

0 Compare disabled.

1 Compare enabled.

AFX **Automatic FISU Transmission**

After the contents of the transmit FIFO (XFIFO) has been transmitted completely, FISUs are transmitted automatically. These FISUs contain the FSN and BSO of the last transmitted signaling unit (provided in XFIFO).

0 Automatic FISU transmission disabled.

1 Automatic FISU transmission enabled.

CR **Command Response**

Reflects the status of the CR bit in the SAPI octet transmitted during Periodical Performance Report (PPR), if CCR5.EPR = 1.

0 CR bit = 0

1 CR bit = 1

EPR **Enable Periodical Performance Report (PPR)**

If the periodical performance report is to be used, an HDLC format must be selected by MODE.MDS(2:0).

0 PPR disabled.

1 PPR enabled.

Global Clock Mode Register 1 (Read/Write)

Value after reset: 00_H

	7							0	
GCM1	PHD_E17	PHD_E16	PHD_E15	PHD_E14	PHD_E13	PHD_E12	PHD_E11	PHD_E10	(92)

PHD_E1(7:0) **Frequency Adjust for E1**

For details see calculation formulas below.

Global Clock Mode Register 2 (Read/Write)

Value after reset: 00_H

	7							0	
GCM2	0	0	1	VFREQ_EN	PHD_E111	PHD_E110	PHD_E19	PHD_E18	(93)

PHD_E1(8:11) **Frequency Adjust for E1**

For details see calculation formulas below.

GCM2.(7:5) reserved

Must be cleared.

GCM2.(4) reserved

Must be set to 1.

Global Clock Mode Register 3 (Read/Write)

Value after reset: 00_H

	7							0	
GCM3	PHD_T17	PHD_T16	PHD_T15	PHD_T14	PHD_T13	PHD_T12	PHD_T11	PHD_T10	(94)

PHD_T1(7:0) **Frequency Adjust for T1**

For details see calculation formulas below.

Global Clock Mode Register 4 (Read/Write)

Value after reset: 00_H

	7							0	
GCM4	0	0	0	0	PHD_T1 11	PHD_T1 10	PHD_T1 9	PHD_T1 8	(95)

PHD_T1(8:11) **Frequency Adjust for T1**

For details see calculation formulas below.

GCM4.(7:4) reserved

Must be cleared.

Global Clock Mode Register 5 (Read/Write)

Value after reset: 00_H

	7							0	
GCM5	0	0	0	PLL_M 4	PLL_M 3	PLL_M 2	PLL_M 1	PLL_M 0	(96)

PLL_M(4:0) **PLL Dividing Factor M**

For details see calculation formulas below.

GCM5.(7:5) reserved

Must be cleared.

Note: Write operations to GCM5 initiate a PLL reset (see below).

Global Clock Mode Register 6 (Read/Write)

Value after reset: 00_H

	7							0	
GCM6	0	0	PLL_N 5	PLL_N 4	PLL_N 3	PLL_N 2	PLL_N 1	PLL_N 0	(97)

PLL_N(5:0) **PLL Dividing Factor N**

For details see calculation formulas below.

GCM6.(7:6) reserved
Must be cleared.

Note: Write operations to GCM6 initiate a PLL reset (see below).

Global Clock Mode Register 7 (Read/Write)

Value after reset: 00_H

	7							0	
GCM7	1	PHSX_ E12	PHSX_ E11	PHSX_ E10	PHSN_ E13	PHSN_ E12	PHSN_ E11	PHSN_ E10	(98)

GCM7.7 reserved
Must be set to 1.

PHSX_E1(2:0) Frequency adjustment value E1

PHSN_E1(3:0) Frequency adjustment value E1

Global Clock Mode Register 8 (Read/Write)

Value after reset: 00_H

	7							0	
GCM8	1	PHSX_ T12	PHSX_ T11	PHSX_ T10	PHSN_ T13	PHSN_ T12	PHSN_ T11	PHSN_ T10	(99)

GCM8.7 reserved
Must be set to 1.

PHSX_T1(2:0) Frequency adjustment value T1/J1

PHSN_T1(3:0) Frequency adjustment value T1/J1

Flexible Clock Mode Settings

The register settings for flexible master clock can be calculated as follows. For some standard frequencies see **Table 61** below. The variables used in these calculations are located in registers GCM1 to GCM8.

To support the necessary calculations, an easy-to-use PC tool is available for free (see **Chapter 13.3** on page **457** for details).

1. PLL_M and PLL_N must fulfill the equations:

a.

for PLL_M = 0 to 31:

$$f_{pdref} = \frac{f_{MCLK}}{PLL\_M + 1}$$

b.

for PLL_N = 25 to 63:

$$1.0\ MHz \leq f_{pdref} \leq 6.0\ MHz$$

for PLL_N = 0 to 24:

$$5.0\ MHz \leq f_{pdref} \leq 15.0\ MHz$$

Attention: To achieve optimum performance it is recommended to adjust f_{pdref} as high as possible.

c.

$$260\ MHz \leq f_{MCLK} \times \frac{4 \times (PLL\_N + 1)}{PLL\_M + 1} \leq 395.26\ MHz$$

(as high as possible within this range)

2. Selection of the dividing mode to best fulfill:

$$f_{outE1} = f_{MCLK} \times \frac{4 \times (PLL\_N + 1)}{\left(PHSN\_E1 + \frac{PHSX\_E1}{6}\right) \times (PLL\_M + 1)} \cong 2 \times 16.384\ MHz$$

$$f_{outT1} = f_{MCLK} \times \frac{4 \times (PLL\_N + 1)}{\left(PHSN\_T1 + \frac{PHSX\_T1}{6}\right) \times (PLL\_M + 1)} \cong 2 \times 12.352\ MHz$$

Though the target frequency might not be met directly, the dividing mode has to be selected to reach a frequency which is as near as possible to the target frequency.

PHSN_E1, PHSN_T1: 1 to 15; PHSX_E1, PHSX_T1: 0 to 5

3. Calculation of the correction value for frequency mismatch correction:

$$PHD\_E1 = 12288 \times \left[\left(PHSN\_E1 + \frac{PHSX\_E1}{6}\right) - \frac{4 \times (PLL\_N + 1)}{PLL\_M + 1} \times \frac{f_{MCLK}}{2 \times 16.384\ MHz}\right]$$

$$PHD\_T1 = 12288 \times \left[\left(PHSN\_T1 + \frac{PHSX\_T1}{6}\right) - \frac{4 \times (PLL\_N + 1)}{PLL\_M + 1} \times \frac{f_{MCLK}}{2 \times 12.352\ MHz}\right]$$

The result of these equations will be in the range of -2048 to +2047. Negative values are represented in 2s-complement format (e.g., $-2000_D = 830_H$; $+2000_D = 7D0_H$).

To achieve optimal QuadFALC performance values < -1023 and > +1023 has to be applied. Negative values are favored.

Table 67 Clock Mode Register Settings for E1 and T1/J1

f_{MCLK}[MHz]	GCM1	GCM2	GCM3	GCM4	GCM5	GCM6	GCM7	GCM8
1.544	F0	19	00	08	00	2B	98	DA
2.048	00	18	D2	0A	00	21	A8	9B
8.192	00	18	D2	0A	03	21	A8	9B
10.000	DD	1A	3B	09	08	3C	98	DA
12.352	11	18	E9	0A	0A	3D	A8	9B
16.384	00	18	D2	0A	07	21	A8	9B

Note: All values given in hexadecimal notation.

Time Slot Even/Odd Select (Read/Write)

Value after reset: 00_H

	7						0		
TSEO							EO11	EO10	(xA0)

HDLC protocol data can be sent in even, odd or both frames of a multiframe. Even frames are frame number 2, 4,..., odd frames are frame number 1, 3,... The selection refers to receive and transmit direction as well. Each multiframe starts with an odd frame and ends with an even frame. By default all frames are used for HDLC reception and transmission.

EO1(1:0) **Even/Odd frame selection - HDLC Channel 1**
Channel 1 HDLC protocol data can be sent in even, odd or both frames of a multiframe.

00 even and odd frames

01 odd frames only

10 even frames only

11 undefined

Time Slot Bit Select 1 (Read/Write)

Value after reset: FF_H

	7						0		
TSBS1	TSB17	TSB16	TSB15	TSB14	TSB13	TSB12	TSB11	TSB10	(xA1)

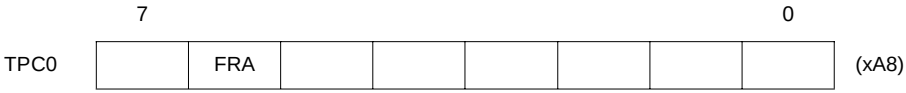
TSB1(7:0) **Time Slot Bit Selection**
Only bits selected by this register are used for HDLC in selected time slots. Time slot selection is done by setting the appropriate bits in registers TTR(4:1) and RTR(4:1) independently for receive and transmit direction. Bit selection is common to receive and transmit direction. By default all bit positions within the selected time slot(s) are enabled.

TSB1x = 0 bit position x in selected time slot(s) is not used for HDLC channel 1 reception and transmission.

TSB1x = 1 bit position x in selected time slot(s) is used for HDLC channel 1 reception and transmission.

Test Pattern Control Register 0 (Read/Write)

Value after reset: 00_H



FRA **Framed/Unframed Selection**

0 PRBS is generated/monitored unframed.

Framing information is overwritten by the generator.

1 PRBS is generated/monitored framed.

Time slot 0 is not overwritten by the generator and not observed by the monitor.

10.3 T1/J1 Status Register Addresses

Table 68 T1/J1 Status Register Address Arrangement

Address[1)]	Register	Type	Comment	Page
x00	RFIFO	R	Receive FIFO	392
x01	RFIFO	R	Receive FIFO	392
x49	RBD	R	Receive Buffer Delay	392
4A	VSTR	R	Version Status Register	393
x4B	RES	R	Receive Equalizer Status	393
x4C	FRS0	R	Framer Receive Status 0	394
x4D	FRS1	R	Framer Receive Status 1	396
x4E	FRS2	R	Framer Receive Status 2	398
x50	FECL	R	Framing Error Counter Low	399
x51	FECH	R	Framing Error Counter High	399
x52	CVCL	R	Code Violation Counter Low	400
x53	CVCH	R	Code Violation Counter High	400
x54	CECL	R	CRC Error Counter Low	401
x55	CECH	R	CRC Error Counter High	401
x56	EBCL	R	Errored Block Counter Low	402
x57	EBCH	R	Errored Block Counter High	402
x58	BECL	R	Bit Error Counter Low	403
x59	BECH	R	Bit Error Counter High	403
x5A	COEC	R	COFA Event Counter	404
x5C	RDL1	R	Receive DL-Bit Register 1	405
x5D	RDL2	R	Receive DL-Bit Register 2	405
x5E	RDL3	R	Receive DL-Bit Register 3	406
x62	RSP1	R	Receive Signaling Pointer 1	406
x63	RSP2	R	Receive Signaling Pointer 2	406
x64	SIS	R	Signaling Status Register	407
x65	RSIS	R	Receive Signaling Status Register	408
x66	RBCL	R	Receive Byte Control Low	410
x67	RBCH	R	Receive Byte Control High	410
x68	ISR0	R	Interrupt Status Register 0	411

Table 68 T1/J1 Status Register Address Arrangement (cont'd)

Address[1)]	Register	Type	Comment	Page
x69	ISR1	R	Interrupt Status Register 1	413
x6A	ISR2	R	Interrupt Status Register 2	414
x6B	ISR3	R	Interrupt Status Register 3	416
x6C	ISR4	R	Interrupt Status Register 4	417
x6E	GIS	R	Global Interrupt Status	417
6F	CIS	R	Channel Interrupt Status Register	418
x70	RS1	R	Receive Signaling Register 1	419
x71	RS2	R	Receive Signaling Register 2	419
x72	RS3	R	Receive Signaling Register 3	419
x73	RS4	R	Receive Signaling Register 4	419
x74	RS5	R	Receive Signaling Register 5	419
x75	RS6	R	Receive Signaling Register 6	419
x76	RS7	R	Receive Signaling Register 7	419
x77	RS8	R	Receive Signaling Register 8	419
x78	RS9	R	Receive Signaling Register 9	419
x79	RS10	R	Receive Signaling Register 10	419
x7A	RS11	R	Receive Signaling Register 11	419
x7B	RS12	R	Receive Signaling Register 12	419

1) x = 0: channel 1 register; x = 1: channel 2 register; x = 2: channel 3 register; x = 3: channel 4 register

10.4 Detailed Description of T1/J1 Status Registers

Receive FIFO (Read)

	7							0	
RFIFO	RF7							RF0	(x00)
RFIFO	RF15							RF8	(x01)

Reading data from RFIFO can be done in an 8-bit (byte) or 16-bit (word) access depending on the selected bus interface mode. The LSB is received first from the serial interface.

The size of the accessible part of RFIFO is determined by programming the bits CCR1.RFT(1:0) (RFIFO threshold level). It can be reduced from 32 bytes (reset value) down to 2 bytes (four values: 32, 16, 4, 2 bytes).

Data Transfer

Up to 32 bytes/16 words of received data can be read from the RFIFO following a RPF or a RME interrupt.

RPF Interrupt: A fixed number of bytes/words to be read (32, 16, 4, 2 bytes). The message is not yet complete.

RME Interrupt: The message is completely received. The number of valid bytes is determined by reading the RBCL, RBCH registers.

RFIFO is released by issuing the “Receive Message Complete” command (RMC).

Receive Buffer Delay (Read)

	7							0	
RBD			RBD5	RBD4	RBD3	RBD2	RBD1	RBD0	(x49)

RBD(5:0) **Receive Elastic Buffer Delay**

These bits informs the user about the current delay (in time slots) through the receive elastic buffer. The delay is updated every 386 or 193 bits (SIC1.RBS1/0). Before reading this register the user has to set bit DEC.DRBD in order to halt the current value of this register. After reading RBD updating of this register is enabled. Not valid if the receive buffer is bypassed.
000000 = delay < 1 time slot
...
111111 = delay >63 time slots

Version Status Register (Read)

	7						0	
VSTR	VN7						VN0	(4A)

VN(7:0) **Version Number of Chip**

05_H Version 2.1

Receive Equalizer Status (Read)

	7							0
RES	EV1	EV0		RES4	RES3	RES2	RES1	RES0 (x4B)

EV(1:0) **Equalizer Status Valid**

These bits informs the user about the current state of the receive equalization network. Only valid if LIM1.EQON is set.

00 equalizer status not valid, still adapting

01 equalizer status valid

10 equalizer status not valid

11 equalizer status valid but high noise floor

RES(4:0) **Receive Equalizer Status**

The current line attenuation status in steps of about 1.4 dB are displayed in these bits. Only valid if bits EV1/0 = 01 and LIM1.EQON = 1.
Accuracy: ± 2 digit, based on temperature influence and noise amplitude variations.

00000 minimum attenuation: 0 dB

...

11001 maximum attenuation: -36 dB

Framer Receive Status Register 0 (Read)

	7							0	
FRS0	LOS	AIS	LFA	RRA			LMFA	FSRF	(x4C)

LOS **Loss of Signal (Red Alarm)**

Detection:
This bit is set when the incoming signal has “no transitions“ (analog interface) or logical zeros (digital interface) in a time interval of T consecutive pulses, where T is programmable by PCD register:
Total account of consecutive pulses: 16 < T < 4096.

Analog interface: The receive signal level where “no transition” is declared is defined by the programmed value of LIM1.RIL(2:0).

Recovery:
Analog interface: The bit is reset in short haul mode when the incoming signal has transitions with signal levels greater than the programmed receive input level (LIM1.RIL(2:0)) for at least M pulse periods defined by register PCR in the PCD time interval. In long haul mode additionally bit RES.6 must be set for at least 250 µs.
Digital interface: The bit is reset when the incoming data stream contains at least M ones defined by register PCR in the PCD time interval.

With the rising edge of this bit an interrupt status bit (ISR2.LOS) is set. For additionally recovery conditions refer also to register LIM2.LOS1. The bit is set during alarm simulation and reset if FRS2.ESC = 0, 3, 4, 6,7 and no alarm condition exists.

AIS **Alarm Indication Signal (Blue Alarm)**

This bit is set when the conditions defined by bit FMR4.AIS3 are detected. The flag stays active for at least one multiframe.

With the rising edge of this bit an interrupt status bit (ISR2.AIS) is set. It is reset with the beginning of the next following multiframe if no alarm condition is detected.

The bit is set during alarm simulation and reset if FRS2.ESC = 0, 3, 4, 7 and no alarm condition exists.

LFA **Loss of Frame Alignment**

The flag is set if pulseframe synchronization has been lost. The conditions are specified by bit FMR4.SSC1/0. Setting this bit causes an interrupt (ISR2.LFA).

The flag is cleared when synchronization has been regained. Additionally interrupt status ISR2.FAR is set with clearing this bit.

RRA **Receive Remote Alarm (Yellow Alarm)**

The flag is set after detecting remote alarm (yellow alarm). Conditions for setting/resetting are defined by bit RC0.RRAM.

With the rising edge of this bit an interrupt status bit ISR2.RA is set.

With the falling edge of this bit an interrupt status bit ISR2.RAR is set.

The bit is set during alarm simulation and reset if FRS2.ESC = 0, 3, 4,5,7 and no alarm condition exists.

LMFA **Loss Of Multiframe Alignment**

Set in F12 or F72 format when 2 out of 4 (or 5 or 6) multiframe alignment patterns are incorrect.

Additionally the interrupt status bit ISR2.LMFA is set.

Cleared after multiframe synchronization has been regained. With the falling edge of this bit an interrupt status bit ISR2.MFAR is generated.

FSRF **Frame Search Restart Flag**

Toggles when no framing candidate (pulseframing or multiframing) is found and a new frame search is started.

Framer Receive Status Register 1 (Read)

	7							0	
FRS1	EXZD	PDEN		LLBDD	LLBAD		XLS	XLO	(x4D)

EXZD **Excessive Zeros Detected**

Significant only if excessive zeros detection is enabled (FMR2.EXZE = 1).

Set after detecting of more than 7 (B8ZS code) or more than 15 (AMI code) contiguous zeros in the received bit stream. This bit is cleared on read.

PDEN **Pulse Density Violation Detected**

The pulse density of the received data stream is below the requirement defined by ANSI T1. 403 or more than 14 consecutive zeros are detected. With the violation of the pulse density this bit is set and remains active until the pulse density requirement is fulfilled for 23 consecutive ’1’-pulses.
Additionally an interrupt status ISR0.PDEN is generated with the rising edge of PDEN.

LLBDD **Line Loop Back Deactivation Signal Detected**

This bit is set in case of the LLB deactivate signal is detected and then received over a period of more than 33,16 ms with a bit error rate less than 10^{-2}. The bit remains set as long as the bit error rate does not exceed 10^{-2}.

If framing is aligned, the first bit position of any frame is not taken into account for the error rate calculation.

Any change of this bit causes an LLBSC interrupt.

LLBAD **Line Loopback Activation Signal Detected/PRBS Status**

Depending on bit LCR1.EPRM the source of this status bit changed.

LCR1.EPRM = 0: This bit is set in case of the LLB activate signal is detected and then received over a period of more than 33,16 ms with a bit error rate less than 10^{-2}. The bit remains set as long as the bit error rate does not exceed 10^{-2}.

If framing is aligned, the first bit position of any frame is not taken into account for the error rate calculation.

Any change of this bit causes an LLBSC interrupt.

PRBS Status

LCR1.EPRM = 1: The current status of the PRBS synchronizer is indicated in this bit. It is set high if the synchronous state is reached even in the presence of a bit error rate of up to 10^{-3}. A data stream containing all zeros or all ones with/without framing bits is also a valid pseudo random bit sequence.

XLS **Transmit Line Short**

Significant only if the ternary line interface is selected by LIM1.DRS = 0.

0 Normal operation. No short is detected.

1 The XL1 and XL2 are shortened for at least 3 pulses. As a reaction of the short the pins XL1 and XL2 are automatically forced into a high impedance state if bit XPM2.DAXLT is reset. After 128 consecutive pulse periods the outputs XL1/2 are activated again and the internal transmit current limiter is checked. If a short between XL1/2 is still further active the outputs XL1/2 are in high impedance state again. When the short disappears pins XL1/2 are activated automatically and this bit is reset. With any change of this bit an interrupt ISR1.XLSC is generated. In case of XPM2.XLT is set this bit is frozen.

XLO **Transmit Line Open**

0 Normal operation

1 This bit is set if at least 32 consecutive zeros were sent on pins XL1/XL2 or XDOP/XDON. This bit is reset with the first transmitted pulse. With the rising edge of this bit an interrupt ISR1.XLSC is set. In case of XPM2.XLT is set this bit is frozen.

Framer Receive Status Register 2 (Read)

	7							0	
FRS2	ESC2	ESC1	ESC0						(x4E)

ESC(2:0) **Error Simulation Counter**

This three-bit counter is incremented by setting bit FMR0.SIM. The state of the counter determines the function to be tested.

For complete checking of the alarm indications, eight simulation steps are necessary (FRS2.ESC = 0 after a complete simulation).

Table 69 Alarm Simulation States

Tested Alarms ESC(2:0) =	0	1	2	3	4	5	6	7
LFA			×				×	
LMFA			×				×	
RRA (bit2 = 0)		×						
RRA (S-bit frame 12)			×					
RRA (DL-pattern)							×	
LOS[1)]		×	×			×		
EBC (F12,F72)			×				×	
EBC (only ESF)		×	×			×	×	
AIS[1)]		×	×			×	×	
FEC			×				×	
CVC		×	×			×		
CEC (only ESF)		×	×			×	×	
RSP		×						
RSN						×		
XSP		×						
XSN						×		
BEC[1)]		×	×			×		
COEC			×				×	

[1)] only active during FMR0.SIM = 1

Some of these alarm indications are simulated only if the QuadFALC is configured in the appropriate mode. At simulation steps 0, 3, 4, and 7 pending status flags are reset

automatically and clearing of the error counters and interrupt status registers ISR(4:0) should be done. Incrementing the simulation counter should not be done at time intervals shorter than 1.5 ms (F4, F12, F72) or 3 ms (ESF). Otherwise, reactions of initiated simulations might occur at later steps. Control bit FMR0.SIM has to be held stable at high or low level for at least one receive clock period before changing it again.

Framing Error Counter (Read)

	7		0	
FECL	FE7		FE0	(x50)
	7		0	
FECH	FE15		FE8	(x51)

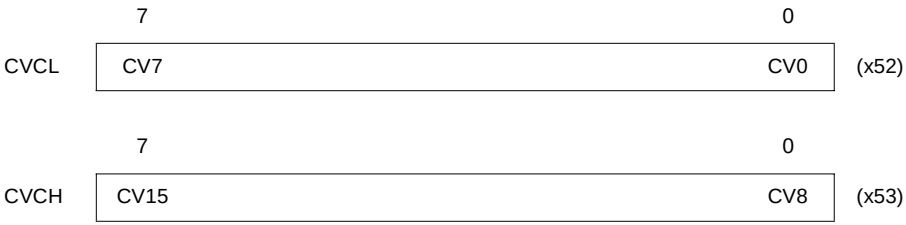
FE(15:0) **Framing Errors**

This 16-bit counter is incremented when incorrect FT and FS-bits in F4, F12 and F72 format or incorrect FAS-bits in ESF format are received.
Framing errors are counted during synchronous state only (but even if multiframe synchronous state is not reached yet). The error counter does not roll over.
During alarm simulation, the counter is incremented twice.

Clearing and updating the counter is done according to bit FMR1.ECM.
If this bit is reset the error counter is permanently updated in the buffer. For correct read access of the error counter bit DEC.DFEC has to be set. With the rising edge of this bit updating the buffer is stopped and the error counter is reset. Bit DEC.DFEC is automatically reset with reading the error counter high byte.

If FMR1.ECM is set every second (interrupt ISR3.SEC) the error counter is latched and then automatically reset. The latched error counter state should be read within the next second.

Code Violation Counter (Read)



CV(15:0) **Code Violations**

No function if NRZ or CMI code has been enabled.

If the B8ZS code (bit FMR0.RC1/0 = 11) is selected, the 16-bit counter is incremented by detecting violations which are not due to zero substitution. If FMR2.EXZE is set, additionally excessive zero strings (more than 7 contiguous zeros) are detected and counted.

If simple AMI coding is enabled (FMR0.RC0/1 = 10) all bipolar violations are counted. If FMR2.EXZE is set, additionally excessive zero strings (more than 15 contiguous zeros) are detected and counted. The error counter does not roll over.

During alarm simulation, the counter is incremented continuously with every second received bit.

Clearing and updating the counter is done according to bit FMR1.ECM.
If this bit is reset the error counter is permanently updated in the buffer. For correct read access of the error counter bit DEC.DCVC has to be set. With the rising edge of this bit updating the buffer is stopped and the error counter is reset. Bit DEC.DCVC is automatically reset with reading the error counter high byte.

If FMR1.ECM is set every second (interrupt ISR3.SEC) the error counter is latched and then automatically reset. The latched error counter state should be read within the next second.

CRC Error Counter (Read)

	7		0	
CECL	CR7		CR0	(x54)

	7		0	
CECH	CR15		CR8	(x55)

CR(15:0) **CRC Errors**

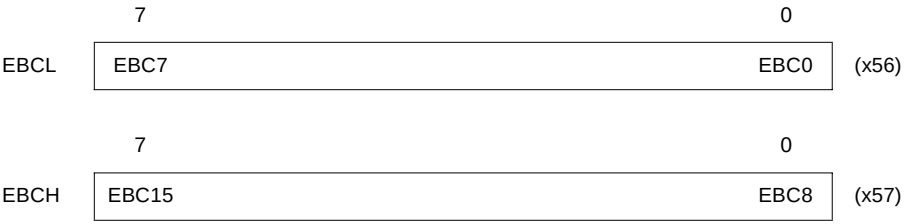
No function if CRC6 procedure or ESF format are disabled.

In ESF mode, the 16-bit counter is incremented when a multiframe has been received with a CRC error. CRC errors are not counted during asynchronous state. The error counter does not roll over.
During alarm simulation, the counter is incremented once per multiframe.

Clearing and updating the counter is done according to bit FMR1.ECM.
If this bit is reset the error counter is permanently updated in the buffer. For correct read access of the error counter bit DEC.DCEC has to be set. With the rising edge of this bit updating the buffer is stopped and the error counter is reset. Bit DEC.DCEC is automatically reset with reading the error counter high byte.

If FMR1.ECM is set every second (interrupt ISR3.SEC) the error counter is latched and then automatically reset. The latched error counter state should be read within the next second.

Errored Block Counter (Read)



EBC(15:0) **Errored Block Counter**

In ESF format this 16-bit counter is incremented once per multiframe if a multiframe has been received with a CRC error or an errored frame alignment has been detected. CRC and framing errors are not counted during asynchronous state. The error counter does not roll over.

In F4/12/72 format an errored block contain 4/12 or 72 frames. Incrementing is done once per multiframe if framing errors has been detected.
During alarm simulation, the counter is incremented in ESF format once per multiframe and in F4/12/72 format only one time.

Clearing and updating the counter is done according to bit FMR1.ECM.

If this bit is reset the error counter is permanently updated in the buffer. For correct read access of the error counter bit DEC.DEBC has to be set. With the rising edge of this bit updating the buffer is stopped and the error counter is reset. Bit DEC.DEBC is automatically reset with reading the error counter high byte.

If FMR1.ECM is set every second (interrupt ISR3.SEC) the error counter is latched and then automatically reset. The latched error counter state should be read within the next second.

Bit Error Counter (Read)

	7		0	
BECL	BEC7		BEC0	(x58)

	7		0	
BECH	BEC15		BEC8	(x59)

BEC(15:0) **Bit Error Counter**

If the PRBS monitor is enabled by LCR1.EPRM = 1 this 16-bit counter is incremented with every received PRBS bit error in the PRBS synchronous state FRS1.LLBAD = 1. The error counter does not roll over.

During alarm simulation, the counter is incremented continuously with every second received bit.

Clearing and updating the counter is done according to bit FMR1.ECM.

If this bit is reset the error counter is permanently updated in the buffer. For correct read access of the PRBS bit error counter bit DEC.DBEC has to be set. With the rising edge of this bit updating the buffer is stopped and the error counter is reset. Bit DEC.DBEC is automatically reset with reading the error counter high byte.

If FMR1.ECM is set every second (interrupt ISR3.SEC) the error counter is latched and then automatically reset. The latched error counter state should be read within the next second.

COFA Event Counter (Read)

	7			0	
COEC	COE7	COE2	COE1	COE0	(x5A)

COE(7:2) **Multiframe Counter**

If GCR.ECMC = 1 this 6 bit counter increments with each multiframe period in the asynchronous state FRS0.LFA/LMFA = 1. The error counter does not roll over.

COE(1:0) **Change of Frame Alignment Counter**

If GCR.ECMC = 1 this 2 bit counter increments with each detected change of frame/multiframe alignment. The error counter does not roll over.
During alarm simulation, the counter is incremented once per multiframe.

Clearing and updating the counter is done according to bit FMR1.ECM.

If this bit is reset the error counter is permanently updated in the buffer. For correct read access of the event counter bit DEC.DCOEC has to be set. With the rising edge of this bit updating the buffer is stopped and the error counter is reset. Bit DEC.DCOEC is automatically reset with reading the error counter high byte on address $5B_H$. Data read on $5B_H$ is not defined.

If FMR1.ECM is set every second (interrupt ISR3.SEC) the error counter is latched and then automatically reset. The latched error counter state should be read within the next second.

Receive DL-Bit Register 1 (Read)

	7							0	
RDL1	RDL17	RDL16	RDL15	RDL14	RDL13	RDL12	RDL11	RDL10	(x5C)

RDL1(7:0) **Receive DL-Bit**

Only valid if F12, F24 or F72 format is enabled.
The received FS/DL-Bits are shifted into this register. RDL10 is received in frame 1 and RDL17 in frame 15, if F24 format is enabled. RDL10 is received in frame 26 and RDL17 in frame 40, if F72 format is enabled.
In F12 format the FS-Bits of a complete multiframe is stored in this register. RDL10 is received in frame 2 and RDL15 in frame 12.
This register is updated with every receive multiframe begin interrupt ISR0.RMB.

Receive DL-Bit Register 2 (Read)

	7							0	
RDL2	RDL27	RDL26	RDL25	RDL24	RDL23	RDL22	RDL21	RDL20	(x5D)

RDL2(7:0) **Receive DL-Bit**

Only valid if F24 or F72 format is enabled.
The received DL-Bits are shifted into this register. RDL20 is received in frame 17 and RDL23 in frame 23, if F24 format is enabled. RDL20 is received in frame 42 and RDL27 in frame 56, if F72 format is enabled.
This register is updated with every receive multiframe begin interrupt ISR0.RMB.

Receive DL-Bit Register 3 (Read)

	7							0	
RDL3	RDL37	RDL36	RDL35	RDL34	RDL33	RDL32	RDL31	RDL30	(x5E)

RDL3(7:0) **Receive DL-Bit**

Only valid if F72 format is enabled.
The received DL-Bits are shifted into this register. RDL30 is received in frame 58 and RDL37 in frame 72, if F72 format is enabled.
This register is updated with every receive multiframe begin interrupt ISR0.RMB.

Receive Signaling Pointer 1 (Read)

Value after reset: 00_H

	7							0	
RSP1	RS8C	RS7C	RS6C	RS5C	RS4C	RS3C	RS2C	RS1C	(x62)

RS(8:1)C **Receive Signaling Register RS(8:1) Changed**

A one in each bit position indicates that the received signaling data in the corresponding RS(8:1) registers are updated. Bit RS1C is the pointer for register RS1,... while RS8C points to RS8.

Receive Signaling Pointer 2 (Read)

Value after reset: 00_H

	7							0	
RSP2					RS12C	RS11C	RS10C	RS9C	(x63)

RS(12:9)C **Receive Signaling Register RS(12:9) Changed**

A one in each bit position indicates that the received signaling data in the corresponding RS(12:9) registers are updated. Bit RS9C is the pointer for register RS9, while RS12C points to RS12

Signaling Status Register (Read)

	7							0	
SIS	XDOV	XFW	XREP	IVB	RLI	CEC	SFS	BOM	(x64)

XDOV **Transmit Data Overflow**

More than 32 bytes have been written to the XFIFO.
This bit is reset by:

– a transmitter reset command XRES or

– when all bytes in the accessible half of the XFIFO have been moved in the inaccessible half.

XFW **Transmit FIFO Write Enable**

Data can be written to the XFIFO.

XREP **Transmission Repeat**

Status indication of CMDR.XREP.

IVB **Invalid BOM Frame Received**

0 valid BOM frame (11111111, 0xxxxxx0) received.

1 invalid BOM frame received.

RLI **Receive Line Inactive**

Neither flags as interframe time fill nor frames are received in the signaling time slot.

CEC **Command Executing**

0 No command is currently executed, the CMDR register can be written to.

1 A command (written previously to CMDR) is currently executed, no further command can be temporarily written in CMDR register.

Note: CEC is active at most 2.5 periods of the current system data rate.

SFS **Status Freeze Signaling**

0 freeze signaling status inactive.

1 freeze signaling status active.

BOM **Bit Oriented Message**

Significant only in ESF frame format and auto switching mode is enabled.

0 HDLC mode

1 BOM mode

Receive Signaling Status Register (Read)

	7							0	
RSIS	VFR	RDO	CRC16	RAB	HA1	HA0	HFR	LA	(x65)

RSIS relates to the last received HDLC or BOM frame; it is copied into RFIFO when end-of-frame is recognized (last byte of each stored frame).

VFR **Valid Frame**

Determines whether a valid frame has been received.

1 valid

0 invalid

An invalid frame is either

– a frame which is not an integer number of 8 bits (n×8 bits) in length (e.g. 25 bits), or

– a frame which is too short taking into account the operation mode selected by MODE (MDS(2:0)) and the selection of receive CRC on/off (CCR2.RCRC) as follows:

- MDS(2:0) = 011 (16 bit Address),
  RCRC = 0: 4 bytes; RCRC = 1: 3 to 4 bytes
- MDS(2:0) = 010 (8 bit Address),
  RCRC = 0: 3 bytes; RCRC = 1: 2 to 3 bytes

Note: Shorter frames are not reported.

RDO **Receive Data Overflow**

A data overflow has occurred during reception of the frame.

Additionally, an interrupt can be generated
(refer to ISR1.RDO/IMR1.RDO).

CRC16 **CRC16 Compare/Check**

0 CRC check failed; received frame contains errors.

1 CRC check o.k.; received frame is error-free.

RAB **Receive Message Aborted**

This bit is set in SS7 mode, if the maximum number of octets (272+7) is exceeded. The received frame was aborted from the transmitting station. According to the HDLC protocol, this frame must be discarded by the receiver station.

HA1, HA0 **High Byte Address Compare**

Significant only if 2-byte address mode or SS7 mode has been selected.

In operating modes which provide high byte address recognition, the QuadFALC compares the high byte of a 2-byte address with the contents of two individually programmable registers (RAH1, RAH2) and the fixed values FE_H and FC_H (broadcast address).

Depending on the result of this comparison, the following bit combinations are possible (SS7 support not active):

00 RAH2 has been recognized

01 Broadcast address has been recognized

10 RAH1 has been recognized C/R = 0 (bit 1)

11 RAH1 has been recognized C/R = 1 (bit 1)

Note: If RAH1, RAH2 contain identical values, a match is indicated by '10' or '11'.

If Signaling System 7 support is activated (see MODE register), the bit functions are defined as follows:

00 not valid

01 Fill In signaling unit (FISU) detected

10 Link status signaling unit (LSSU) detected

11 Message signaling unit (MSU) detected

HFR **HDLC Frame Format**

0 A BOM frame was received.

1 A HDLC frame was received.

Note: Bits RSIS.(7:2) and RSIS.0 are not valid with a BOM frame. This means, if HFR = 0, all other bits of RSIS have to be ignored
Not valid in SS7 mode. Bit HFR has to be ignored, if SS7 mode is selected.

LA **Low Byte Address Compare**

Significant in HDLC modes only.

The low byte address of a 2-byte address field, or the single address byte of a 1-byte address field is compared to two registers. (RAL1, RAL2).

0 RAL2 has been recognized
1 RAL1 has been recognized

Note: Not valid in SS7 mode. Bit LA has to be ignored, if SS7 mode is selected.

Receive Byte Count Low (Read)

	7						0	
RBCL	RBC7						RBC0	(x66)

Together with RBCH (bits RBC(11:8)), indicates the length of a received frame (1 to 4095 bytes). Bits RBC(4:0) indicate the number of valid bytes currently in RFIFO. These registers must be read by the CPU following a RME interrupt.

Received Byte Count High (Read)

Value after reset: 000_{xxxxx}

	7							0	
RBCH				OV	RBC11	RBC10	RBC9	RBC8	(x67)

OV **Counter Overflow**

More than 4095 bytes received.

RBC(11:8) **Receive Byte Count (most significant bits)**

Together with RBCL (bits RBC7...0) indicates the length of the received frame.

Interrupt Status Register 0 (Read)

Value after reset: 00_H

	7							0	
ISR0	RME	RFS/BIV	ISF	RMB	RSC	CRC6	PDEN	RPF	(x68)

All bits are reset when ISR0 is read.

If bit GCR.VIS is set, interrupt statuses in ISR0 are flagged although they are masked by register IMR0. However, these masked interrupt statuses neither generate a signal on INT, nor are visible in register GIS.

RME **Receive Message End**

One complete message of length less than 32 bytes, or the last part of a frame at least 32 bytes long is stored in the receive FIFO, including the status byte.

The complete message length can be determined reading the RBCH, RBCL registers, the number of bytes currently stored in RFIFO is given by RBC(4:0). Additional information is available in the RSIS register.

RFS/BIV **Receive Frame Start**

This is an early receiver interrupt activated after the start of a valid frame has been detected, i.e. after an address match (in operation modes providing address recognition), or after the opening flag (transparent mode 0) is detected, delayed by two bytes. After a RFS interrupt, the contents of RAL1and RSIS.3-1 are valid and can be read by the CPU.

BOM Frame Invalid

Only valid if CCR2.RBFE is set.

When the BOM receiver left the valid BOM status (detecting 7 out of 10 equal BOM frames) this interrupt is generated.

ISF **Incorrect Sync Format**

The QuadFALC did not detect eight consecutive ones within 32 bits in BOM mode. Only valid if BOM receiver has been activated.

RMB **Receive Multiframe Begin**

This bit is set with the beginning of a received multiframe of the receive line timing.

RSC **Received Signaling Information Changed**

This interrupt bit is set during each multiframe in which signaling information on at least one channel changes its value from the previous multiframe. This interrupt only occurs in the synchronous state. The registers RS(12:1) should be read within the next 3 ms otherwise the contents is lost.

CRC6 **Receive CRC6 Error**

0 No CRC6 error occurs.

1 The CRC6 check of the last received multiframe failed.

PDEN **Pulse Density violation**

The pulse density violation of the received data stream defined by ANSI T1. 403 is violated. More than 14 consecutive zeros or less than N ones in each and every time window of 8×(N+1) data bits (N = 23) are detected. If GCR.SCI is set high this interrupt status bit is activated with every change of state of FRS1.PDEN.

RPF **Receive Pool Full**

32 bytes of a frame have arrived in the receive FIFO. The frame is not yet received completely.

Interrupt Status Register 1 (Read)

	7							0	
ISR1	CASE	RDO	ALLS	XDU	XMB	SUEX	XLSC	XPR	(x69)

All bits are reset when ISR1 is read.

If bit GCR.VIS is set, interrupt statuses in ISR1 are flagged although they are masked by register IMR1. However, these masked interrupt statuses neither generate a signal on INT, nor are visible in register GIS.

CASE **Transmit CAS Register Empty**

In ESF format this bit is set with the beginning of a transmitted multiframe related to the internal transmitter timing. In F12 and F72 format this interrupt occurs every 24 frames to inform the user that new bit robbing data may be written to the XS(12:1) registers. This interrupt is generated only if the serial signaling access on the system highway is not enabled.

RDO **Receive Data Overflow**

This interrupt status indicates that the CPU did not respond fast enough to an RPF or RME interrupt and that data in RFIFO has been lost. Even when this interrupt status is generated, the frame continues to be received when space in the RFIFO is available again.

Note: Whereas the bit RSIS.RDO in the frame status byte indicates whether an overflow occurred when receiving the frame currently accessed in the RFIFO, the ISR1.RDO interrupt status is generated as soon as an overflow occurs and does not necessarily pertain to the frame currently accessed by the processor.

ALLS **All Sent**

This bit is set if the last bit of the current frame has been sent completely and XFIFO is empty. This bit is valid in HDLC mode only.

XDU **Transmit Data Underrun**

Transmitted frame was terminated with an abort sequence because no data was available for transmission in XFIFO and no XME was issued.

Note: Transmitter and XFIFO are reset and deactivated if this condition occurs. They are reactivated not before this interrupt status register has been read. Thus, XDU should not be masked by register IMR1.

XMB **Transmit Multiframe Begin**

This bit is set with the beginning of a transmitted multiframe related to the internal transmit line interface timing.

SUEX **Signaling Unit Error Threshold Exceeded**

Masks the indication by interrupt that the selected error threshold for SS7 signaling units has been exceeded.

0 signaling unit error count below selected threshold

1 signaling unit error count exceeded selected threshold

Note: SUEX is only valid, if SS7 mode is selected.
If SUEX is caused by an aborted/invalid frame, the interrupt will be issued regularly until a valid frame is received (e.g. a FISU).

XLSC **Transmit Line Status Change**

XLSC is set with the rising edge of the bit FRS1.XLO or with any change of bit FRS1.XLS.

The actual status of the transmit line monitor can be read from the FRS1.XLS and FRS1.XLO.

XPR **Transmit Pool Ready**

A data block of up to 32 bytes can be written to the transmit FIFO. XPR enables the fastest access to XFIFO. It has to be used for transmission of long frames, back-to-back frames or frames with shared flags.

Interrupt Status Register 2 (Read)

	7							0	
ISR2	FAR	LFA	MFAR	LMFA	AIS	LOS	RAR	RA	(x6A)

All bits are reset when ISR2 is read.

If bit GCR.VIS is set, interrupt statuses in ISR2 are flagged although they are masked by register IMR2. However, these masked interrupt statuses neither generate a signal on INT, nor are visible in register GIS.

FAR **Frame Alignment Recovery**

The framer has reached synchronization. Set with the falling edge of bit FRS0.LFA.

It is set also after alarm simulation is finished and the receiver is still synchronous.

LFA **Loss of Frame Alignment**

The framer has lost synchronization and bit FRS0.LFA is set.
It is set during alarm simulation.

MFAR **Multiframe Alignment Recovery**

Set when the framer has reached multiframe alignment in F12 or F72 format. With the negative transition of bit FRS0.LMFA this bit is set. It is set during alarm simulation.

LMFA **Loss of Multiframe Alignment**

Set when the framer has lost the multiframe alignment in F12 or F72 format. With the positive transition of bit FRS0.LMFA this bit is set. It is set during alarm simulation.

AIS **Alarm Indication Signal (Blue Alarm)**

This bit is set when an alarm indication signal is detected and bit FRS0.AIS is set. If GCR.SCI is set high this interrupt status bit is activated with every change of state of FRS0.AIS.
It is set during alarm simulation.

LOS **Loss of Signal (Red Alarm)**

This bit is set when a loss of signal alarm is detected in the received data stream and FRS0.LOS is set. If GCR.SCI is set high this interrupt status bit is activated with every change of state of FRS0.LOS.
It is set during alarm simulation.

RAR **Remote Alarm Recovery**

Set if a remote alarm (yellow alarm) is cleared and bit FRS0.RRA is reset. It is set also after alarm simulation is finished and no remote alarm is detected.

RA **Remote Alarm**

A remote alarm (yellow alarm) is detected. Set with the rising edge of bit FRS0.RRA. It is set during alarm simulation.

Interrupt Status Register 3 (Read)

	7							0	
ISR3	ES	SEC			LLBSC		RSN	RSP	(x6B)

All bits are reset when ISR3 is read.

If bit GCR.VIS is set, interrupt statuses in ISR3 are flagged although they are masked by register IMR3. However, these masked interrupt statuses neither generate a signal on INT, nor are visible in register GIS.

ES **Errored Second**

This bit is set if at least one enabled interrupt source by ESM is set during the time interval of one second. Interrupt sources of ESM register:

LFA = Loss of frame alignment detected
FER = Framing error received
CER = CRC error received
AIS = Alarm indication signal (blue alarm)
LOS = Loss of signal (red alarm)
CVE = Code violation detected
SLIP = Transmit slip or receive slip positive/negative detected

SEC **Second Timer**

The internal one second timer has expired. The timer is derived from clock RCLK.

LLBSC **Line Loop Back Status Change/PRBS Status Change**

Depending on bit LCR1.EPRM the source of this interrupt status changed:

LCR1.EPRM = 0: This bit is set if the LLB activate signal or the LLB deactivate signal is detected over a period of 33,16 ms with a bit error rate less than 10^{-2}.

The LLBSC bit is also set, if the current detection status is left, i.e., if the bit error rate exceeds 10^{-2}.

The actual detection status can be read from the FRS1.LLBAD and FRS1.LLBDD, respectively.

PRBS Status Change

LCR1.EPRM = 1: With any change of state of the PRBS synchronizer this bit is set. The current status of the PRBS synchronizer is indicated in FRS1.LLBAD.

RSN **Receive Slip Negative**

The frequency of the receive route clock is greater than the frequency of the receive system interface working clock based on 1.544 MHz. A frame is skipped. It is set during alarm simulation.

RSP **Receive Slip Positive**

The frequency of the receive route clock is less than the frequency of the receive system interface working clock based on 1.544 MHz. A frame is repeated. It is set during alarm simulation.

Interrupt Status Register 4 (Read)

	7							0	
ISR4	XSP	XSN							(x6C)

All bits are reset when ISR4 is read.

If bit GCR.VIS is set, interrupt statuses in ISR4 are flagged although they are masked by register IMR4. However, these masked interrupt statuses neither generate a signal on INT, nor are visible in register GIS.

XSP **Transmit Slip Positive**

The frequency of the transmit clock is less than the frequency of the transmit system interface working clock based on 1.544 MHz. A frame is repeated. After a slip has performed writing of register XC1 is not necessary.

XSN **Transmit Slip Negative**

The frequency of the transmit clock is greater than the frequency of the transmit system interface working clock based on 1.544 MHz. A frame is skipped. After a slip has performed writing of register XC1 is not necessary.

Global Interrupt Status Register (Read)

Value after reset: 00_H

	7							0	
GIS				ISR4	ISR3	ISR2	ISR1	ISR0	(x6E)

This status register points to pending interrupts sourced by ISR(4:0).

Channel Interrupt Status Register (Read)

Value after reset: $x0000000_B$

	7							0	
CIS	PLLL	0	0	0	GIS4	GIS3	GIS2	GIS1	(6F)

This status register points to pending interrupts sourced by the GIS registers of each channel

PLLL: PLL locked status: 1 if PLL is locked, 0 if PLL is unlocked

GIS4 register GIS of channel 4

GIS3 register GIS of channel 3

GIS2 register GIS of channel 2

GIS1 register GIS of channel 1

Undefined bit positions CIS(6:4) shall be ignored.

Receive Signaling Register (Read)

Value after reset: not defined

Table 70 Receive Signaling Registers (T1/J1)

	7							0	
RS1	A1	B1	C1/A2	D1/B2	A2/A3	B2/B3	C2/A4	D2/B4	(x70)
RS2	A3/A5	B3/B5	C3/A6	D3/B6	A4/A7	B4/B7	C4/A8	D4/B8	(x71)
RS3	A5/A9	B5/B9	C5/A10	D5/B10	A6/A11	B6/B11	C6/A12	D6/B12	(x72)
RS4	A7/A13	B7/B13	C7/A14	D7/B14	A8/A15	B8/B15	C8/A16	D8/B16	(x73)
RS5	A9/A17	B9/B17	C9/A18	D9/B18	A10/A19	B10/B19	C10/A20	D10/B20	(x74)
RS6	A11/A21	B11/B21	C11/A22	D11/B22	A12/A23	B12/B23	C12/A24	D12/B24	(x75)
RS7	A13/A1	B13/B1	C13/A2	D13/B2	A14/A3	B14/B3	C14/A4	D14/B4	(x76)
RS8	A15/A5	B15/B5	C15/A6	D15/B6	A16/A7	B16/B7	C16/A8	D16/B8	(x77)
RS9	A17/A9	B17/B9	C17/A10	D17/B10	A18/A11	B18/B11	C18/A12	D18/B12	(x78)
RS10	A19/A13	B19/B13	C19/A14	D19/B14	A20/A15	B20/B15	C20/A16	D20/B16	(x79)
RS11	A21/A17	B21/B17	C21/A18	D21/B18	A22/A19	B22/B19	C22/A20	D22/B20	(x7A)
RS12	A23/A21	B23/B21	C23/A22	D23/B22	A24/A23	B24/B23	C24/A24	D24/B24	(x7B)

Receive Signaling Register (12:1)

Each register contains the received bit robbing information for 8 DS0 channels. The received robbed bit signaling information of a complete ESF multiframe is compared to the previously received one. In F12/72 frame format the received signaling information of every 24 frames is compared to the previously received 24 frames. If the contents changed a Receive Signaling Changed interrupt ISR0.RSC is generated and informs the user that a new multiframe has to be read within the next 3 ms. Received data is stored in RS(12:1) registers. The RS1.7 is received in channel 1 frame 1 and RS12.0 in channel 24 frame 24 (ESF).

If requests for reading the RS(12:1) registers are ignored, received data might get lost.

Additionally a receive signaling data change pointer indicates an update of register RS(12:1). Refer also to register RSP1/2.
Access to RS(12:1) registers is only valid if the serial receive signaling access on the system highway is disabled.

11 Electrical Characteristics

11.1 Absolute Maximum Ratings

Parameter	Symbol	Limit Values	Unit
Ambient temperature under bias	T_A	– 40 to 85	°C
Storage temperature	T_{stg}	– 65 to 125	°C
IC supply voltage (pads, digital)	V_{DD}	– 0.3 to 3.60	V
IC supply voltage (core, digital)	V_{DDC}	– 0.3 to 1.98	V
IC supply voltage PLL (analog)	V_{DDP}	– 0.3 to 3.60	V
IC supply voltage receive (analog)	V_{DDR}	– 0.3 to 3.60	V
IC supply voltage transmit (analog)	V_{DDX}	– 0.3 to 3.60	V
Voltage on any pin with respect to ground[1)]	V_S	– 0.3 to 3.60	V
ESD robustness[2)] HBM: 1.5 kΩ, 100 pF	$V_{ESD,HBM}$	2000	V

1) except V_{DDC}

2) According to JEDEC standard JESD22-A114 (2000).

Attention: If the 1.8-V power supply is externally driven on V_{DDC}, the voltage on this pin must never exceed the 3.3-V supply voltages on pins V_{DD}, V_{DDP}, V_{DDX} and V_{DDR}, even during power up and power down of the circuit.

Attention: Stresses above those listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

11.2 Operating Range

Parameter	Symbol	Limit Values		Unit	Test Condition
		min.	max.		
Ambient temperature	T_A	-40	85	°C	
Supply voltages	V_{DD}	3.13	3.46	V	3.3 V ± 5%
	V_{DDP} [1]	3.13	3.46	V	3.3 V ± 5%
	V_{DDR} [1]	3.13	3.46	V	3.3 V ± 5%
	V_{DDC}	1.62	1.98	V	1.8 V ± 10%
	V_{DDX} [1]	3.13	3.46	V	3.3 V ± 5%
Analog input voltages	V_{IA}	0	3.60 [2]	V	3.3 V ± 5%
Digital input voltages	V_{ID}	0	3.46	V	3.3 V ± 5%
Ground	V_{SS} V_{SSP} V_{SSR} V_{SSX}	0	0	V	

[1] Voltage ripple less than 50 mV on these 3.3V supplies.

[2] Depending on the applied power supply level, signal clipping may occur due to activation of the ESD protection diodes if the signal level exceeds V_{DDR} + 0.3 V

Note: In the operating range, the functions given in the circuit description are fulfilled. V_{DD}, V_{DDP}, V_{DDR} and V_{DDX} have to be connected to the same voltage level, V_{SS}, V_{SSP}, V_{SSR} and V_{SSX} have to be connected to ground level.

11.3 DC Characteristics

Parameter	Symbol	Limit Values		Unit	Notes
		min.	max.		
Input low voltage	V_{IL}	– 0.4	0.8	V	1)
Input high voltage	V_{IH}	2.0	3.46	V	
Output low voltage	V_{OL}	V_{SS}	0.45	V	I_{OL} = + 2 mA 2)
Output high voltage	V_{OH}	2.4	V_{DD}	V	I_{OH} = - 2 mA 2)
Average power supply current (analog line interface mode)	I_{DDE1}		260	mA	E1 application 3) LIM1.DRS = 0
	I_{DDT1}		330	mA	T1 application 4) LIM1.DRS = 0
Average power supply current (digital line interface mode)	I_{DD}		150	mA	LIM1.DRS = 1 5)
Input leakage current	I_{IL11}		1	µA	$V_{IN} = V_{DD}$ 6); all except RDO
Input leakage current	I_{IL12}		1	µA	$V_{IN} = V_{SS}$ 6); all except RDO
Input pullup current	I_{IP}	2	15	µA	$V_{IN} = V_{SS}$
Output leakage current	I_{OZ1}		1	µA	V_{OUT} = *tristate* 1) $V_{SS} < V_{meas} < V_{DD}$ measured against V_{DD} and V_{SS}; all except XL1/2
Transmitter leakage current	I_{TL}		15.0	µA	XL1/2 = VDDX; XPM2.XLT = 1
			15.0	µA	XL1/2 = VSSX; XPM2.XLT = 1
Transmitter output impedance	R_X		3	Ω	applies to XL1and XL2 7)
Transmitter output current	I_X		105	mA	XL1, XL2 7)
Differential peak voltage of a mark (between XL1 and XL2)	V_X		2.15	V	

Parameter	Symbol	Limit Values		Unit	Notes
		min.	max.		
Receiver differential peak voltage of a mark (between RL1 and RL2)	V_R		V_{DDR}+0.3	V	RL1, RL2
Receiver input impedance	Z_R	50 (typical value)		kΩ	10)
Receiver sensitivity	S_{RSH}		10	dB	RL1, RL2 LIM0.EQON = 0 (short haul)
Receiver sensitivity	S_{RLH}		43 8)	dB	RL1, RL2 LIM0.EQON = 1 (E1, long haul)
			36		RL1, RL2 LIM0.EQON = 1 (T1/J1, long haul)
Receiver input threshold	V_{RTH}	45		%	LIM2.SLT(1:0) = 11 7)
		50			LIM2.SLT(1:0) = 10 7) default setting
		55			LIM2.SLT(1:0) = 00 7)
		67			LIM2.SLT(1:0) = 01 7)

Parameter	Symbol	Limit Values		Unit	Notes
		min.	max.		
Loss of signal detection limit[9)10)]	V_{LOS}	1.80 1.00 0.50 0.30 0.19 0.12 0.08 0.06 (typical values)		V	RIL(2:0) = 000 RIL(2:0) = 001 RIL(2:0) = 010 RIL(2:0) = 011 RIL(2:0) = 100 RIL(2:0) = 101 RIL(2:0) = 110 RIL(2:0) = 111 7)

1) Applies to all input pins except analog pins RLx

2) Applies to all output pins except pins XLx

3) Wiring conditions and external circuit configuration according to **Figure 112** and **Table 91** on **Page 451**.

4) Wiring conditions and external circuit configuration according to **Figure 112** and **Table 92** on **Page 452**.

5) System interface at 16 MHz; PRBS data.

6) Pin leakage is measured in a test mode with all internal pullups disabled. RDO pins are not tristatable, no leakage is measured.

7) Parameter not tested in production

8) To achieve maximum receiver sensitivity of -43 dB (E1) take special care on sufficient attenuation of crosstalk between Rx and Tx on board (e.g. in transformer) and run sequence as specified in **Table 49** on **Page 195**

9) Differential input voltage between RL1 and RL2

10) Values only valid for LIM0.EQON = 1, LOS detection limits set to PCR = 15_H, PCD = A_H, applied signal sequence +1,+,-1,0,...

Note: Typical characteristics specify mean values expected over the production spread. If not specified otherwise, typical characteristics apply at $T_A = 25\,°C$ and 3.3 V supply voltage.

11.4 AC Characteristics

11.4.1 Master Clock Timing

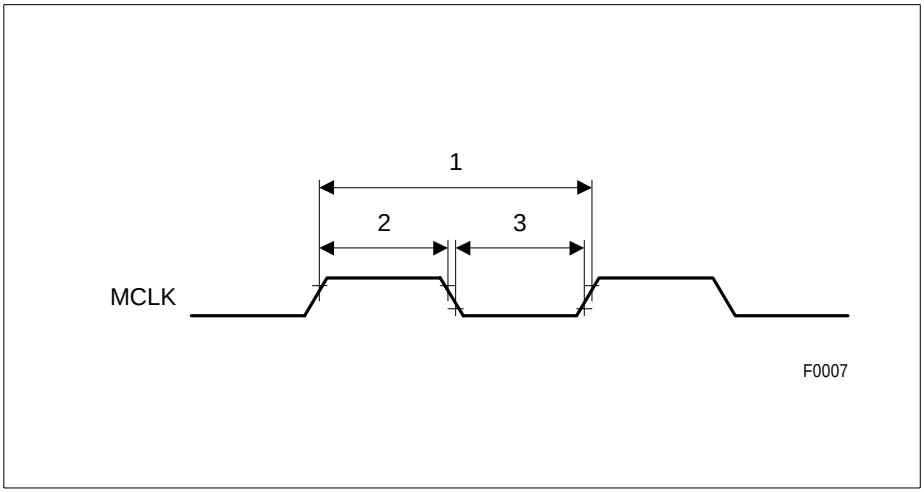


Figure 86 MCLK Timing

Table 71 MCLK Timing Parameters

No.	Parameter	Limit Values			Unit	Condition
		min.	typ.	max.		
1	Clock period of MCLK		488		ns	E1, fixed mode
			648		ns	T1/J1, fixed mode
		50		980.4	ns	E1/T1/J1, flexible mode
2	High phase of MCLK	40			%	
3	Low phase of MCLK	40			%	
	Clock accuracy	32[1)]		28[2)]	ppm	

[1)] if clock divider programming fits without rounding

[2)] if clock divider programming requires rounding

11.4.2 JTAG Boundary Scan Interface

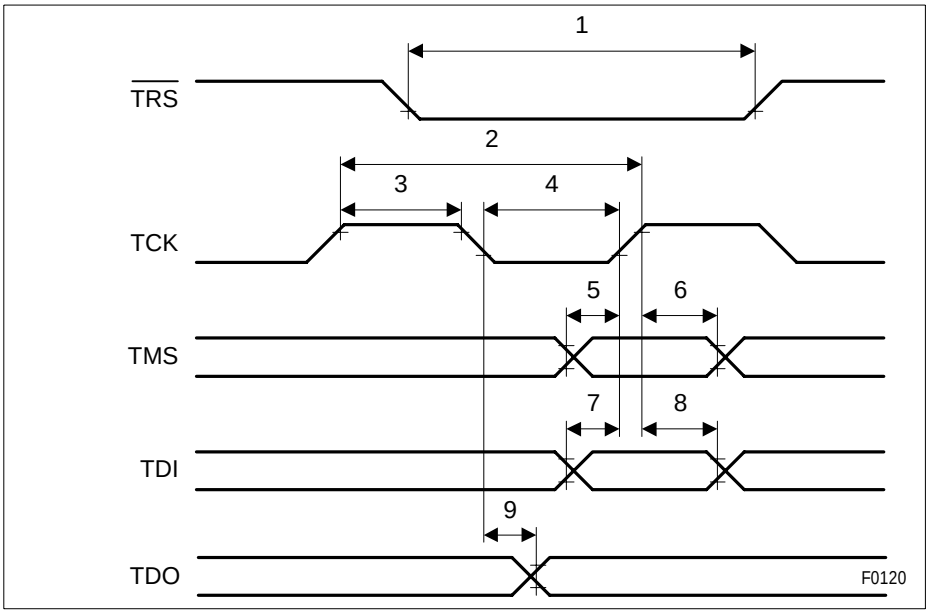


Figure 87 JTAG Boundary Scan Timing

Table 72 JTAG Boundary Scan Timing Parameter Values

No.	Parameter	Limit Values		Unit
		min.	max.	
1	$\overline{\text{TRS}}$ reset active low time	200		ns
2	TCK period	250		ns
3	TCK high time	80		ns
4	TCK low time	80		ns
5	TMS, TDI setup time	40		ns
6	TMS, TDI hold time	40		ns
7	TDATI setup time	40		ns
8	TDATI hold time	40		ns
9	TDO, TDATO output delay		100	ns

Identification Register: 32 bit; Version: $3_{H;}$ Part Number: $4D_H$, Manufacturer: 083_H

11.4.3 Reset

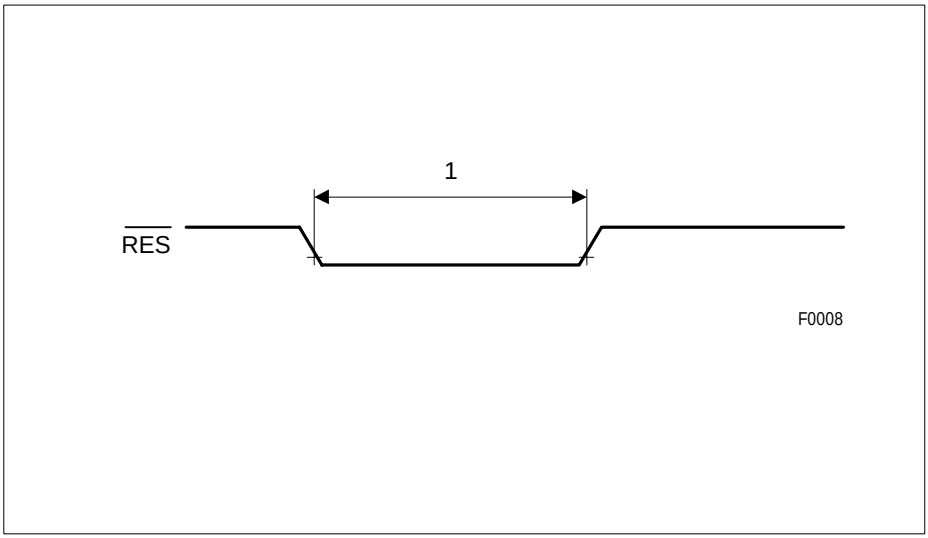


Figure 88 Reset Timing

Table 73 Reset Timing Parameter Values

No.	Parameter	Limit Values		Unit
		min.	max.	
1	$\overline{\text{RES}}$ pulse width low	10[1)]		µs

[1)] while MCLK is running

11.4.4 Microprocessor Interface

11.4.4.1 Intel Bus Interface Mode

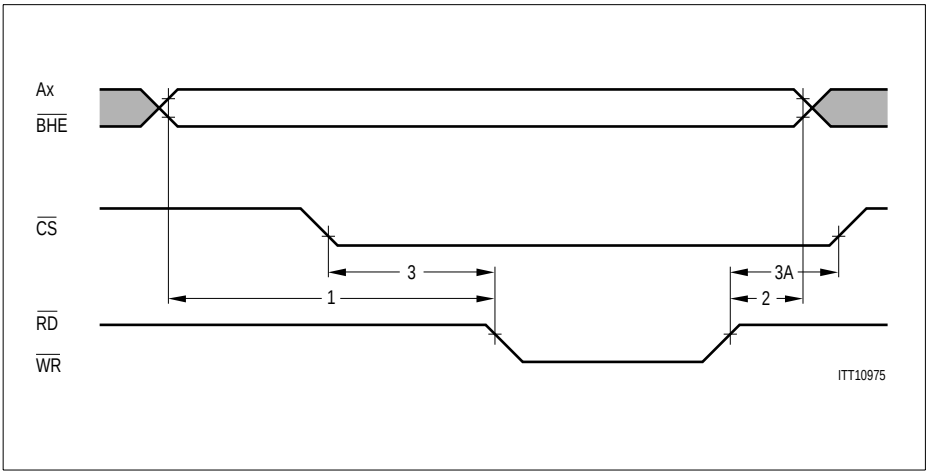


Figure 89 Intel Non-Multiplexed Address Timing

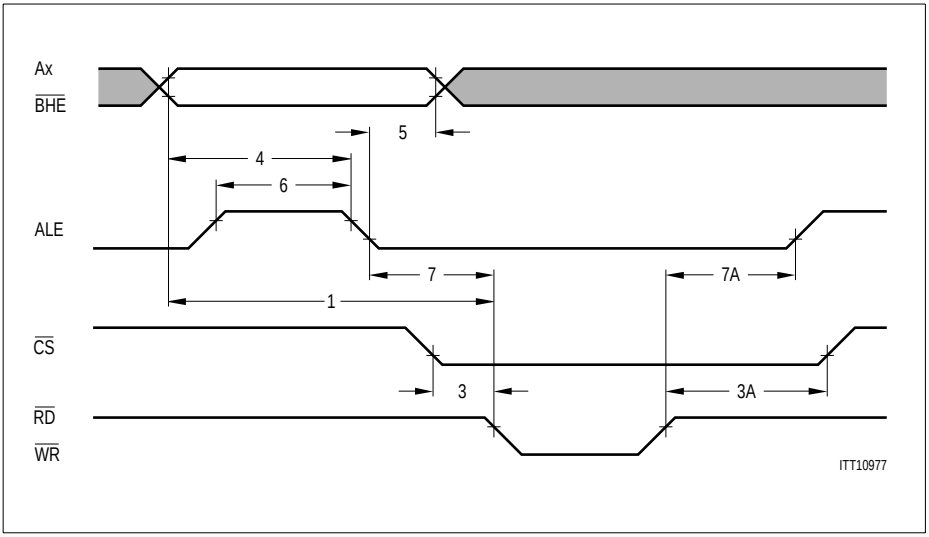


Figure 90 Intel Multiplexed Address Timing

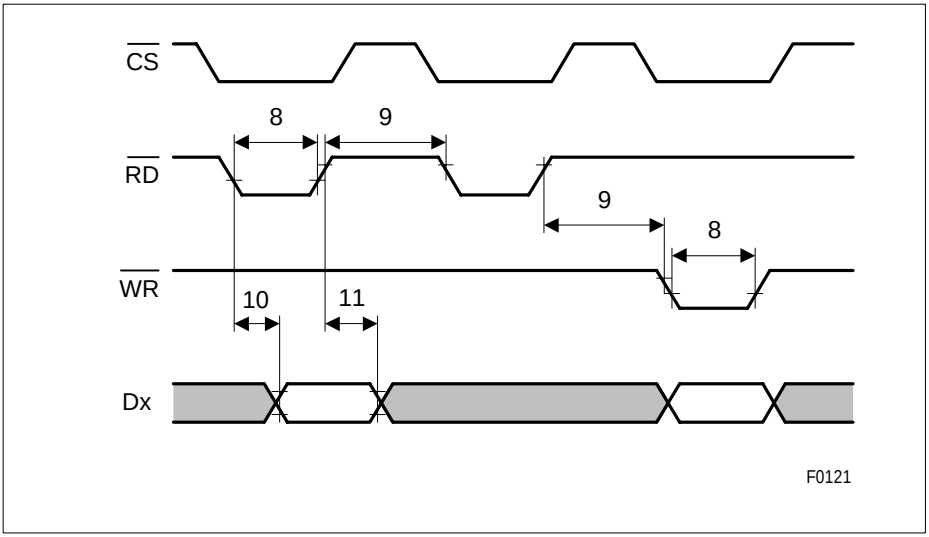


Figure 91 Intel Read Cycle Timing

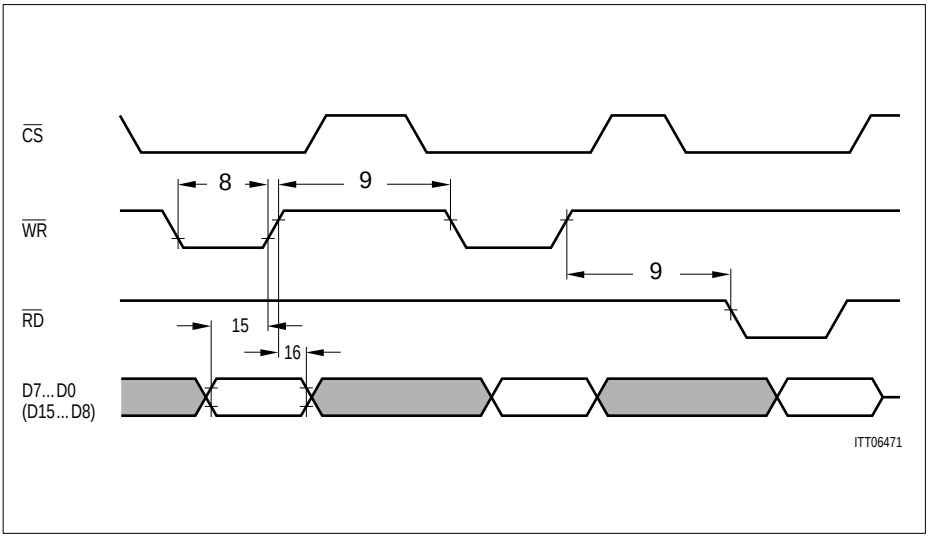


Figure 92 Intel Write Cycle Timing

Table 74 Intel Bus Interface Timing Parameter Values

No.	Parameter	Limit Values		Unit
		min.	max.	
1	Address, $\overline{BHE}$ setup time	5		ns
2	Address, $\overline{BHE}$ hold time	0		ns
3	$\overline{CS}$ setup time	0		ns
3A	$\overline{CS}$ hold time	0		ns
4	Address, $\overline{BHE}$ stable before ALE inactive	20		ns
5	Address, $\overline{BHE}$ hold after ALE inactive	10		ns
6	ALE pulse width	30		ns
7	ALE setup time before command active	0		ns
7A	ALE to command inactive delay	30		ns
8	$\overline{RD}$, $\overline{WR}$ pulse width	80		ns
9	$\overline{RD}$, $\overline{WR}$ control interval	70		ns
10	Data valid after $\overline{RD}$ active		75	ns
11	Data hold after $\overline{RD}$ inactive	10	30	ns
15	Data stable before $\overline{WR}$ inactive	30		ns
16	Data hold after $\overline{WR}$ inactive	10		ns

11.4.4.2 Motorola Bus Interface Mode

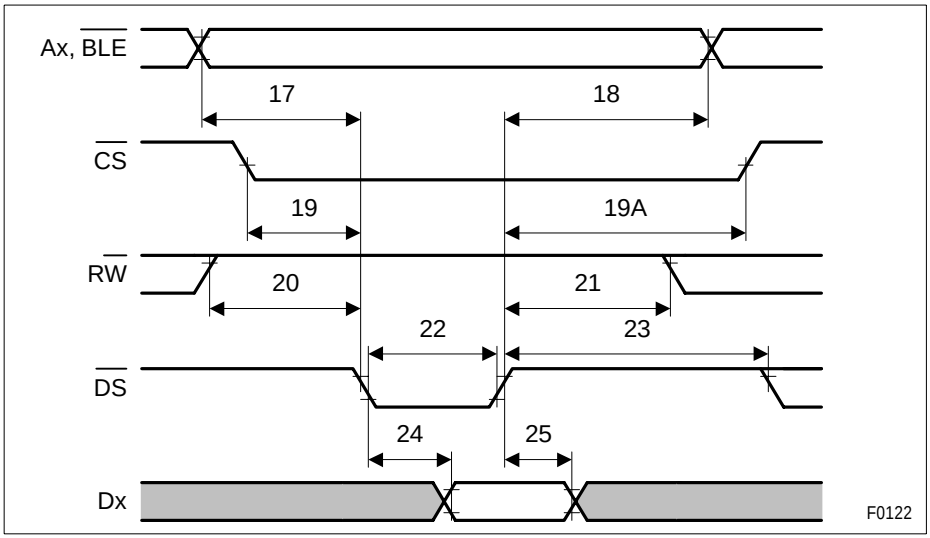


Figure 93 Motorola Read Cycle Timing

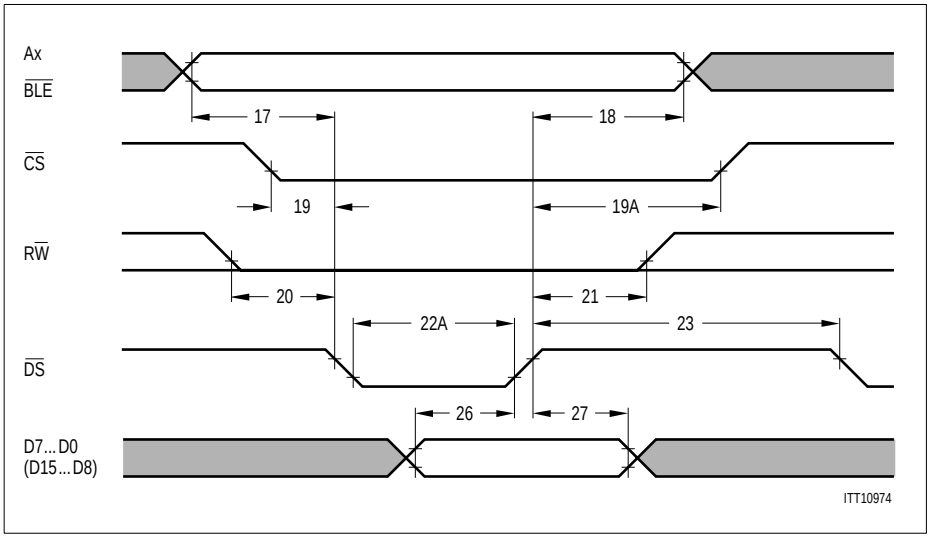


Figure 94 Motorola Write Cycle Timing

Table 75 Motorola Bus Interface Timing Parameter Values

No.	Parameter	Limit Values		Unit
		min.	max.	
17	Address, $\overline{BLE}$ setup time before $\overline{DS}$ active	15		ns
18	Address, $\overline{BLE}$ hold after $\overline{DS}$ inactive	0		ns
19	$\overline{CS}$ active before $\overline{DS}$ active	0		ns
19A	$\overline{CS}$ hold after $\overline{DS}$ inactive	0		ns
20	R$\overline{W}$ stable before $\overline{DS}$ active	10		ns
21	R$\overline{W}$ hold after $\overline{DS}$ inactive	0		ns
22	$\overline{DS}$ pulse width (read access)	80		ns
22A	$\overline{DS}$ pulse width (write access)	70		ns
23	$\overline{DS}$ control interval	70		ns
24	Data valid after $\overline{DS}$ active (read access)		75	ns
25	Data hold after $\overline{DS}$ inactive (read access)	10	30	ns
26	Data stable before $\overline{DS}$ active (write access)	30		ns
27	Data hold after $\overline{DS}$ inactive (write access)	10		ns

11.4.5 Line Interface

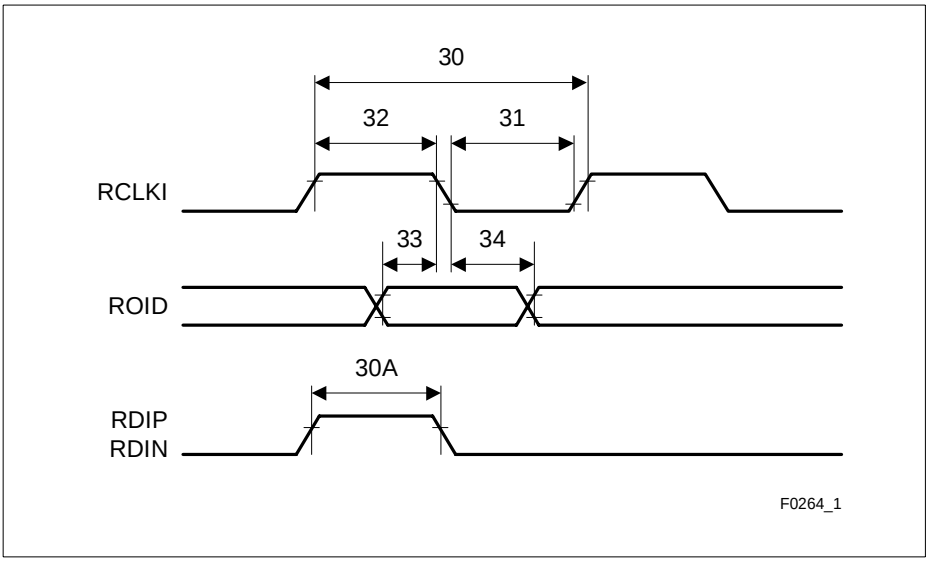


Figure 95 Digital Line Interface Receive Timing

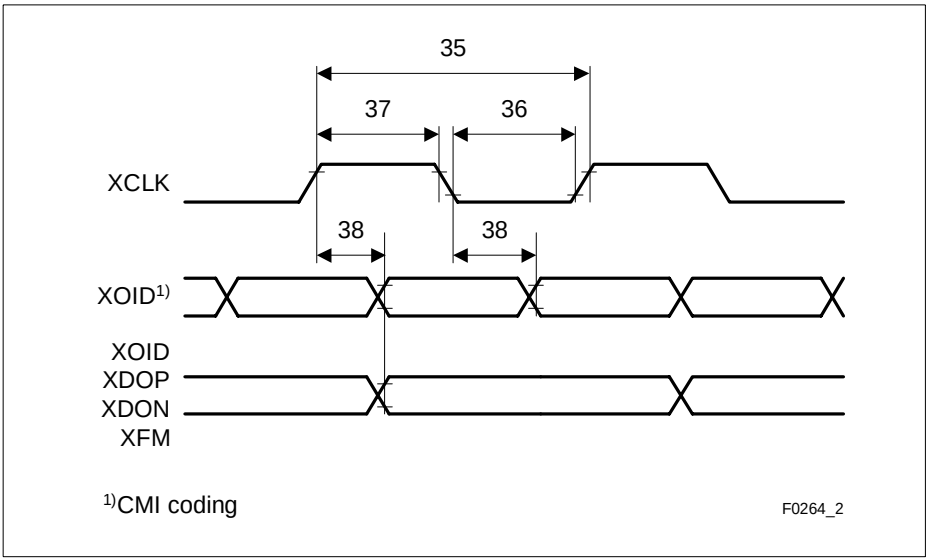


Figure 96 Digital Line Interface Transmit Timing

Table 76 Digital Line Interface Parameter Values

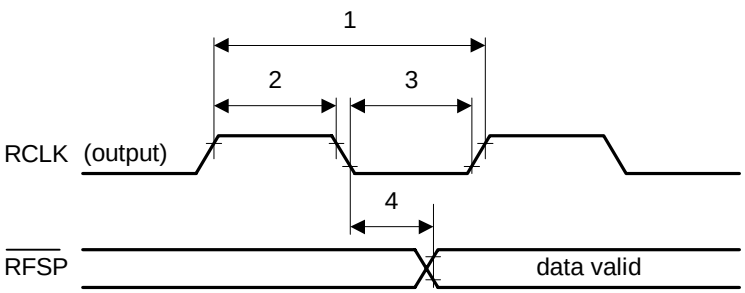
No.	Parameter	Limit Values						Unit
		E1			T1			
		min.	typ.	max.	min.	typ.	max.	
30	RCLKI clock period		488			648		ns
30A	RDIP/RDIN period high	122	244	366	162	324	486	ns
31	RCLKI clock period low	180			240			ns
32	RCLKI clock period high	180			240			ns
33	ROID setup	50			50			ns
34	ROID hold	50			50			ns
35	XCLK clock period		488			648		ns
36	XCLK clock period low XCLK clock period low[1)]	190 150			230 200			ns
37	XCLK clock period high XCLK clock period high[1)]	190 150			230 200			ns
38	XOID delay[2)] XDOP/XDON delay[3)]			60			60	ns

1) depends on input RCLKI in optical interface and remote loop without transmit jitter attenuator enabled (LIM1.JATT/RL=01)

2) NRZ coding

3) HDB3/AMI/B8ZS coding

11.4.6 System Interface



Note: active edge can be programmed to be positive or negative (only negative edge timing shown here); valid only, if RCLK is derived from DPLL (not, if RCLK jitter is attenuated)

F0009

Figure 97 RCLK, RFSP Output Timing

Table 77 RCLK, $\overline{\text{RFSP}}$ Timing Parameter Values

No.	Parameter	Limit Values			Unit
		min.	typ.	max.	
1	RCLK period E1 (2.048 MHz)		488		ns
	RCLK period E1 (2.048 MHz × 4)		122		ns
	RCLK period T1/J1 (1.544 MHz)		648		ns
	RCLK period T1/J1 (1.544 MHz × 4)		162		ns
2	RCLK pulse high	40		60	%
3	RCLK pulse low	40		60	%
4	$\overline{\text{RFSP}}$ delay			80	ns

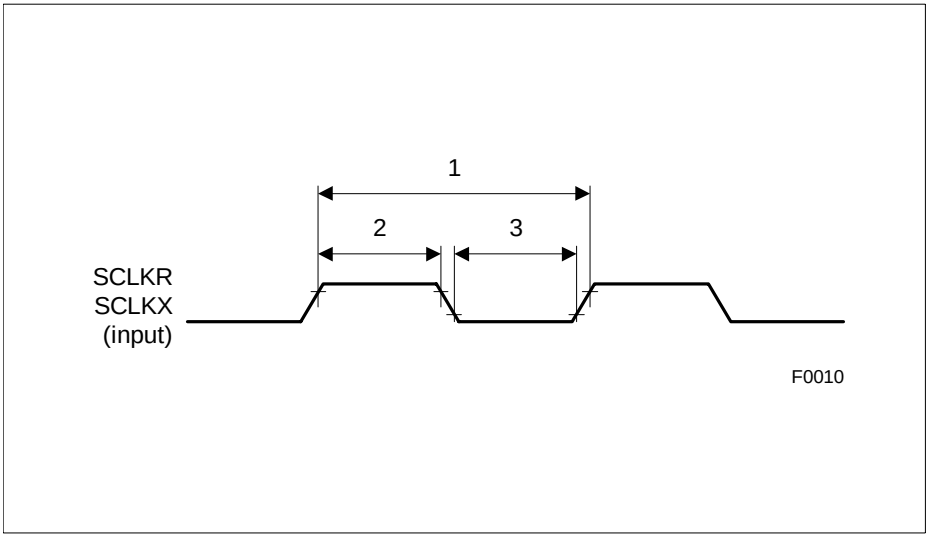


Figure 98 SCLKR/SCLKX Input Timing

Table 78 SCLKR/SCLKX Timing Parameter Values

No.	Parameter	Limit Values			Unit
		min.	typ.	max.	
1	SCLKR/SCLKX period at 16.384 MHz		61		ns
1	SCLKR/SCLKX period at 8.192 MHz		122		ns
1	SCLKR/SCLKX period at 4.096 MHz		244		ns
1	SCLKR/SCLKX period at 2.048 MHz		488		ns
1	SCLKR/SCLKX period at 12.352 MHz		81		ns
1	SCLKR/SCLKX period at 6.176 MHz		162		ns
1	SCLKR/SCLKX period at 3.088 MHz		324		ns
1	SCLKR/SCLKX period at 1.544 MHz		648		ns
2	SCLKR/SCLKX pulse high	40			%
3	SCLKR/SCLKX pulse low	40			%

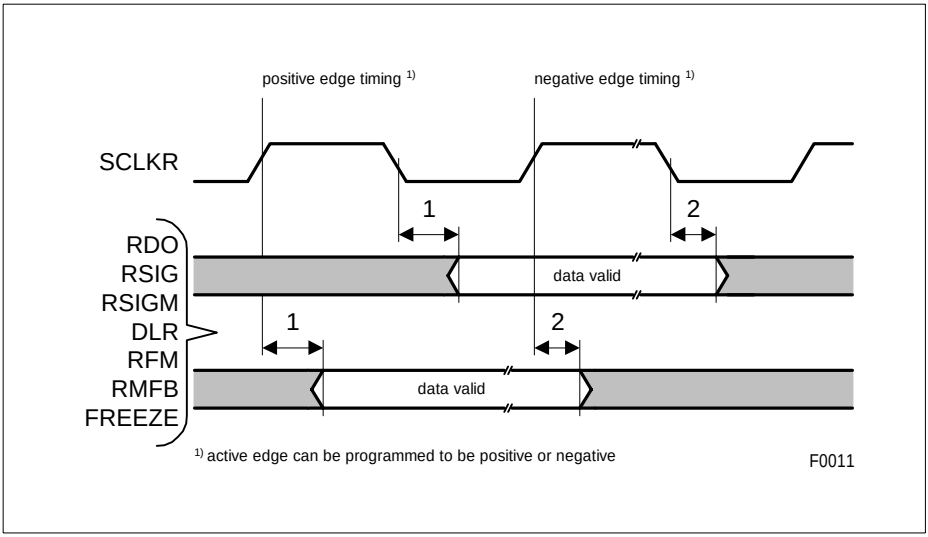


Figure 99 System Interface Marker Timing (Receive)

Table 79 System Interface Marker Timing Parameter Values

No.	Parameter	Limit Values			Unit
		min.	typ.	max.	
SCLKR input mode					
1	RDO delay	0		35	ns
2	RSIGM, RMFB, DLR, RFM, FREEZE, RSIG marker delay	0		45	ns
SCLKR output mode					
1A	RDO delay	-55		-20	ns
2A	RSIGM, RMFB, DLR, RFM, FREEZE, RSIG marker delay	-55		-20	ns

SCLKR can be input or output.

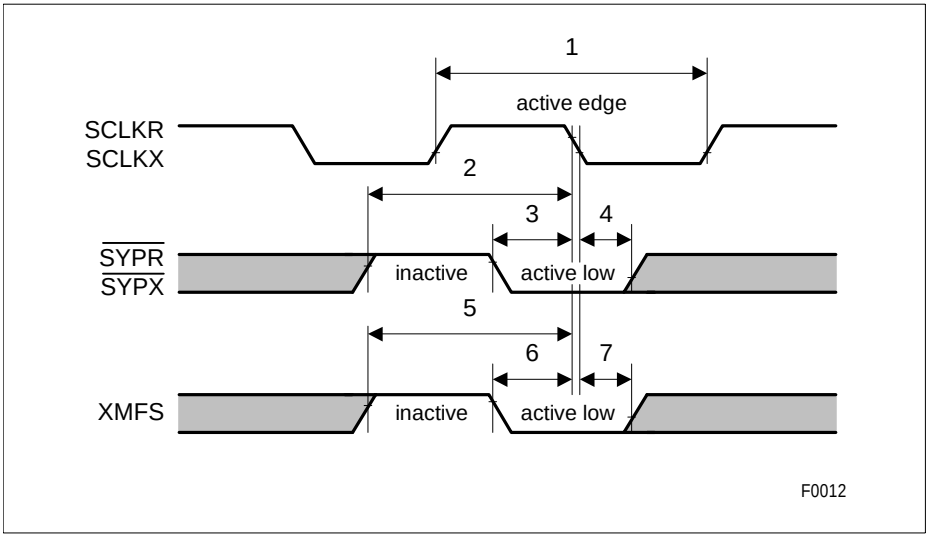


Figure 100 $\overline{\text{SYPR}}$, $\overline{\text{SYPX}}$ Timing

Table 80 $\overline{\text{SYPR}}$/$\overline{\text{SYPX}}$ Timing Parameter Values

No.	Parameter	Limit Values			Unit
		min.	typ.[1)]	max.	
SCLKR input mode					
1	SCLKR period (t_1)	61		648	ns
2	$\overline{\text{SYPR}}$/$\overline{\text{SYPX}}$ inactive setup time	1 x t_1			ns
3	$\overline{\text{SYPR}}$/$\overline{\text{SYPX}}$ setup time	5			ns
4	$\overline{\text{SYPR}}$/$\overline{\text{SYPX}}$ hold time	15			ns
5	XMFS inactive setup time	1 x t_1			ns
6	XMFS setup time	5			ns
7	XMFS hold time	15			ns
SCLKR output mode					
1A	SCLKR period (t_1)	61		648	ns
2A	$\overline{\text{SYPR}}$/$\overline{\text{SYPX}}$ inactive setup time	1 x t_1			ns
3A	$\overline{\text{SYPR}}$/$\overline{\text{SYPX}}$ setup time	10			ns

Table 80 $\overline{\text{SYPR}}$/$\overline{\text{SYPX}}$ Timing Parameter Values (cont'd)

No.	Parameter	Limit Values			Unit
		min.	typ.[1)]	max.	
4A	$\overline{\text{SYPR}}$/$\overline{\text{SYPX}}$ hold time	0			ns
5A	XMFS inactive setup time	1 x t_1			ns
6A	XMFS setup time	10			ns
7A	XMFS hold time	0			ns

1) typical value, not tested in production

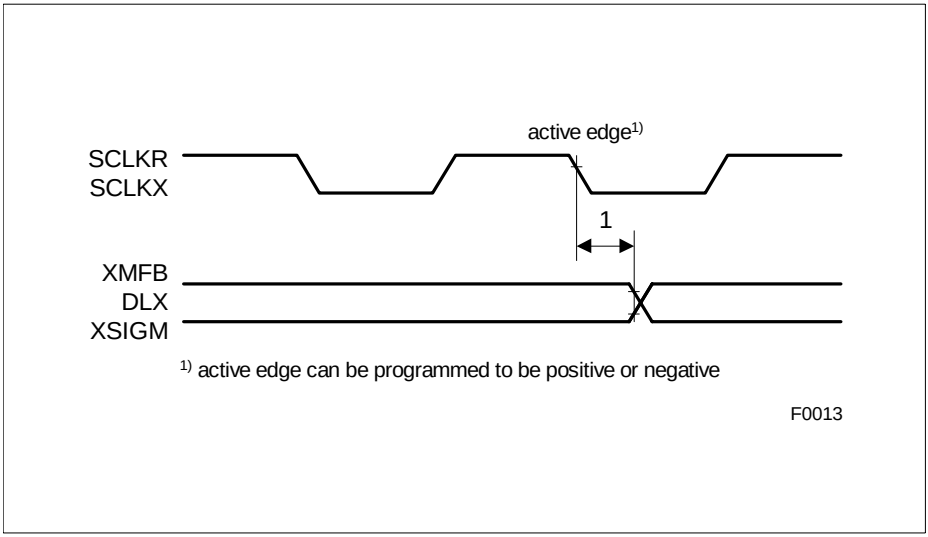


Figure 101 System Interface Marker Timing (Transmit)

Table 81 System Interface Marker Timing Parameter Values[1)]

No.	Parameter	Limit Values			Unit
		min.	typ.	max.	
SCLKR input mode					
1	XMFB, DLX, XSIGM delay			100	ns
SCLKR output mode					
1A	XMFB, DLX, XSIGM delay			-20	ns

1) Parameters based on SCLKR when CMR2.IXSC = 1 and on SCLKX when CMR2.IXSC = 0 (input mode only)

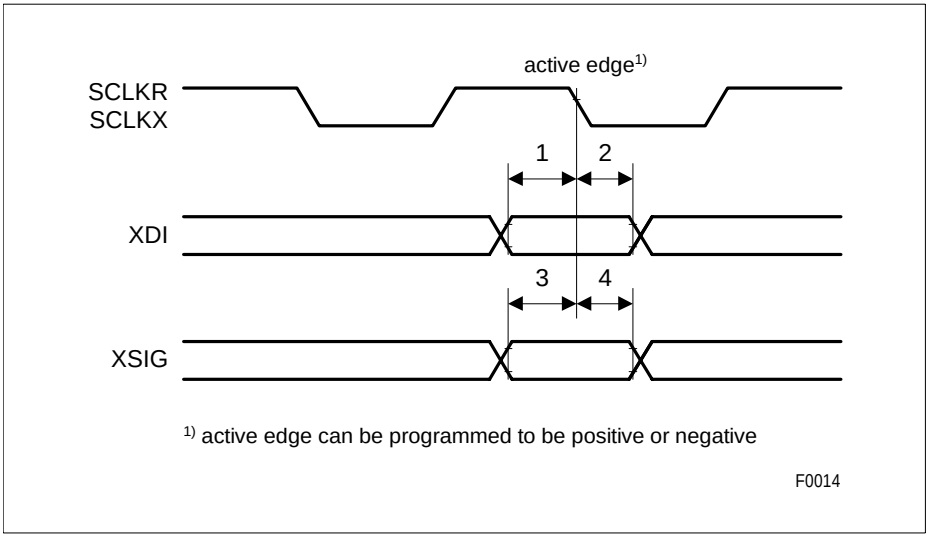


Figure 102 XDI, XSIG Timing

Table 82 XDI, XSIG Timing Parameter Values[1)]

No.	Parameter	Limit Values			Unit
		min.	typ.	max.	
SCLKR input mode					
1	XDI setup time	5			ns
2	XDI hold time	15			ns
3	XSIG setup time	5			ns
4	XSIG hold time	15			ns
SCLKR output mode					
1A	XDI setup time	10			ns
2A	XDI hold time	20			ns
3A	XSIG setup time	10			ns
4A	XSIG hold time	20			ns

1) Parameters based on SCLKR when CMR2.IXSC = 1 and on SCLKX when CMR2.IXSC = 0 (input mode only)

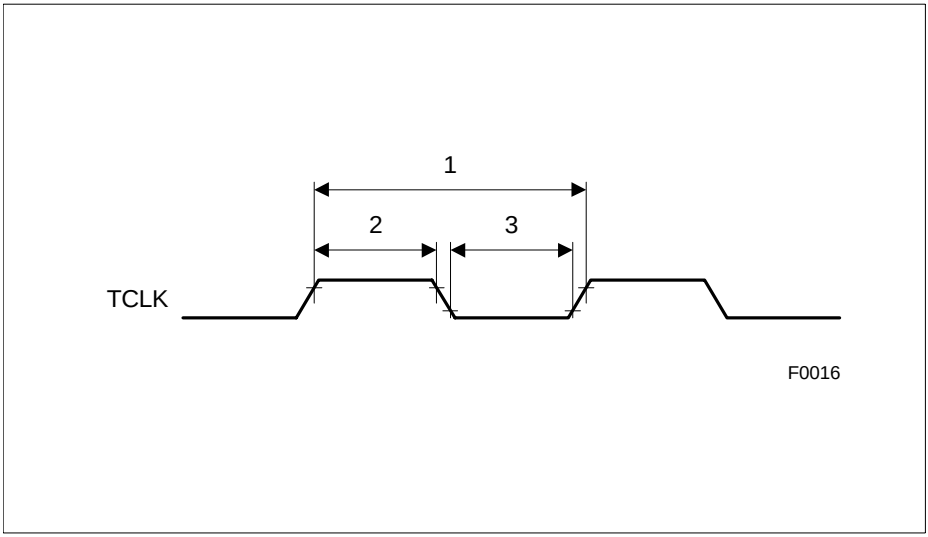


Figure 103 TCLK Input Timing

Table 83 TCLK Timing Parameter Values

No.	Parameter	Limit Values			Unit
		min.	typ.	max.	
1	TCLK period E1 (2.048 MHz)		488		ns
	TCLK period E1 (2.048 MHz × 4)		122		ns
	TCLK period T1/J1 (1.544 MHz)		648		ns
	TCLK period T1/J1 (1.544 MHz × 4)		162		ns
2	TCLK high	40			%
3	TCLK low	40			%

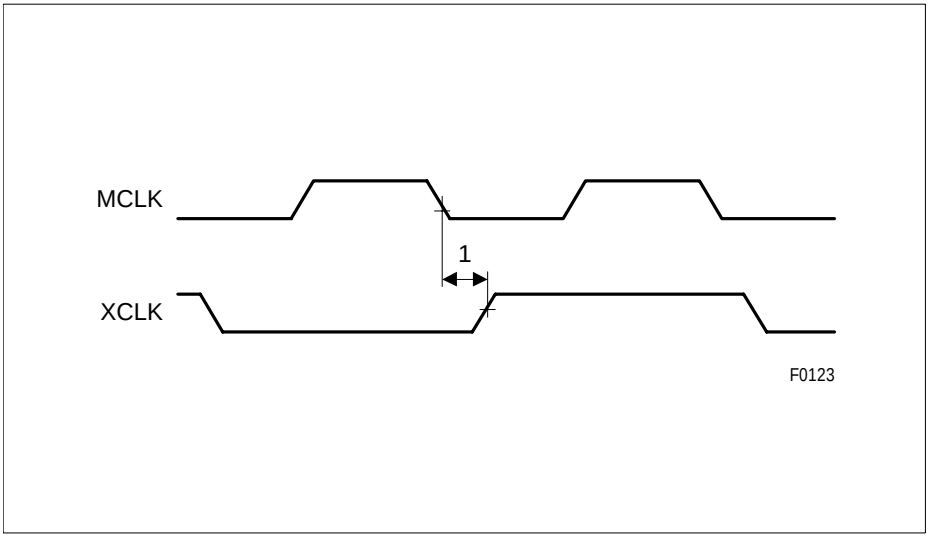


Figure 104 XCLK Timing

Table 84 XCLK Timing Parameter values

No.	Parameter	Limit Values						Unit
		E1			T1			
		min.	typ.	max.	min.	typ.	max.	
1	XCLK delay[1)]			100			100	ns

[1)] valid in transmit buffer bypass mode only

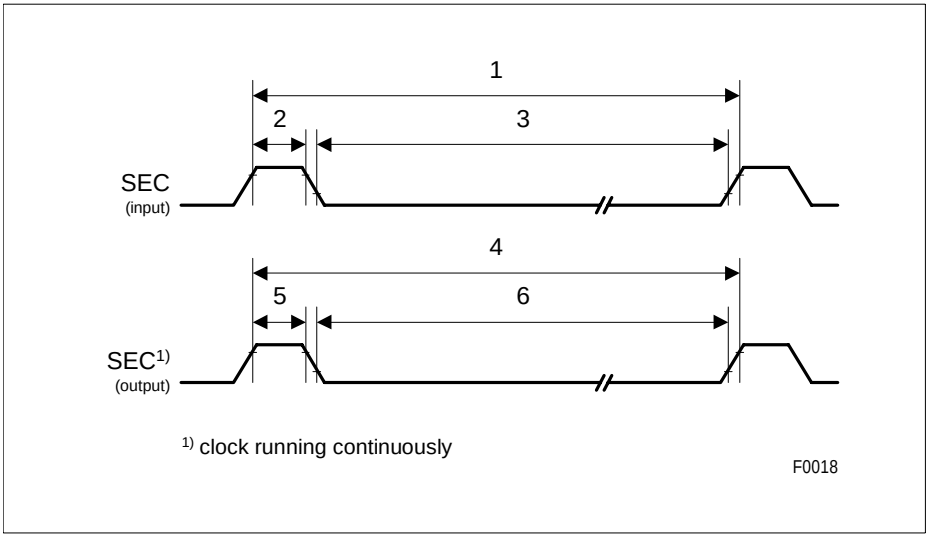


Figure 105 SEC Timing

Table 85 SEC Timing Parameter Values

No.	Parameter[1)]	Limit Values			Unit
		min.	typ.	max.	
1	SEC input period E1/T1/J1		1		s
2	SEC input high E1	976			ns
	SEC input high T1/J1	1296			ns
3	SEC input low E1	976			ns
	SEC input low T1/J1	1296			ns
4	SEC output period E1/T1/J1		1		s
5	SEC high output E1	976			ns
	SEC high output T1/J1	1296			ns

1) typical value, not tested in production

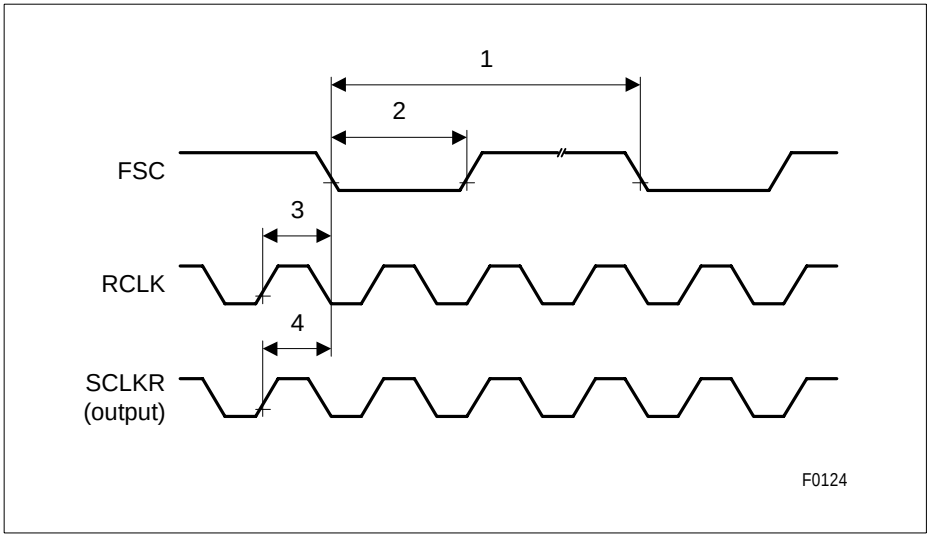


Figure 106 FSC Timing

Table 86 FSC Timing Parameter Values

No.	Parameter	Limit Values			Unit
		min.	typ.	max.	
1	FSC[1)] period		125		µs
2	FSC high/low active time E1		488		ns
2	FSC high/low active time T1/J1		648		ns
3	RCLK to FSC delay		50	80	ns
4	SCLKR to FSC delay		50	80	ns

1) FSC can be programmed to be active high or active low (only the active low timing diagram is shown here)

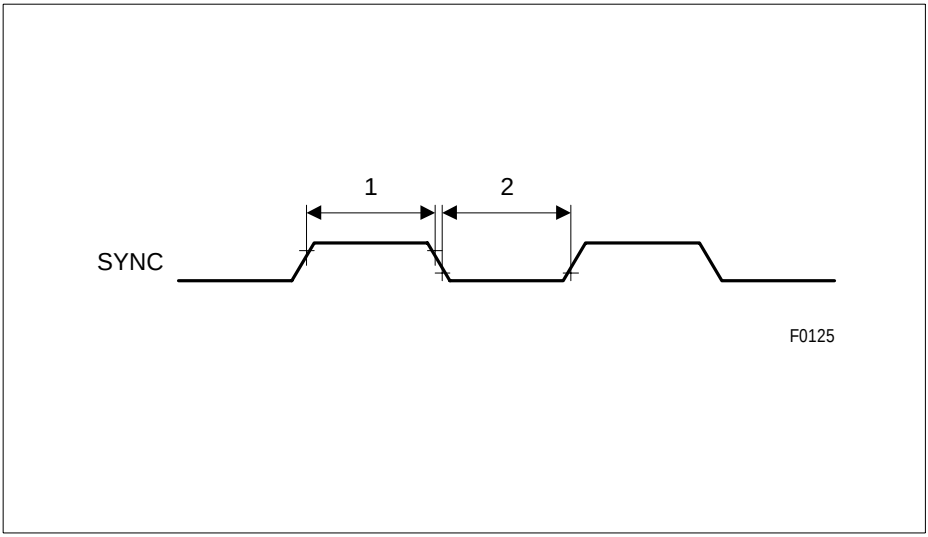


Figure 107 SYNC Timing

Table 87 SYNC Timing Parameter Values

No.	Parameter	Limit Values			Unit
		min.	typ.	max.	
1	SYNC high time	30			%
2	SYNC low time	30			%

11.4.7 Pulse Templates - Transmitter

11.4.7.1 Pulse Template E1

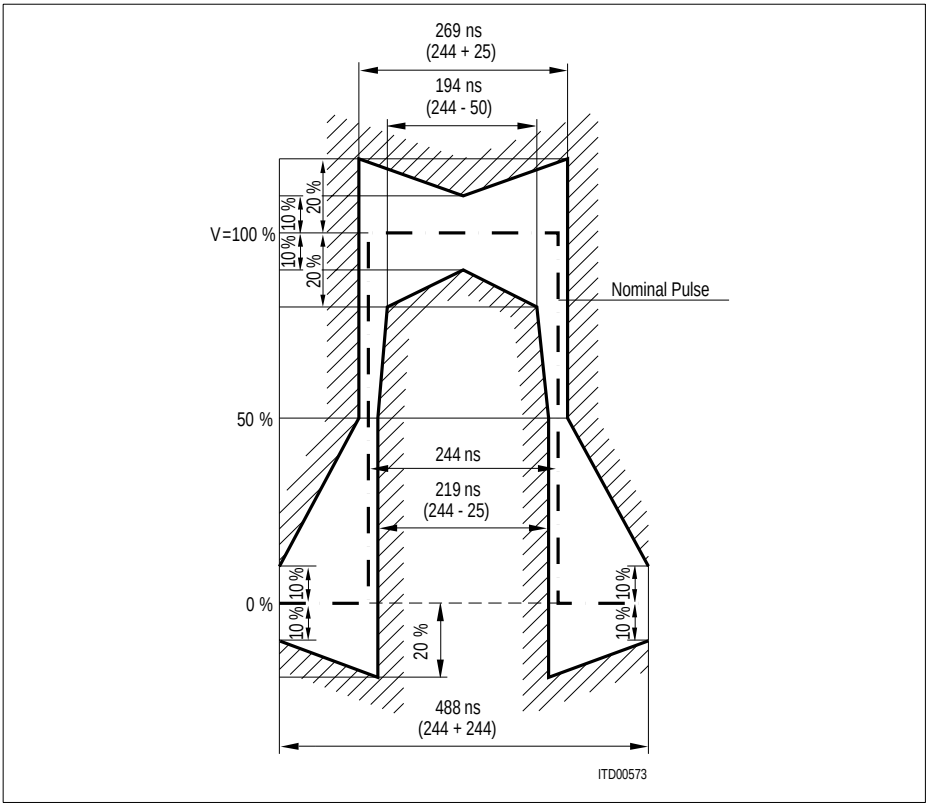


Figure 108 E1 Pulse Shape at Transmitter Output

11.4.7.2 Pulse Template T1

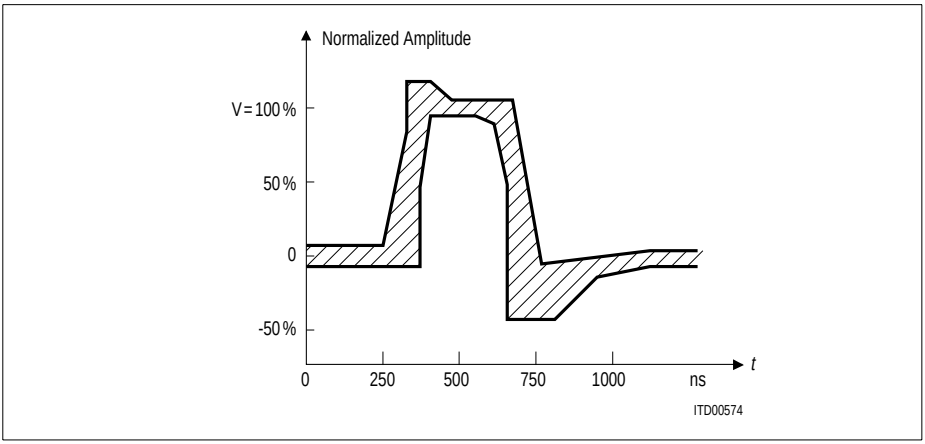


Figure 109 T1 Pulse Shape at the Cross Connect Point

Table 88 T1 Pulse Template at Cross Connect Point (T1.102[1])

Maximum Curve		Minimum Curve	
Time [ns]	**Level [%][2]**	**Time [ns]**	**Level [%]**
0	5	0	-5
250	5	350	-5
325	80	350	50
325	115	400	95
425	115	500	95
500	105	600	90
675	105	650	50
725	-7	650	-45
1100	5	800	-45
1250	5	925	-20
		1100	-5
		1250	-5

1) requirements of ITU-T G.703 are also fulfilled

2) 100 % value must be in the range of 2.4 V and 3.6 V;
tested at 0 ft. and 655 ft. using PIC 22AWG cable characteristics.

11.5 Capacitances

Parameter	Symbol	Limit Values		Unit	Notes
		min.	max.		
Input capacitance[1)]	C_{IN}	5	10	pF	
Output capacitance[1)]	C_{OUT}	8	15	pF	all except XLx
Output capacitance[1)]	C_{OUT}	8	20	pF	XLx

1) not tested in production

11.6 Package Characteristics

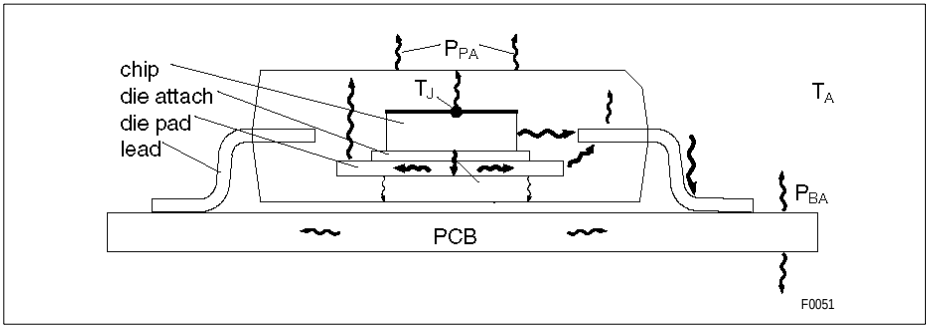


Figure 110 Thermal Behavior of Package

Table 89 Package Characteristic Values

Parameter	Symbol	Limit Values			Unit	Notes
		min.	typ.	max.		
Thermal Resistance P-TQFP-144	R_{thja1} 1)		30		K/W	single layer PCB, no convection
	R_{thja2}		15		K/W	multilayer PCB, free convection
	R_{thjc} 2)		3		K/W	
Thermal Resistance P-BGA-160	R_{thja1} 1)		31		K/W	4-layer PCB, no convection
Junction Temperature	R_j			125	°C	

1) $R_{thja} = (T_{junction} - T_{ambient})/Power$; this value is not tested in production.

2) $R_{thjc} = (T_{junction} - T_{case})/Power$; this value is not tested in production.

11.7 Test Configuration

11.7.1 AC Tests

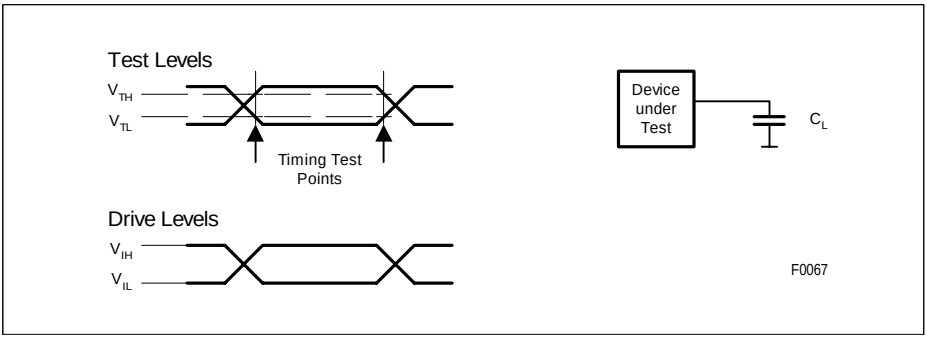


Figure 111 Input/Output Waveforms for AC Testing

Table 90 AC Test Conditions

Parameter	Symbol	Test Values	Unit	Notes
Load Capacitance	C_L	50	pF	
Input Voltage high	V_{IH}	2.4	V	all except RLx
Input Voltage low	V_{IL}	0.4	V	all except RLx
Test Voltage high	V_{TH}	2.0	V	all except XLx
Test Voltage low	V_{TL}	0.8	V	all except XLx

11.7.2 Power Supply Test

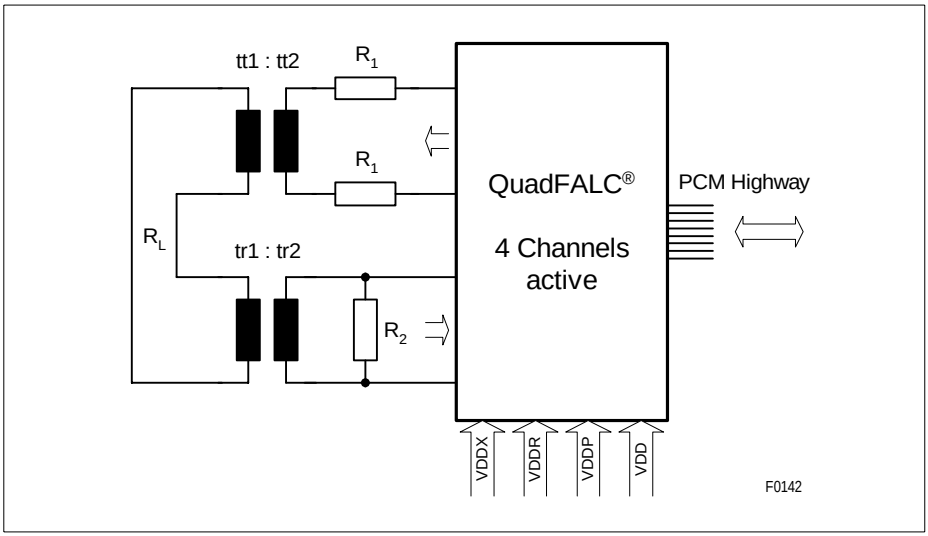


Figure 112 Device Configuration for Power Supply Testing

Table 91 Power Supply Test Conditions E1

Parameter	Symbol	Test Values	Unit	Notes
Load Resistance	R1	7.5	Ω	1%
Termination Resistance	R2	120	Ω	1%
Line Impedance	RL	120	Ω	
Line Length	L	< 0.2	m	
Transformer Ratio Transmit	tt1 : tt2	2.4		
Transformer Ratio Receive	tr1 : tr2	1		
PCM Highway Frequency	SCLKX SCLKR	2.048	MHz	
Test Signal		2^{15}-1		PRBS pattern
Active Channels (DCOs active, 2-frame buffer)		4		

Table 91 Power Supply Test Conditions E1 (cont'd)

Parameter	Symbol	Test Values	Unit	Notes
Pulse Mask Programming	XPM2	00_H		
	XPM1	03_H		
	XPM0	$9C_H$		
Ambient Temperature		85	°C	

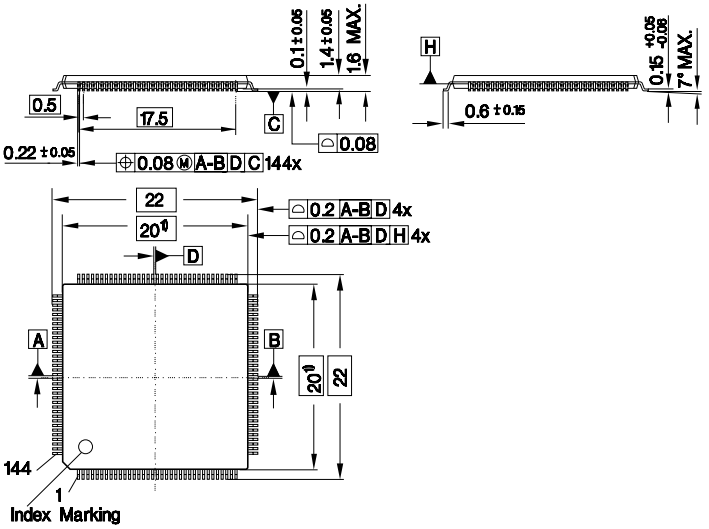
Table 92 Power Supply Test Conditions T1/J1

Parameter	Symbol	Test Values	Unit	Notes
Load Resistance	R1	2	Ω	1%
Termination Resistance	R2	100	Ω	1%
Line Impedance	RL	100	Ω	
Line Length	L	< 0.2	m	
Transformer Ratio Transmit	tt1 : tt2	2.4		
Transformer Ratio Receive	tr1 : tr2	1		
PCM Highway Frequency	SCLKX SCLKR	1.544	MHz	
Test Signal		2^{15}-1		PRBS pattern
Active Channels (DCOs active, 2-frame buffer)		4		
Pulse Mask Programming	XPM2	01_H		
	XPM1	16_H		
	XPM0	95_H		
Ambient Temperature		85	°C	

12 Package Outlines

12.1 Thin Flat Pack Package

P-TQFP-144
(Plastic Metric Quad Flat Package)



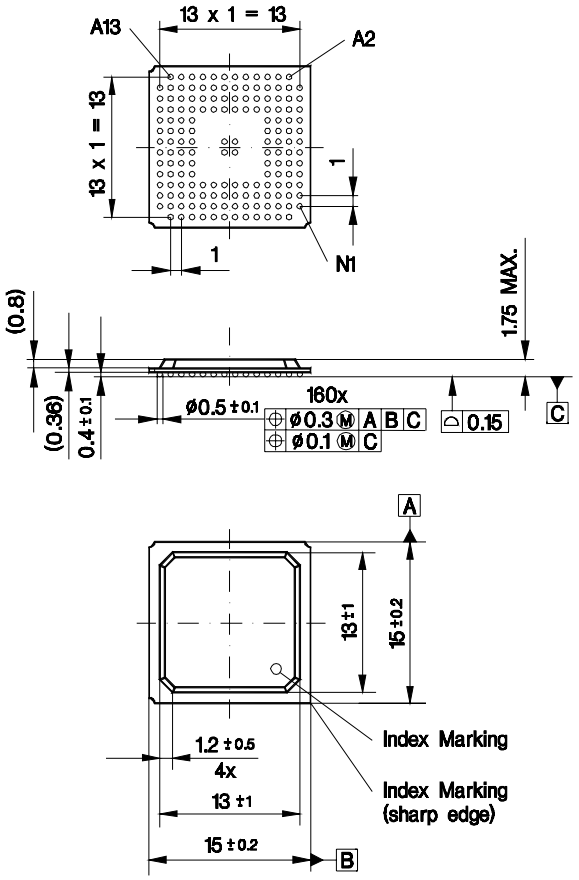
You can find all of our packages, sorts of packing and others in our Infineon Internet Page “Products”: http://www.infineon.com/products.

SMD = Surface Mounted Device

Dimensions in mm

12.2 Ball Grid Array Package

P-BGA-160
(Plastic Ball Grid Array Package)



You can find all of our packages, sorts of packing and others in our Infineon Internet Page “Products”: http://www.infineon.com/products.

SMD = Surface Mounted Device

Dimensions in mm

13 Appendix

13.1 Protection Circuitry

The design in **Figure 113** shows an example of how to build up a generic E1/T1/J1 platform. The circuit shown has been successfully checked against ITU-T K.20 and K.21 lightning surge tests (basic level).

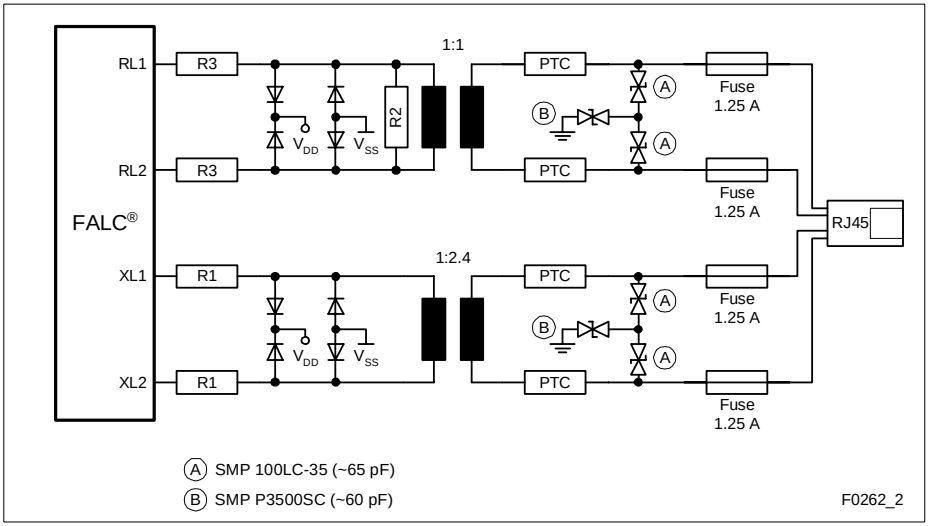


Figure 113 Protection Circuitry Examples

13.2 Application Notes

Several application notes and technical documentation provide additional information. Online access to supporting information is available on the internet page:

http://www.infineon.com/falc

On the same page you find as well the

- Boundary Scan File for QuadFALC Version 2.1 (BSDL File)
- IBIS File for QuadFALC Version 2.1

13.3 Software Support

The following software package is provided together with the QuadFALC Reference System EASY22554:

- E1 and T1 driver functions supporting different ETSI, AT&T and Telcordia (former: Bellcore) requirements
- IBIS model for QuadFALC Version 2.1 (according to ANSI/EIA-656)
- Flexible Master Clock Calculator
- External Line Front End Calculator
- Application Wizard

To make system design easier, three software tools are available. The first is the ’Master Clock Frequency Calculator’, which calculates the required register settings depending on the external master clock frequency (MCLK). The second is the ’External Line Front End Calculator’ which provides an easy method to optimize the external components depending on the selected application type. Calculation results are traced an can be stored in a file or printed out for documentation. The third tool is the ’Application Wizard’ which helps to set up the detailed device configuration.

The tools run under a Win9x/NT environment.

Screenshots of the programs are shown in **Figure 114** to **Figure 116** below.

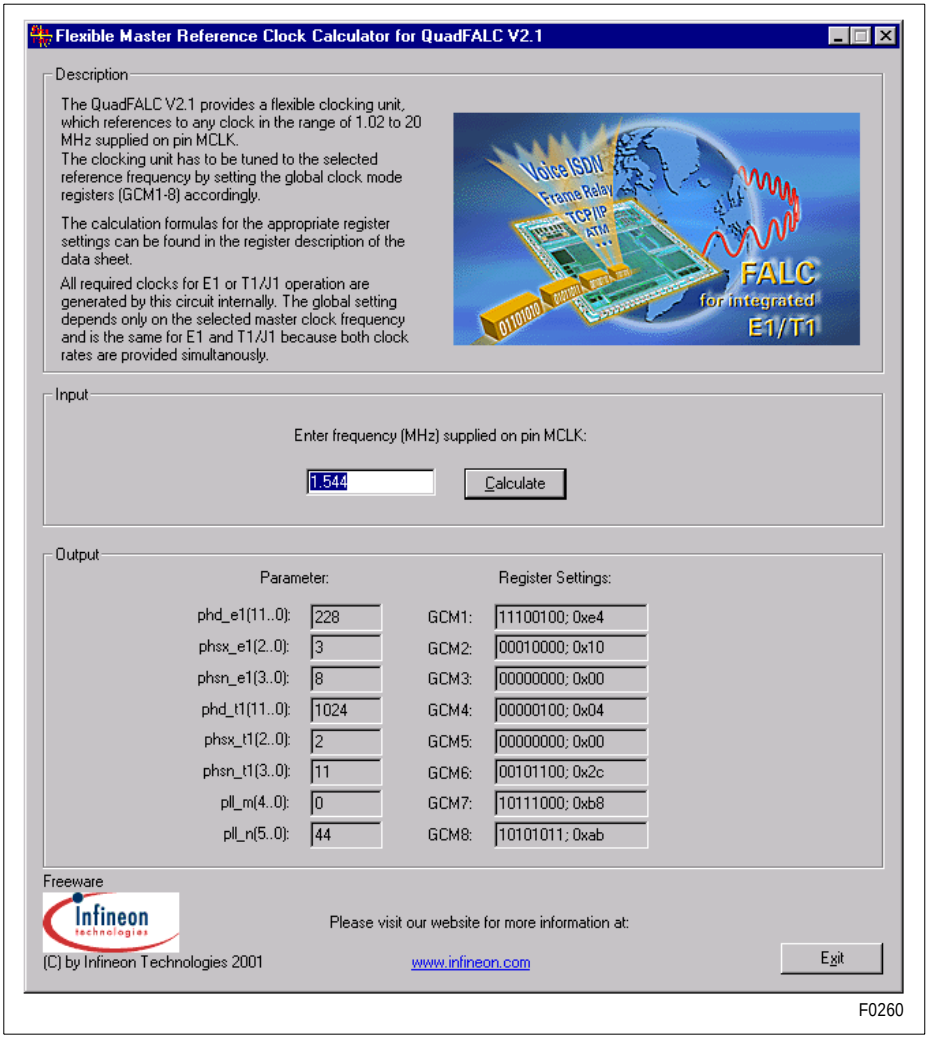


Figure 114 Master Clock Frequency Calculator

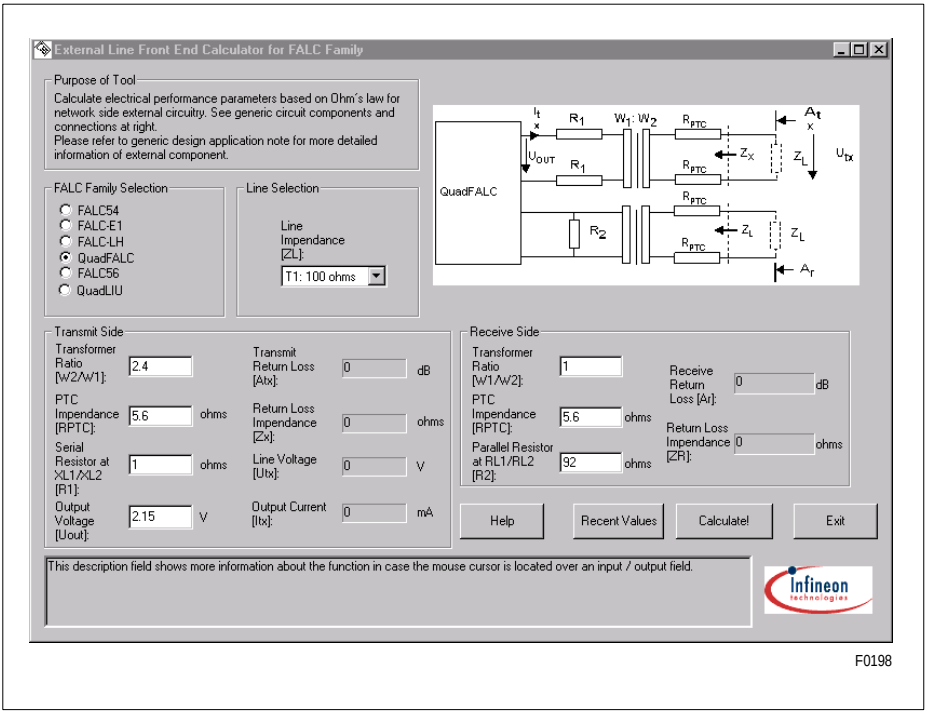


Figure 115 External Line Frontend Calculator

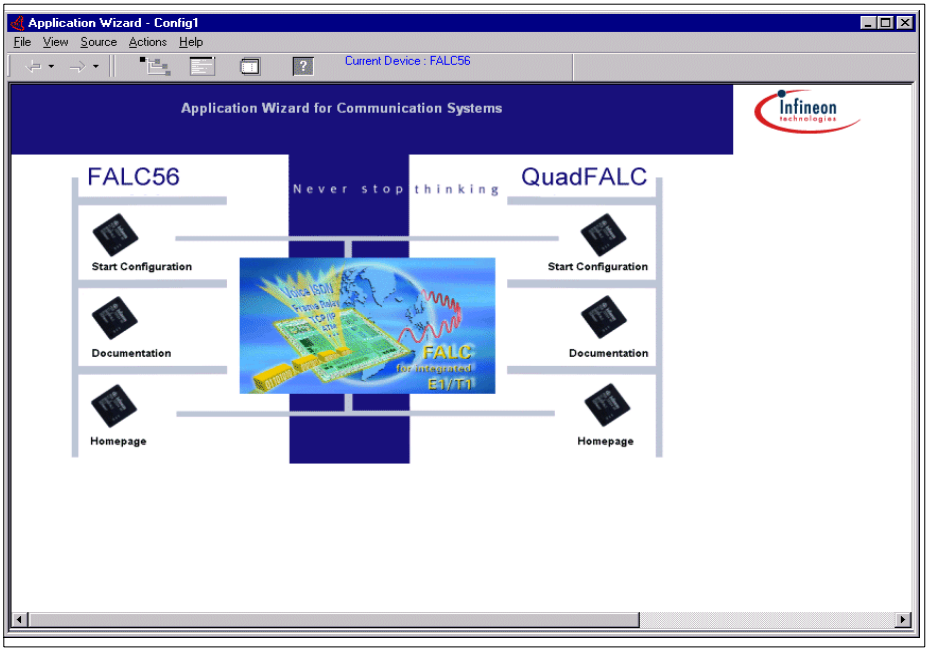


Figure 116 Application Wizard

14 Terminology

A/D	Analog to digital
ADC	Analog to digital converter
AIS	Alarm indication signal (blue alarm)
AGC	Automatic gain control
ALOS	Analog loss of signal
AMI	Alternate mark inversion
ANSI	American National Standards Institute
ATM	Asynchronous transfer mode
AUXP	Auxiliary pattern
B8ZS	Line coding to avoid too long strings of consecutive ’0’
BER	Bit error rate
BFA	Basic frame alignment
BOM	Bit orientated message
Bellcore	Bell Communications Research
BPV	Bipolar violation
BSN	Backward sequence number
CAS	Channel associated signaling
CAS-BR	Channel associated signaling - bit robbing
CAS-CC	Channel associated signaling - common channel
CCS	Common channel signaling
CMI	coded mark inversion code (also known as 1T2B code, e.g., defined in ITU-T G.703 and Telcordia GR-499-CORE)
CR	Command/Response (special bit in PPR)
CRC	Cyclic redundancy check
CSU	Channel service unit
CVC	Code violation counter
DCO	Digitally controlled oscillator
DL	Digital loop
DPLL	Digitally controlled phase locked loop
DS1	Digital signal level 1
EA	Extended address (special bit in PPR)

ESD	Electrostatic discharge
EASY	Evaluation system for FALC products
ESF	Extended superframe (F24) format
EQ	Equalizer
ETSI	European Telecommunication Standards Institute
FALC®	Framing and line interface component
FAS	Frame alignment sequence
FCC	US Federal Communication Commission
FCS	Frame check sequence (used in PPR)
FISU	Fill in signaling unit
FPS	Framing pattern sequence
FSN	Forward sequence number
HBM	Human body model for ESD classification
HDB3	High density bipolar of order 3
HDLC	High level data link control
IBIS	I/O buffer information specification (ANSI/EIA-656)
IBL	In band loop (=LLB)
ISDN	Integrated services digital network
ITU	International Telecommunications Group
JATT	Jitter attenuator
JTAG	Joined Test Action Group
LAPD	Link access procedure on D-channel
LBO	Line build out
LCV	Line code violation
LIU	Line interface unit
LFA	Loss of frame alignment
LL	Local loop
LLB	Line loop back (= IBL)
LOS	Loss of signal (red alarm)
LSB	Least significant bit
LSSU	Link status signaling unit
MF	Multiframe

MSB	Most significant bit
MSU	Message signaling unit
NRZ	Non return to zero signal
PDV	Pulse density violation
PLB	Payload loop back
PLL	Phase locked loop
PMQFP	Plastic metric quad flat pack (device package)
PPR	Periodical performance report
PRBS	Pseudo random binary sequence
PTQFP	Plastic thin metric quad flat pack (device package)
RAI	Remote alarm indication (yellow alarm)
RL	Remote loop
SAPI	Service access point identifier (special octet in PPR)
SF	Superframe
Sidactor	Overvoltage protection device for transmission lines
TAP	Test access port
TEI	Terminal endpoint identifier (special octet in PPR)
UI	Unit interval
ZCS	Zero code suppression

Index

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