



Integrated Device Technology, Inc.

FAST CMOS OCTAL BIDIRECTIONAL TRANSCEIVERS

IDT54/74FCT245/A/C
IDT54/74FCT640/A/C
IDT54/74FCT645/A/C

FEATURES:

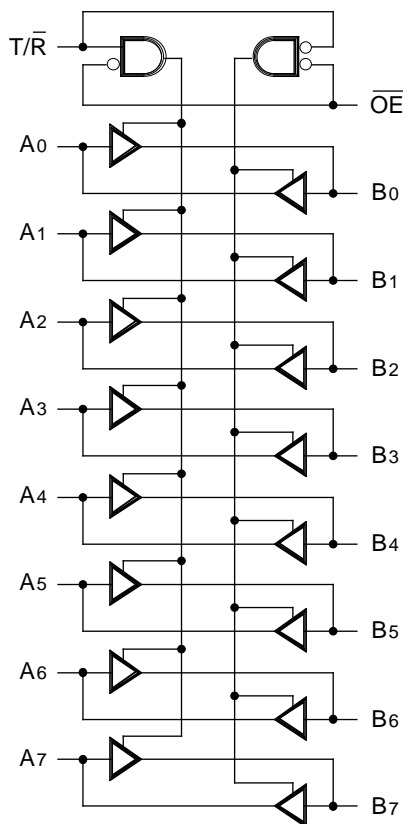
- IDT54/74FCT245/640/645 equivalent to FAST™ speed and drive
- **IDT54/74FCT245A/640A/645A 25% faster than FAST**
- **IDT54/74FCT245C/640C/645C 40% faster than FAST**
- TTL input and output level compatible
- CMOS output level compatible
- IOL = 64mA (commercial) and 48mA (military)
- Input current levels only 5µA max.
- CMOS power levels (2.5mW typical static)
- Direction control and over-riding 3-state control
- Product available in Radiation Tolerant and Radiation Enhanced versions
- Military product compliant to MIL-STD-883, Class B and DESC listed
- Meets or exceeds JEDEC Standard 18 specifications

DESCRIPTION:

The IDT octal bidirectional transceivers are built using an advanced dual metal CMOS technology. The IDT54/74FCT245/A/C, IDT54/74FCT640/A/C and IDT54/74FCT645/A/C are designed for asynchronous two-way communication between data buses. The transmit/receive (T/\bar{R}) input determines the direction of data flow through the bidirectional transceiver. Transmit (active HIGH) enables data from A ports to B ports, and receive (active LOW) from B ports to A ports. The output enable (\overline{OE}) input, when HIGH, disables both A and B ports by placing them in High-Z condition.

The IDT54/74FCT245/A/C and IDT54/74FCT645/A/C transceivers have non-inverting outputs. The IDT54/74FCT640/A/C has inverting outputs.

FUNCTIONAL BLOCK DIAGRAM

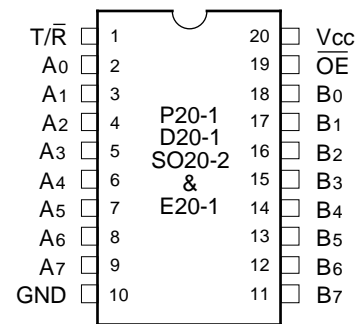


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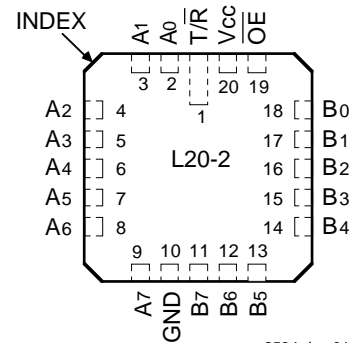
NOTES:

1. FCT245, 645 are noninverting options.
2. FCT640 is the inverting option.

PIN CONFIGURATIONS



DIP/SOIC/CERPACK
TOP VIEW



LCC
TOP VIEW

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MILITARY AND COMMERCIAL TEMPERATURE RANGES

MAY 1992

PIN DESCRIPTION

Pin Names	Description
\overline{OE}	Output Enable Input (Active LOW)
T/\overline{R}	Transmit/Receive Input
A ₀ –A ₇	Side A Inputs or 3-State Outputs
B ₀ –B ₇	Side B Inputs or 3-State Outputs

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FUNCTION TABLE⁽²⁾

Inputs		Outputs
\overline{OE}	T/\overline{R}	
L	L	Bus B Data to Bus A ⁽¹⁾
L	H	Bus A Data to Bus B ⁽¹⁾
H	X	High Z State

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NOTES:

- 640 is inverting from input to output.
- H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Symbol	Rating	Commercial	Military	Unit
V _{TERM} ⁽²⁾	Terminal Voltage with Respect to GND	–0.5 to +7.0	–0.5 to +7.0	V
V _{TERM} ⁽³⁾	Terminal Voltage with Respect to GND	–0.5 to V _{CC}	–0.5 to V _{CC}	V
T _A	Operating Temperature	0 to +70	–55 to +125	°C
T _{BIAS}	Temperature Under Bias	–55 to +125	–65 to +135	°C
T _{STG}	Storage Temperature	–55 to +125	–65 to +150	°C
P _T	Power Dissipation	0.5	0.5	W
I _{OUT}	DC Output Current	120	120	mA

NOTES:

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- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability. No terminal voltage may exceed V_{CC} by +0.5V unless otherwise noted.
- Inputs and V_{CC} terminals.
- Outputs and I/O terminals.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter ⁽¹⁾	Conditions	Typ.	Max.	Unit
C _{IN}	Input Capacitance	V _{IN} = 0V	6	10	pF
C _{I/O}	I/O Capacitance	V _{OUT} = 0V	8	12	pF

NOTE:

2534 tbl 02

- This parameter is measured at characterization but not tested.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified: $V_{LC} = 0.2V$; $V_{HC} = V_{CC} - 0.2V$

Commercial: $T_A = 0^{\circ}C$ to $+70^{\circ}C$, $V_{CC} = 5.0V \pm 5\%$; Military: $T_A = -55^{\circ}C$ to $+125^{\circ}C$, $V_{CC} = 5.0V \pm 10\%$

Symbol	Parameter	Test Conditions ⁽¹⁾	Min.	Typ. ⁽²⁾	Max.	Unit	
V_{IH}	Input HIGH Level	Guaranteed Logic HIGH Level	2.0	—	—	V	
V_{IL}	Input LOW Level	Guaranteed Logic LOW Level	—	—	0.8	V	
I_{IH}	Input HIGH Current (Except I/O pins)	$V_{CC} = \text{Max}$ $V_I = V_{CC}$	—	—	5	μA	
			—	—	$5^{(4)}$		
I_{IL}	Input LOW Current (Except I/O pins)	$V_{CC} = \text{Max}$ $V_I = 0.5V$	—	—	$-5^{(4)}$	μA	
			—	—	-5		
I_{IH}	Input HIGH Current (I/O pins only)	$V_{CC} = \text{Max}$ $V_I = V_{CC}$	—	—	15	μA	
			—	—	$15^{(4)}$		
I_{IL}	Input LOW Current (I/O pins only)	$V_{CC} = \text{Max}$ $V_I = 0.5V$	—	—	$-15^{(4)}$	μA	
			—	—	-15		
V_{IK}	Clamp Diode Voltage	$V_{CC} = \text{Min.}$, $I_N = -18mA$	—	-0.7	-1.2	V	
I_{OS}	Short Circuit Current	$V_{CC} = \text{Max.}^{(3)}$, $V_O = \text{GND}$	-60	-120	—	mA	
V_{OH}	Output HIGH Voltage	$V_{CC} = 3V$, $V_{IN} = V_{LC}$ or V_{HC} , $I_{OH} = -32\mu A$	V_{HC}	V_{CC}	—	V	
		$V_{CC} = \text{Min.}$ $V_{IN} = V_{IH}$ or V_{IL}	$I_{OH} = -300\mu A$	V_{HC}	V_{CC}		—
			$I_{OH} = -12mA \text{ MIL.}$	2.4	4.3		—
			$I_{OH} = -15mA \text{ COM'L.}$	2.4	4.3	—	
V_{OL}	Output LOW Voltage (Port A and Port B)	$V_{CC} = 3V$, $V_{IN} = V_{LC}$ or V_{HC} , $I_{OL} = 300\mu A$	—	GND	V_{LC}	V	
		$V_{CC} = \text{Min.}$ $V_{IN} = V_{IH}$ or V_{IL}	$I_{OL} = 300\mu A$	GND	$V_{LC}^{(4)}$		
			$I_{OL} = 48mA \text{ MIL.}$	—	0.3		0.55
			$I_{OL} = 64mA \text{ COM'L.}$	—	0.3	0.55	

NOTES:

- For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
- Typical values are at $V_{CC} = 5.0V$, $+25^{\circ}C$ ambient and maximum loading.
- Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.
- This parameter is guaranteed but not tested.

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POWER SUPPLY CHARACTERISTICS

$V_{LC} = 0.2V$; $V_{HC} = V_{CC} - 0.2V$

Symbol	Parameter	Test Conditions ⁽¹⁾		Min.	Typ. ⁽²⁾	Max.	Unit
I _{CC}	Quiescent Power Supply Current	V _{CC} = Max. V _{IN} ≥ V _{HC} ; V _{IN} ≤ V _{LC}		—	0.5	1.5	mA
ΔI _{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V _{CC} = Max. V _{IN} = 3.4V ⁽³⁾		—	0.5	2.0	mA
I _{CCD}	Dynamic Power Supply Current ⁽⁴⁾	V _{CC} = Max. Outputs Open $\overline{OE} = GND$ T/ $\overline{R} = GND$ or V _{CC} One Input Toggling 50% Duty Cycle	V _{IN} ≥ V _{HC} V _{IN} ≤ V _{LC}	—	0.15	0.25	mA/MHz
I _C	Total Power Supply Current ⁽⁶⁾	V _{CC} = Max. Outputs Open f _i = 10MHz 50% Duty Cycle T/ $\overline{R} = \overline{OE} = GND$ One Bit Toggling	V _{IN} ≥ V _{HC} V _{IN} ≤ V _{LC} (FCT)	—	2.0	4.0	mA
		V _{CC} = Max. Outputs Open f _i = 2.5MHz 50% Duty Cycle T/ $\overline{R} = \overline{OE} = GND$ Eight Bits Toggling	V _{IN} = 3.4V V _{IN} = GND	—	2.3	5.0	
			V _{IN} ≥ V _{HC} V _{IN} ≤ V _{LC} (FCT)	—	3.5	6.5 ⁽⁵⁾	
			V _{IN} = 3.4V V _{IN} = GND	—	5.5	14.5 ⁽⁵⁾	

NOTES:

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- For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
- Typical values are at V_{CC} = 5.0V, +25°C ambient.
- Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
- This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
- Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
- I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}
 $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_i)$
 I_{CC} = Quiescent Current
 ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
 D_H = Duty Cycle for TTL Inputs High
 N_T = Number of TTL Inputs at D_H
 I_{CCD} = Dynamic Current Caused by an Output Transition Pair (HLH or LHL)
 f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
 f_i = Input Frequency
 N_i = Number of Inputs at f_i
 All currents are in milliamps and all frequencies are in megahertz.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE FOR FCT245/A/C

Symbol	Parameter	Condition ⁽¹⁾	54/74FCT245		54/74FCT245A		54/74FCT245C		Unit						
			Com'l.		Mil.		Com'l.			Mil.					
			Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.		Min. ⁽²⁾	Max.				
tPLH tPHL	Propagation Delay A to B, B to A	CL = 50 pF RL = 500Ω	1.5	7.0	1.5	7.5	1.5	4.6	1.5	4.9	1.5	4.1	1.5	4.5	ns
tpZH tpZL	Output Enable Time OE to A or B		1.5	9.5	1.5	10.0	1.5	6.2	1.5	6.5	1.5	5.8	1.5	6.2	ns
tPHZ tPLZ	Output Disable Time OE to A or B		1.5	7.5	1.5	10.0	1.5	5.0	1.5	6.0	1.5	4.8	1.5	5.2	ns
tpZH tpZL	Output Enable Time T/R to A or B ⁽³⁾		1.5	9.5	1.5	10.0	1.5	6.2	1.5	6.5	1.5	5.8	1.5	6.2	ns
tPHZ tPLZ	Output Disable Time T/R to A or B ⁽³⁾		1.5	7.5	1.5	10.0	1.5	5.0	1.5	6.0	1.5	4.8	1.5	5.2	ns

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SWITCHING CHARACTERISTICS OVER OPERATING RANGE FOR FCT640/A/C

Symbol	Parameter	Condition ⁽¹⁾	54/74FCT640		54/74FCT640A		54/74FCT640C		Unit						
			Com'l.		Mil.		Com'l.			Mil.					
			Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.		Min. ⁽²⁾	Max.				
tPLH tPHL	Propagation Delay A to B, B to A	CL = 50 pF RL = 500Ω	2.0	7.0	2.0	8.0	1.5	5.0	1.5	5.3	1.5	4.4	1.5	4.7	ns
tpZH tpZL	Output Enable Time OE to A or B		2.0	13.0	2.0	16.0	1.5	6.2	1.5	6.5	1.5	5.8	1.5	6.2	ns
tPHZ tPLZ	Output Disable Time OE to A or B		2.0	10.0	2.0	12.0	1.5	5.0	1.5	6.0	1.5	4.8	1.5	5.2	ns
tpZH tpZL	Output Enable Time T/R to A or B ⁽³⁾		2.0	13.0	2.0	16.0	1.5	6.2	1.5	6.5	1.5	5.8	1.5	6.2	ns
tPHZ tPLZ	Output Disable Time T/R to A or B ⁽³⁾		2.0	10.0	2.0	12.0	1.5	5.0	1.5	6.0	1.5	4.8	1.5	5.2	ns

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SWITCHING CHARACTERISTICS OVER OPERATING RANGE FOR FCT645/A/C

Symbol	Parameter	Condition ⁽¹⁾	54/74FCT645		54/74FCT645A		54/74FCT645C		Unit						
			Com'l.		Mil.		Com'l.			Mil.					
			Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.		Min. ⁽²⁾	Max.				
tPLH tPHL	Propagation Delay A to B, B to A	CL = 50 pF RL = 500Ω	1.5	9.5	1.5	11.0	1.5	4.6	1.5	4.9	1.5	4.1	1.5	4.5	ns
tpZH tpZL	Output Enable Time OE to A or B		1.5	11.0	1.5	12.0	1.5	6.2	1.5	6.5	1.5	5.8	1.5	6.2	ns
tPHZ tPLZ	Output Disable Time OE to A or B		1.5	12.0	1.5	13.0	1.5	5.0	1.5	6.0	1.5	4.8	1.5	5.2	ns
tpZH tpZL	Output Enable Time T/R to A or B ⁽³⁾		1.5	11.0	1.5	12.0	1.5	6.2	1.5	6.5	1.5	5.8	1.5	6.2	ns
tPHZ tPLZ	Output Disable Time T/R to A or B ⁽³⁾		1.5	12.0	1.5	13.0	1.5	5.0	1.5	6.0	1.5	4.8	1.5	5.2	ns

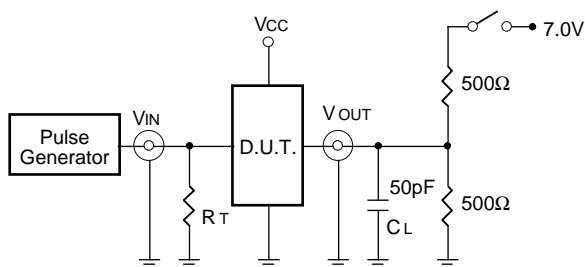
NOTES:

1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. This parameter is guaranteed but not tested.

2534 tbl 09

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUITS FOR ALL OUTPUTS



SWITCH POSITION

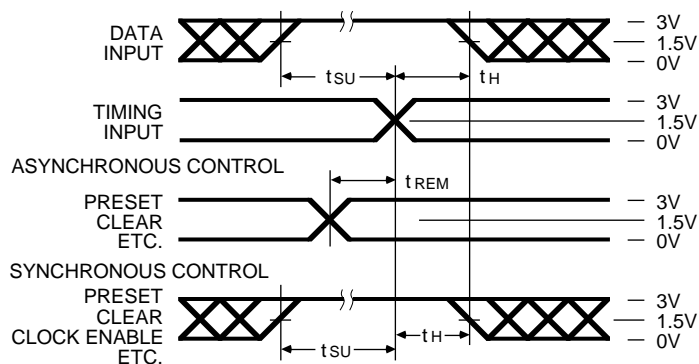
Test	Switch
Open Drain Disable Low Enable Low	Closed
All Other Tests	Open

DEFINITIONS:

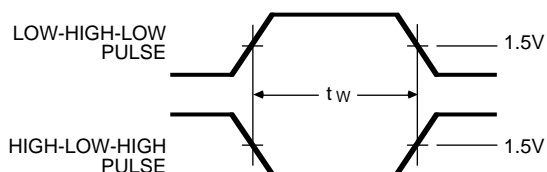
CL = Load capacitance: includes jig and probe capacitance.
RT = Termination resistance: should be equal to ZOUT of the Pulse Generator.

2534 tbl 08

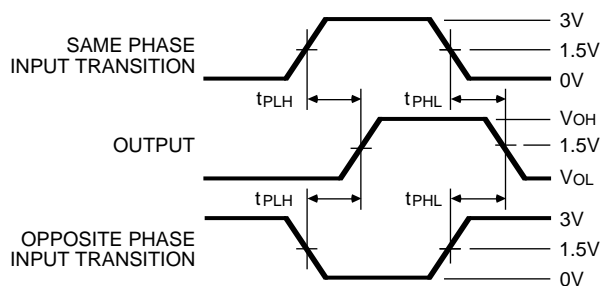
SET-UP, HOLD AND RELEASE TIMES



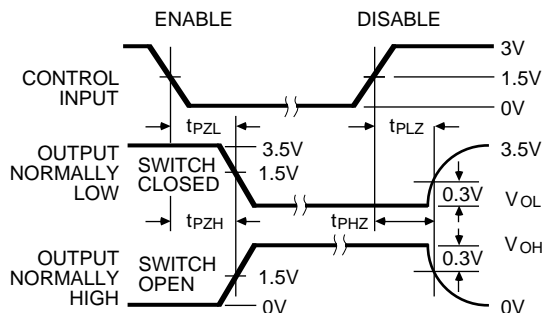
PULSE WIDTH



PROPAGATION DELAY



ENABLE AND DISABLE TIMES

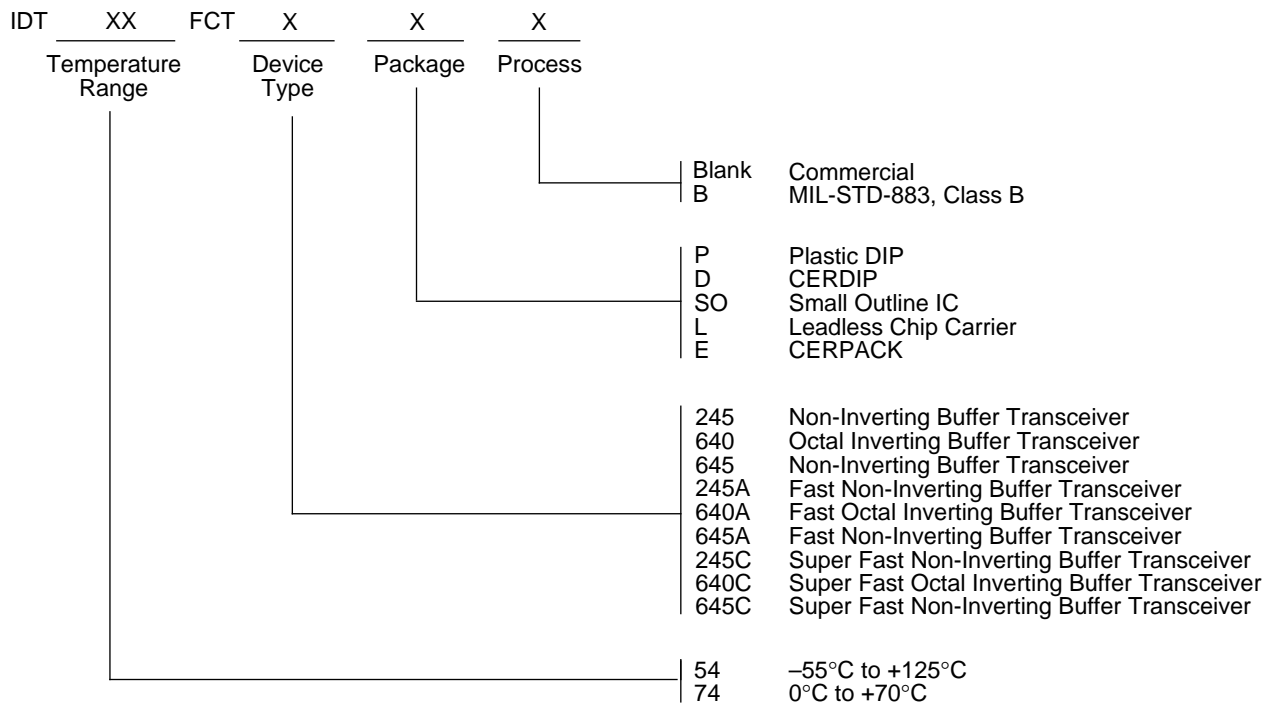


NOTES

- Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.
- Pulse Generator for All Pulses: Rate ≤ 1.0 MHz; $Z_o \leq 50\Omega$; $t_f \leq 2.5$ ns; $t_r \leq 2.5$ ns.

2534 drw 04

ORDERING INFORMATION



2534 drw 03