HM67W1664 Series

65536-word × 16-bit High Speed BiCMOS SRAM

HITACHI

Preliminary
Rev. 4
Sept. 30, 1994

The HM67W1664 is asynchronous high speed static RAM organized as 65536-word × 16-bit. These operate 3.3V. It realizes high speed access time of 10/12 ns by employing 0.5µm Bi-CMOS process technology.

It is most appropriate for applications which require high speed, high density memory and word width configuration, such as cache and buffer memory.

Features

- Single 3.3 V supply.
- Fast access times: 10/12 ns (max).
- Completely static memory.
  No clock or timing strobe required.
- Equal access and cycle times.
- Directly LVTTL compatible.
- All inputs and outputs.
- Low active power: 900/792 mW (max).
- 400-mil 44-pin SOJ package.
- Center V_{CC} and V_{SS} type pinout.

Ordering Information

Type No.	Access time	Package
HM67W1664JP-10	10 ns	400 mil 44 pin plastic SOJ (CP-44D)
HM67W1664JP-12	12 ns	

Note: The specifications of this device are subject to change without notice. Please contact your nearest Hitachi's Sales Dept. regarding specifications.

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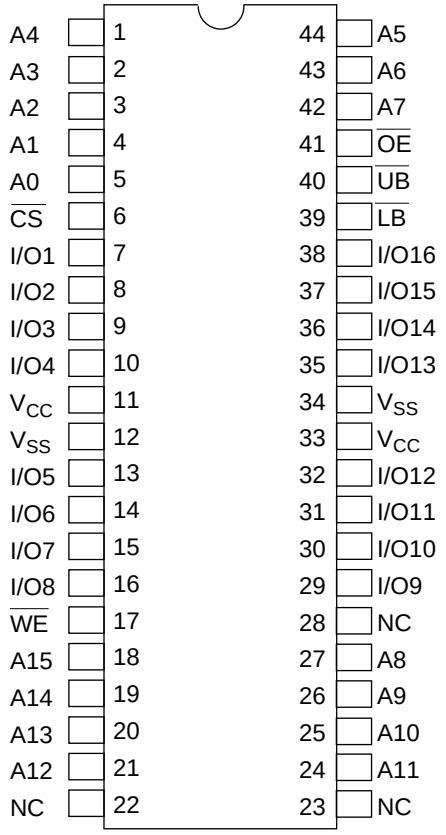
Pin Arrangement

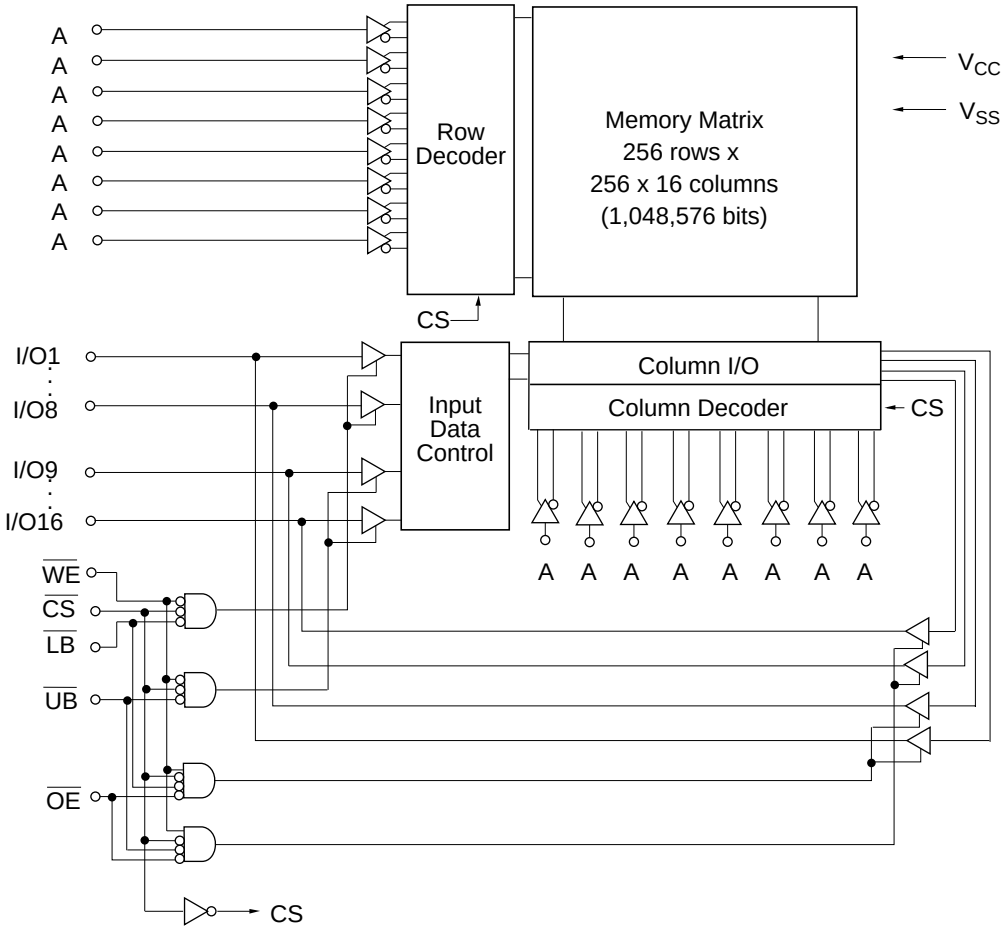


(Top view)

Pin Description

Pin name	Function
A0 to A15	Address
I/O1 to I/O8	Input/output (lower byte)
I/O9 to I/O16	Input/output (upper byte)
$\overline{CS}$	Chip select
$\overline{LB}$	Lower byte select
$\overline{UB}$	Upper byte select
$\overline{OE}$	Output enable
$\overline{WE}$	Write enable
NC	No connection
V_{CC}	Power supply
V_{SS}	Ground

Block Diagram



Function Table

$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	$\overline{LB}$	$\overline{UB}$	V_{CC} current	I/O1 – I/O8	I/O9 – I/O16	Ref. cycle
H	X	X	X	X	I_{SB}, I_{SB1}	High-Z	High-Z	—
L	H	H	X	X	I_{CC}	High-Z	High-Z	—
L	L	H	L	L	I_{CC}	Output	Output	Read cycle
L	L	H	L	H	I_{CC}	Output	High-Z	Read cycle
L	L	H	H	L	I_{CC}	High-Z	Output	Read cycle
L	L	H	H	H	I_{CC}	High-Z	High-Z	—
L	X	L	L	L	I_{CC}	Input	Input	Write cycle
L	X	L	L	H	I_{CC}	Input	High-Z	Write cycle
L	X	L	H	L	I_{CC}	High-Z	Input	Write cycle
L	X	L	H	H	I_{CC}	High-Z	High-Z	—

Note: X: H or L

Absolute Maximum Ratings

Item	Symbol	Value	Unit
Supply voltage relative to V_{SS}	V_{CC}	–0.5 to 4.6	V
Voltage on any pin relative to V_{SS}	Vt	–0.5[*1] to V_{CC} + 0.5 (≤ 4.6 max)	V
Power dissipation	Pt	1.0	W
Operating temperature	Topr	0 to +70	°C
Storage temeprature	Tstg	–55 to +125	°C
Storage temeprature under bias	Tbias	–10 to +85	°C

Notes: 1. –2.0 V for pulse width ≤ 10 ns

Permanent device damage may occur if absolute maximum ratings are exceeded. Under the DC and AC specifications shown in the table, this device is tested under the minimum transverse air flow exceeding 500 linear feet per minuts.

Recommended DC Operating Conditions (Ta = 0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	3.0	3.3	3.6	V
	V_{SS}	0	0	0	V
Input voltage	V_{IH}	2.2	—	V_{CC} + 0.5	V
	V_{IL}	–0.5[*1]	—	0.8	V

Note: 1. –2.0 V for pulse width ≤10 ns.

DC Characteristics (Ta = 0 to 70°C, V_{CC} = 3.3 V ± 0.3 V, V_{SS} = 0 V)

Parameter	Symbol	Min	Typ	Max	Unit		Test conditions
Input leakage current	I_{LI}	—	—	2	µA		Vin = V_{SS} to V_{CC} V_{CC} = 3.6 V
Output leakage current	I_{LO}	—	—	10	µA		$V_{I/O}$ = V_{SS} to V_{CC} $\overline{CS}$ = V_{IH} or $\overline{OE}$ = V_{IH} or $\overline{LB}$ = $\overline{UB}$ = V_{IH} or $\overline{WE}$ = V_{IL}
Operating power supply current	I_{CC}	—	—	250	mA	10 ns cycle	$\overline{CS}$ = V_{IL} Iout = 0 mA Other inputs = V_{IH}/V_{IL}
		—	—	220	mA	12 ns cycle	
Standby power supply current	I_{SB}	—	—	80	mA	10 ns cycle	$\overline{CS}$ = V_{IH} Other inputs = V_{IH}/V_{IL}
		—	—	60	mA	12 ns cycle	
Standby power supply current (1)	I_{SB1}	—	—	15	mA		V_{CC} ≥ $\overline{CS}$, V_{CC} – 0.2 V, 0 V ≤ Vin ≤ 0.2 V or V_{CC} ≥ Vin ≥ V_{CC} – 0.2 V
Output voltage	V_{OL}	—	—	0.4	V		I_{OL} = 4 mA
	V_{OH}	2.4	—	—	V		I_{OH} = –2 mA

Capacitance (Ta = 25, f = 1.0 MHz)*1

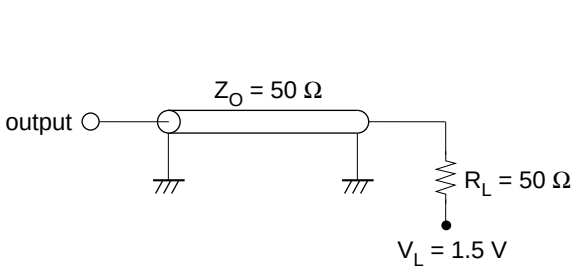
Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Input capacitance	Cin	—	—	5	pF	Vin = 0 V
Input/output capacitance	$C_{I/O}$	—	—	7	pF	$V_{I/O}$ = 0 V

Note: 1. This parameter is sampled and not 100% tested.

AC Characteristics (Ta = 0 to 70°C, V_{CC} = 3.3 V ± 0.3 V, V_{SS} = 0 V, unless otherwise noted.)

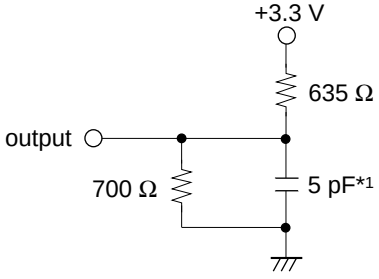
Test conditions

- Input pulse levels: V_{SS} to 3.3 V
- Input rise and fall times: 3 ns
- Input and output timing reference levels: 1.5 V
- Output load: See figures



Output Load A

(t_{AA}, t_{ACS}, t_{OE}, t_{LB}, t_{UB}, t_{OH})



Output Load B

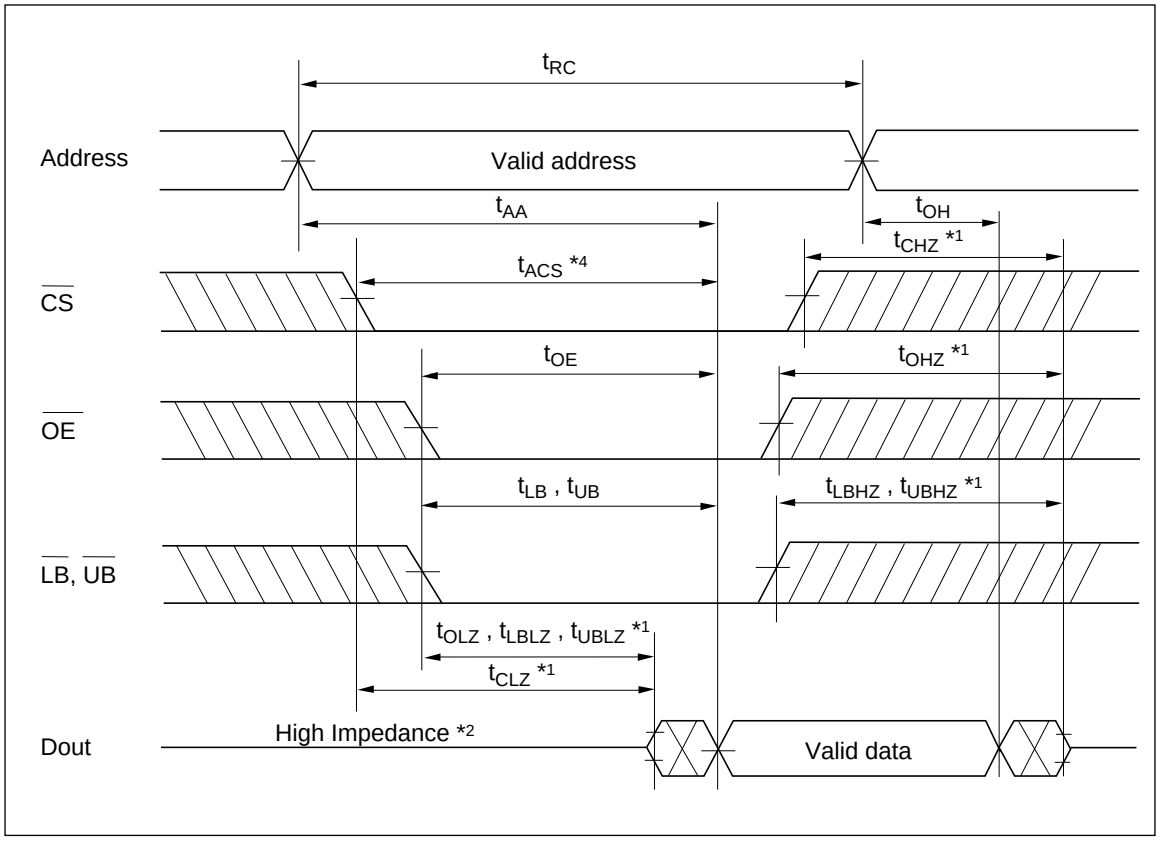
(for t_{CLZ}, t_{OLZ}, t_{LBLZ}, t_{UBLZ}, t_{CHZ}, t_{OHZ}, t_{LBHZ}, t_{UBHZ}, t_{WHZ}, and t_{OW})

Note: 1. Including scope & jig.

Read Cycle

		HM67W1664-10		HM67W1664-12		
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Unit**
Read cycle time	t_{RC}	10	—	12	—	ns
Address access time	t_{AA}	—	10	—	12	ns
Chip select access time	t_{ACS}	—	10	—	12	ns
Output enable to output valid	t_{OE}	—	5	—	6	ns
Byte select to output valid	t_{LB}, t_{UB}	—	5	—	6	ns
Output hold from address change	t_{OH}	3	—	3	—	ns
Chip select to output in low-Z	t_{CLZ}	3	—	3	—	ns
Output enable to output in low-Z	t_{OLZ}	0	—	0	—	ns
Byte select to output in low-Z	t_{LBLZ}, t_{UBLZ}	0	—	0	—	ns
Chip deselect to output in high-Z	t_{CHZ}	—	5	—	5	ns
Output disable to output in high-Z	t_{OHZ}	—	5	—	5	ns
Byte deselect to output in high-Z	t_{LBHZ}, t_{UBHZ}	—	5	—	5	ns

Read Timing Waveform*3

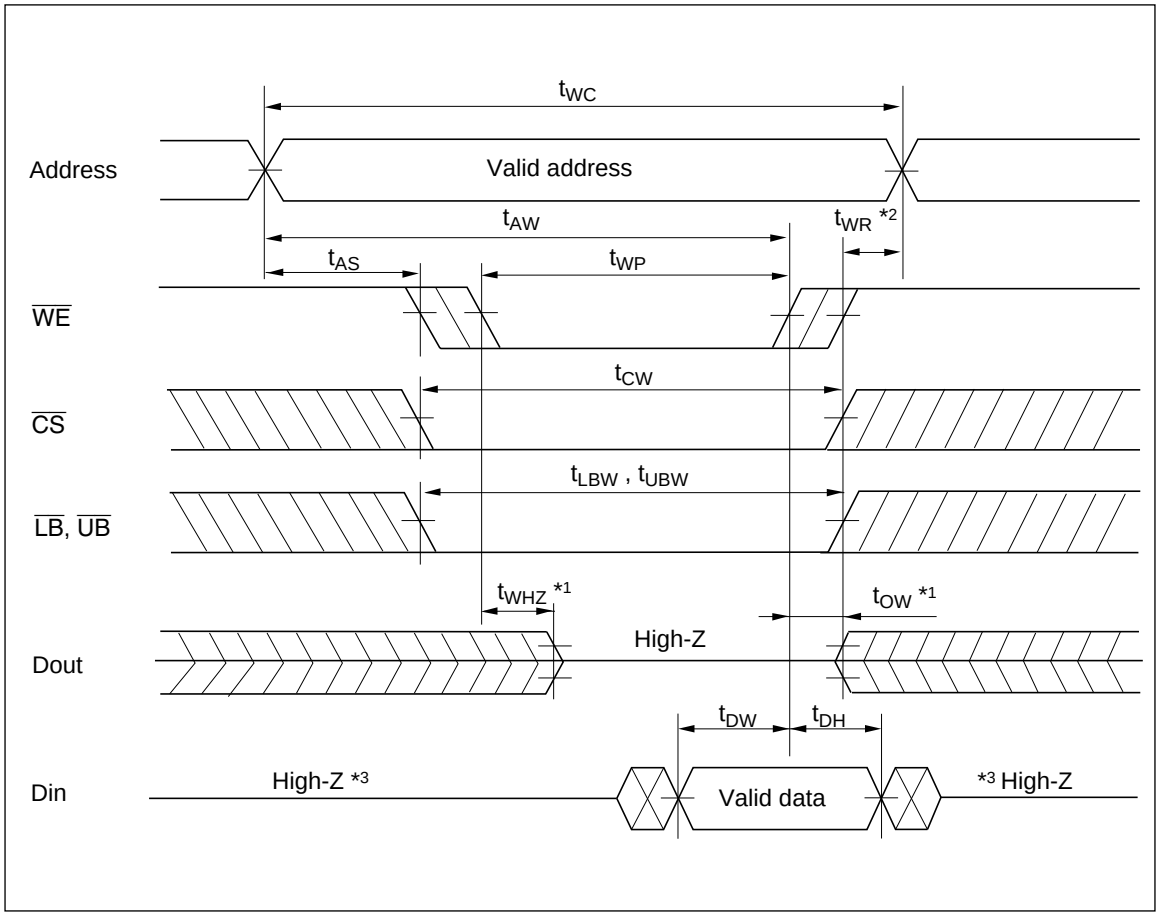


Notes: 1. Transition is measured ±200 mV from steady voltage with Load (B).
This parameter is sampeld and not 100% tested.
2. When $\overline{CS}$, $\overline{OE}$ and $\overline{LB}$ are low, Dout (lower byte) is low impedance.
When $\overline{CS}$, $\overline{OE}$, and $\overline{UB}$ are low, Dout (upper byte) is low impedance.
3. $\overline{WE}$ is high for read cycle.
4. Address valid prior to or coincident with $\overline{CS}$ transition low.

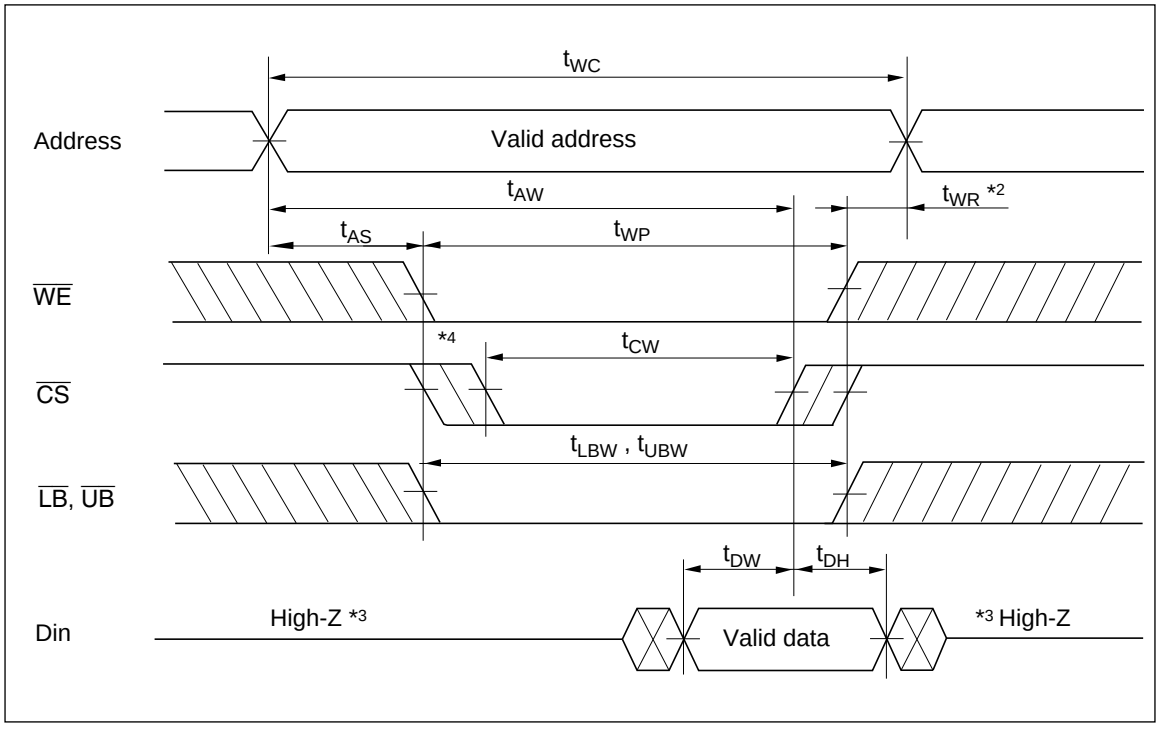
Write Cycle

		HM67W1664-10		HM67W1664-12		
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Unit**
Write cycle time	t_{WC}	10	—	12	—	ns
Address valid to end of write	t_{AW}	9	—	10	—	ns
Chip select to end of write	t_{CW}	9	—	10	—	ns
Write pulse width	t_{WP}	8	—	9	—	ns
Byte select to end of write	t_{LBW}, t_{UBW}	8	—	9	—	ns
Address setup time	t_{AS}	0	—	0	—	ns
Write recovery time	t_{WR}	0	—	0	—	ns
Data valid to end of write	t_{DW}	5	—	6	—	ns
Data hold time from end of write	t_{DH}	0	—	0	—	ns
Write disable to output in low-Z	t_{OW}	3	—	3	—	ns
Write enable to output in high-Z	t_{WHZ}	—	5	—	5	ns

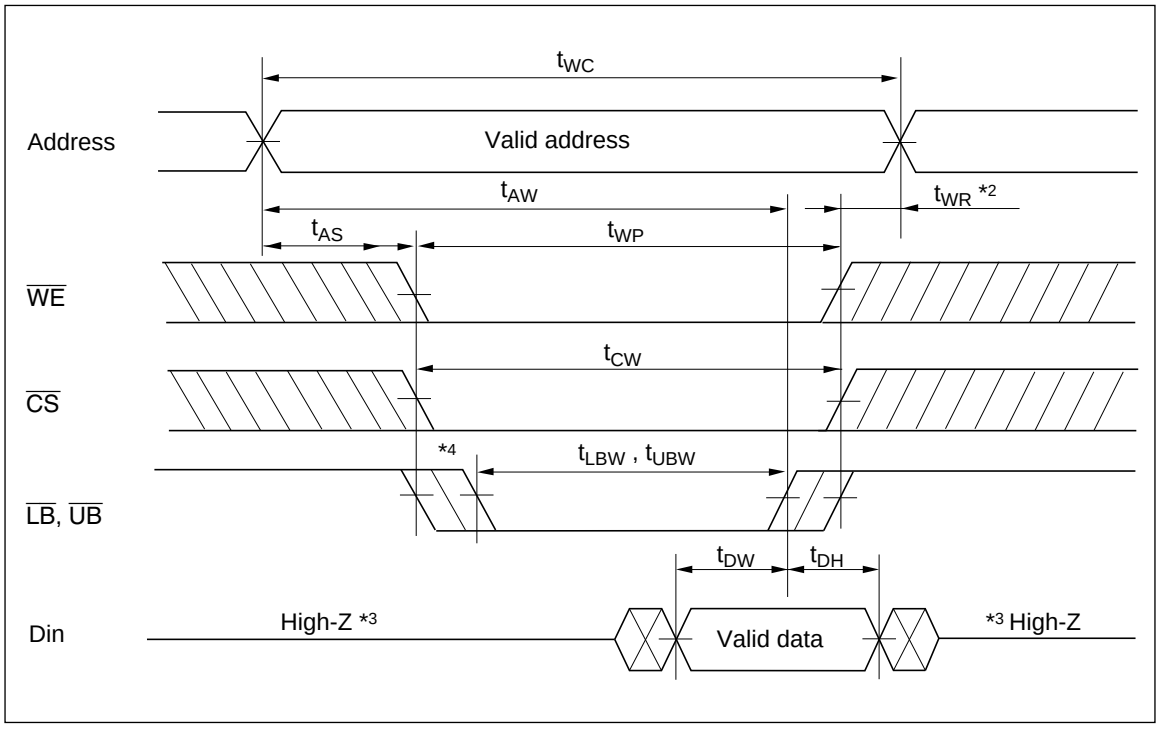
Write Timing Waveforms (1) ($\overline{WE}$ Controlled)



Write Timing Waveform (2) ($\overline{CS}$ Controlled)



Write Timing Waveforms (3) ($\overline{LB}$, $\overline{UB}$ Controlled)



Notes: 1. Transition is measured ±200 mV from high impedance voltage with Load (B).
This parameter is sampled and not 100% tested.

2. $\overline{WE}$ must be high during address transition except when the device is disabled with $\overline{CS}$, $\overline{LB}$ or $\overline{UB}$.
3. If $\overline{CS}$, $\overline{OE}$, $\overline{LB}$, and $\overline{UB}$ are low during this period, I/O pins are in the output state. Then, the data input signals of opposite phase to the outputs must not be applied to them.
4. If the $\overline{CS}$, or $\overline{LB}$ or $\overline{UB}$ low transition occurs simultaneously with the $\overline{WE}$ low transitions or after the $\overline{WE}$ transition, output remains a high impedance state.
5. All write occurs during the overlap of a low $\overline{CS}$, low $\overline{UB}$ of low $\overline{LB}$, and a low $\overline{WE}$ (t_{WP}).
6. All write cycle timings are referred from the last valid address to the first transitioning address.