2.5 Gbit/s 16:1 Multiplexer with Laser Driver Output GD16505

Preliminary

General Information

The GD16505 is a high performance 2.488 Gbit/s 16:1 Multiplexer with on-chip VCO and PLL - system, device applicable for optical communication systems including:

- SDH STM16
- SONET OC-48.

The GD16505 multiplexes sixteen 155 Mbit/s data streams into a single 2.5 Gbit/s data stream output using an external reference clock at 155.52 MHz or 77.6 MHz.

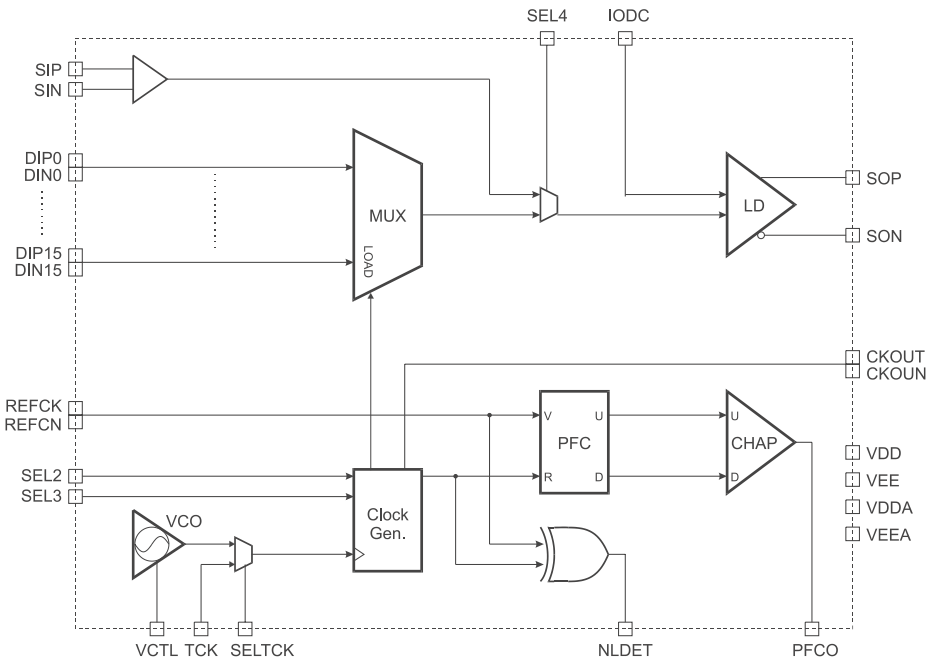
A selecable high-speed data input allows direct 2.5 Gbit/s input to the laser driver.

Internal clock synchronisation is provided by an on-chip PLL circuit requiring a simple passive external loop filter. The PLL circuit features an NLDET pin output for simple implementation of a lock detect function, as shown overleaf.

The multiplexed data stream is outputted by a high modulation-current laser driver with an adjustable modulation-current in the range of 5 – 80 mA.

Mark/space ratio may be monitored as a DC voltage between the two pins MSO and MSNO, provided a decoupling capacitor is connected between the pins.

It is packaged in a 68 pin leaded Multi Layer Ceramic (MLC) package with 50 Ω transmission lines and cavity down for easy cooling/heat sinking.



Features

- SDH STM-16, SONET OC-48 compatible.
- On-chip PLL containing low jitter 2.5 GHz VCO, phase/frequency detector and charge pump.
- PLL lock detect output.
- On-chip high modulation current laser driver (80 mA typ.).
- Adjustable skew and pulse width.
- Single -5.2 V supply operation.
- Differential ECL compatible data and clock inputs.
- Power dissipation: 1.0 W (typ.).
- Packaged in:
  – a 68 pin leaded Multi Layer Ceramic (MLC) package
- The GD16505-68BA is 100% interchangeable with GD16055.

Applications

- Tele Communications
  – SDH STM-16
  – SONET OC-48 systems
- Data Communications

Functional Details

The GD16505 consists of 3 major functional parts:

- a 16:1 MUX unit
- a PLL (PFD) system
- a laser driver.

The function of the MUX is to multiplex the 16-bit word DIx0-DIx15 into a 16-bit serial-data stream. The order of bits in the multiplexed bit stream is DIx15 as the first coming bit and then DIx14, …, DIx1, and DIx0.

The multiplexed bit stream is buffered and converted to an output current in the laser driver in order to interface to a 25 Ω/50 Ω laser diode (or external impedance). Logic HI means output current in pin SON (i.e. laser on for 50 Ω laser diode interface) and output current in pin SOP LO (i.e. laser off for 25 Ω laser diode interface).

On GD16505-68BA, the laser driver is coupled as a CML output, i.e. Logic HI means High voltage on pin SOP.

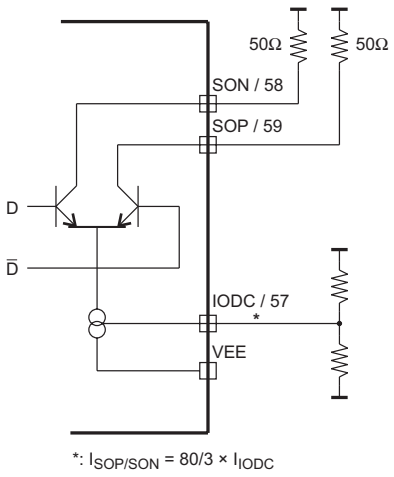


Figure 1. *CML Output (68BA)*

The PLL system consists of a low-jitter LC type VCO running at approximately 2.5 GHz, an analog phase/frequency detector and a charge pump.

The 2.5 GHz VCO, is locked to an external reference clock selectable at 155.52 MHz or 77.6 MHz.

The 16:1 MUX can be bypassed by setting the SEL4 input high, thus selecting the 2.5 Gbit/s ECL inputs SIP / SIN.

Application Details

PLL Loop Filter and PLL Reset

The recommended loop filter for the GD16505 is shown in Figure 2. This loop filter is used in the AC production test set-up and has been found to ensure that the jitter performance of GD16505 is within ITU specifications.

The optimum choice of component values with regard to jitter is affected by the reference clock phase-noise performance.

For noise and jitter reasons it is very important that the capacitor is connected to VDD/VDDA close to VCTL pin.

Lock Detect Circuit

A simple PLL lock detect function can be implemented by 3 external components (R3, C3 and ST1), comprising a low-pass filter followed by a Schmitt trigger, as shown in Figure 2.

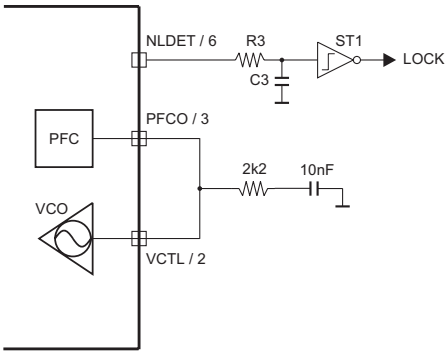


Figure 2. *PLL Loop Filter (68BA)*

Laser Driver Current Control

The output modulation current is controlled by the pin IODC and can be controlled in the range from 5 mA to 80 mA.

The output voltage swing across the external load may be varied accordingly. The modulation current control on pin IODC is implemented as a current mirror and therefore sinks a current proportional to the modulation current. The current sink into the IODC pin is 3/80 of the modulation current.

By using an external general-purpose operational amplifier the laser current may be controlled accurately and independent of environmental changes.

The op-amp must be able to drive the IODC pin input in the range V_{EE} -2.0 V to V_{EE} +1.2 V.

GD16505-68BA

The GD16505-BA version is made to give the old customers of GD16055 a plug compatible silicon device with improved AC and DC.

The 68 lead MLC package sets some limitation to the functionality of the device.

Also the limited number of pins has reduced the selectable reference clock, hence only 155.52 MHz is available.

On GD16505-68BA, the laser driver is coupled as a CML output, i.e. the polarity is a high voltage on SOP for logic high, also current specifications have been reduced to 30 mA in 50 Ω. And all special control inputs on the laser driver have been removed leaving only IODC for controlling the output current.

Pin List

Mnemonic:	Pin number 68BA	TBD	Pin Type:	Description:
DIP0, DIN0 DIP1, DIN1 DIP2, DIN2 DIP3, DIN3 DIP4, DIN4 DIP5, DIN5 DIP6, DIN6 DIP7, DIN7 DIP8, DIN8 DIP9, DIN9 DIP10, DIN10 DIP11, DIN11 DIP12, DIN12 DIP13, DIN13 DIP14, DIN14 DIP15, DIN15	8, 7 11, 10 13, 12 16, 15 20, 19 23, 22 25, 24 28, 27 33, 32 37, 36 40, 39 42, 41 45, 44 47, 46 50, 49 54, 53		ECL IN	Differential data inputs. Shifted to the serial output starting with DI15, followed by DI14, DI13....
SIP, SIN	63, 62		CML IN	Differential serial input. High speed self-terminating input to be used in conjunction with GD16504 for remote/line loop back.
REFCK, REFCN	67, 66		ECL IN	Reference clock differential input for PLL.
SEL1*			ECL IN	Sselect signal for reference clock frequency. When high, 155.52 MHz is selected; when low, 77.76 MHz. Bonded high for 155.52 MHz option in current package pinout. * In the 68BA version this pin is internally set low.
SEL2, SEL3*	61		ECL IN	Phase relation select between positive going edge of CKOUT and sample time of input data: SEL3, SEL2 1 1 T_{DEL} = 0° 1 0 T_{DEL} = 90° 0 1 T_{DEL} = 180° 0 0 T_{DEL} = 270° *SEL3 is internally set to high in the 68BA version.
SEL4	35		ECL IN	Select between MUX or Serial Input as source for the output buffer. When high, MUX is selected; low, Serial Input.
IODC	57		Anl. IN	Serial Output Current control. Ratio I_{IODC} to $I_{SOP/SON}$ is 3:80.
VCTL	2		Anl. IN	VCO voltage control input.
TCK	64		ECL IN	Test clock input. Replaces the VCO as clock source when SELTCK is set to high.
SOP, SON	59, 58		OC OUT	Open Collector Differential Serial Output, 2.488 Gbit/s.
CKOUT, CKOUN	29, 30		ECL OUT	155.52 MHz subdivided VCO-clock. Phase relation between this output and sample point of input data configurable by SEL2, 3.
PFCO	3		Anl. OUT	Phase/ frequency comparator output. Changes between Drive High - Tristate - Drive Low according to VCO phase and freq. with respect to REFCK.
NLDET	6		Anl. OUT	Inverted Lock Detect output. Refer to Figure 2 for connection.
SELTCK	17		ECL IN	Select TCK for Clock input. For DC test only. Connect to VEE for normal operation.
VDD	4, 9, 14, 21, 26, 31, 38, 43, 48, 55, 60, 65		PWR	0 V Power for core and ECL I/O.
VEE	34		PWR	-5 V Power for core and ECL I/O.
VDDA	1		PWR	0 V Power for VCO.
VEEA	18, 68		PWR	-5 V Power for VCO.

Mnemonic:	Pin number 68BA	TBD	Pin Type:	Description:
VEEP	52		PWR	-5 V Power for High Speed Output Driver (SOP / SON).
NC	5 56 51		NC	Not connected. BBDO in GD16055. Not connected. MSYM in GD16055 Not connected.

Package Pinout

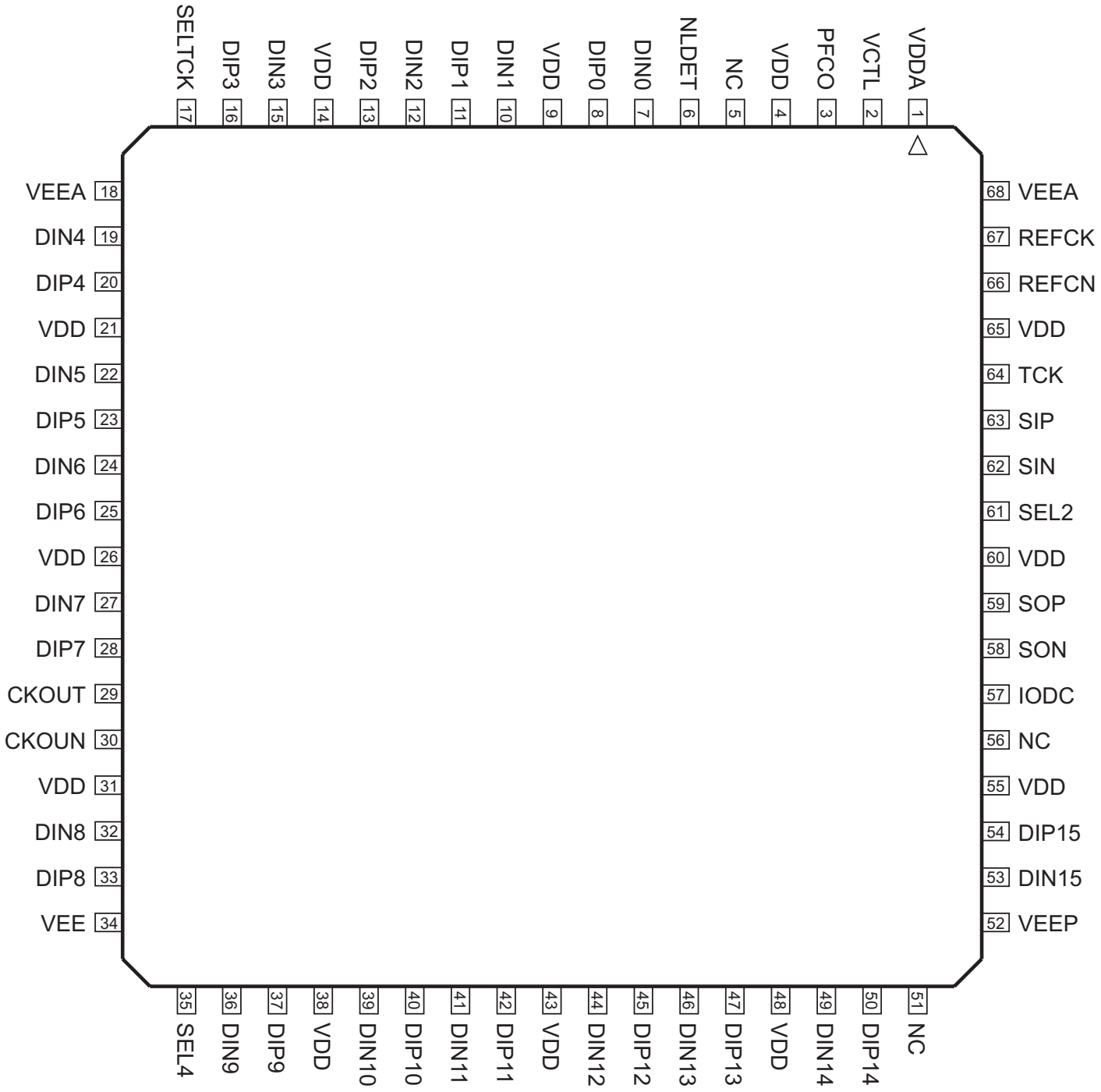


Figure 3. *Package Pinout, 68BA – Top View*

Maximum Ratings

These are the limits beyond which the component may be damaged.
All voltages in the table are referred to VDD (Ground).
All currents in the table are defined positive out of the pin.

Symbol:	Characteristic:	Conditions:	MIN.:	TYP.:	MAX.:	UNIT:
V_{EE}, V_{EEA}, V_{EEP}	Power Supply		-5.5		0	V
V_O	Applied Voltage (all outputs)		V_{EE} -0.5		0.5	V
$I_{O\ ECL}$	Output Current ECL		-10		40	mA
$I_{O\ NLDET}$	Output Current NLDET		-3		8	mA
$I_{O\ MSO,MSNO}$	Output Current MSO,MSNO		-4		4	mA
V_I	Applied Voltage (all inputs except VMOD)		V_{EE} -0.5		0.5	V
$V_{I\ VMOD}$	Applied Voltage to VMOD	Note 1	V_{EE} -2.0		V_{EE} +1.4	V
$V_{IO\ ESD}$	ESD I/O Sensitivity	Note 2		±500		V
$I_{I\ ECL}$	Input Current ECL		-1		1	mA
$I_{I\ SYM}$	Input Current SYM		-4		4	mA
$I_{I\ VMOD}$	Input Current VMOD	Note 1	-4		4	mA
T_O	Operating Temperature	Junction	-40		+125	°C
T_S	Storage Tempeature		-65		+150	°C

Note 1: Voltage and/or current should be externally limited to specified range.
Note 2: Human body model (100 pF, 1500 Ω) MIL 883 method.

DC Characteristics

T_{CASE} = 0 °C to 85 °C, V_{EE} = -4.75 V to -5.25 V
All voltages in the table are referred to VDD.
All input signal and power currents in the table are defined positive into the pin.
All output signal currents are defined positive out of the pin.

Symbol:	Characteristic:	Conditions:	MIN.:	TYP.:	MAX.:	UNIT:
V_{EE}	Supply Voltage		-5.25		-4.75	V
I_{EE}	Supply Current			200	250	mA
P_{DISS}	Power Dissipation			1000		mW
$V_{IH\ ECL}$	ECL Input HI Voltage		-1.1		-0.7	V
$V_{IL\ ECL}$	ECL Input LO Voltage	Note 1	V_{EE}		-1.5	V
$I_{IH\ ECL}$	ECL Input HI Current	V_{IH} = - 0.7		12	100	mA
$I_{IL\ ECL}$	ECL input LO Current	V_{IL} = -1.8		0.01	-1.0	mA
$V_{OH\ ECL}$	ECL Output HI Voltage	Note 1, 3	-1.0		-0.5	V
$V_{OL\ ECL}$	ECL Output LO Voltage	Note 1, 3	V_{TT}		-1.6	V
$I_{OH\ ECL}$	ECL Output HI Current	Note 4	20	23	30	mA
$I_{OL\ ECL}$	ECL Output LO Current	Note 4	-2	5	8	mA
$V_{OH\ NLDET}$	NLDET Output HI Voltage		-1.2		0	V
$V_{OL\ NLDET}$	NLDET Output LO Voltage		V_{EE}		V_{EE}+1.2	V
$I_{OH\ NLDET}$	NLDET Output HI Current		1			mA
$I_{OL\ NLDET}$	NLDET Output LO Current		-1			mA
V_{CTL}	VCO Control Voltage	I_{VCTL}< 30 μA	V_{EE}		-0.5	V
V_{IODC}	Output Current Control Input		V_{EE}		V_{DD}	V
I_{IODC}	Output Current Control Input	V_{IODC} = -2.5 V	0		3	mA
$V_{O\ SOP,\ SON}$	Open Collector Output Voltage	Note 2	-3		-0.05	V
$I_{DR\ SOP,\ SON}$	Open Collector Output Drive Current	Note 2	-60		-5	mA
$I_{CO\ SOP,SON}$	Open Collector Output Cut-off Current	Note 2	-3		1	A
$I_{OH\ PFCO}$	PFCO Output HI Current	Note 5	20	100		μA
$I_{OL\ PFCO}$	PFCO Output LO Current	Note 5		-100	20	μA

Note 1: V_{TT} = -2.0 V ± 5 %.
Note 2: R_{load} = 50 Ω to*VDD*. Sink current is controlled by current into IODC pin. Data logic Low (“0") corresponds to SOP driving low.
Note 3: R_{load} = 50 Ω to V_{TT}.
Note 4: Not tested, consistent with V_{OH} and V_{OL} tests.
Note 5: Output terminated to -2.5 V during test.

AC Characteristics

T_{CASE} = 0 °C to 85 °C, V_{EE} = -4.75 V to -5.25 V.

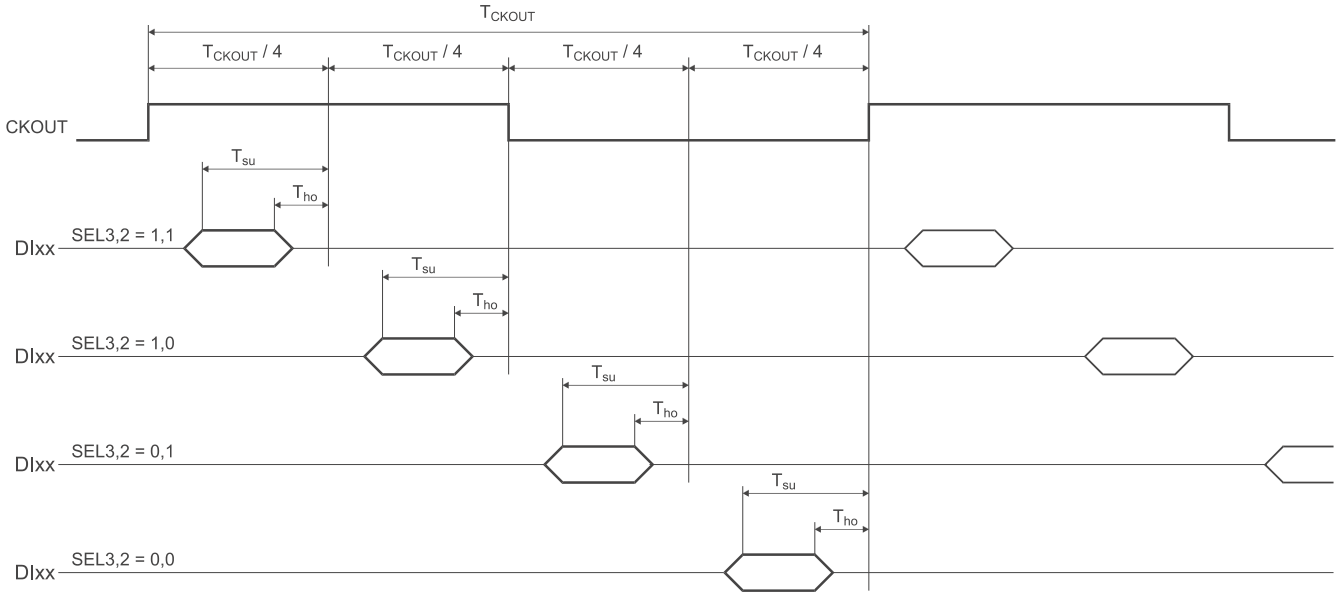
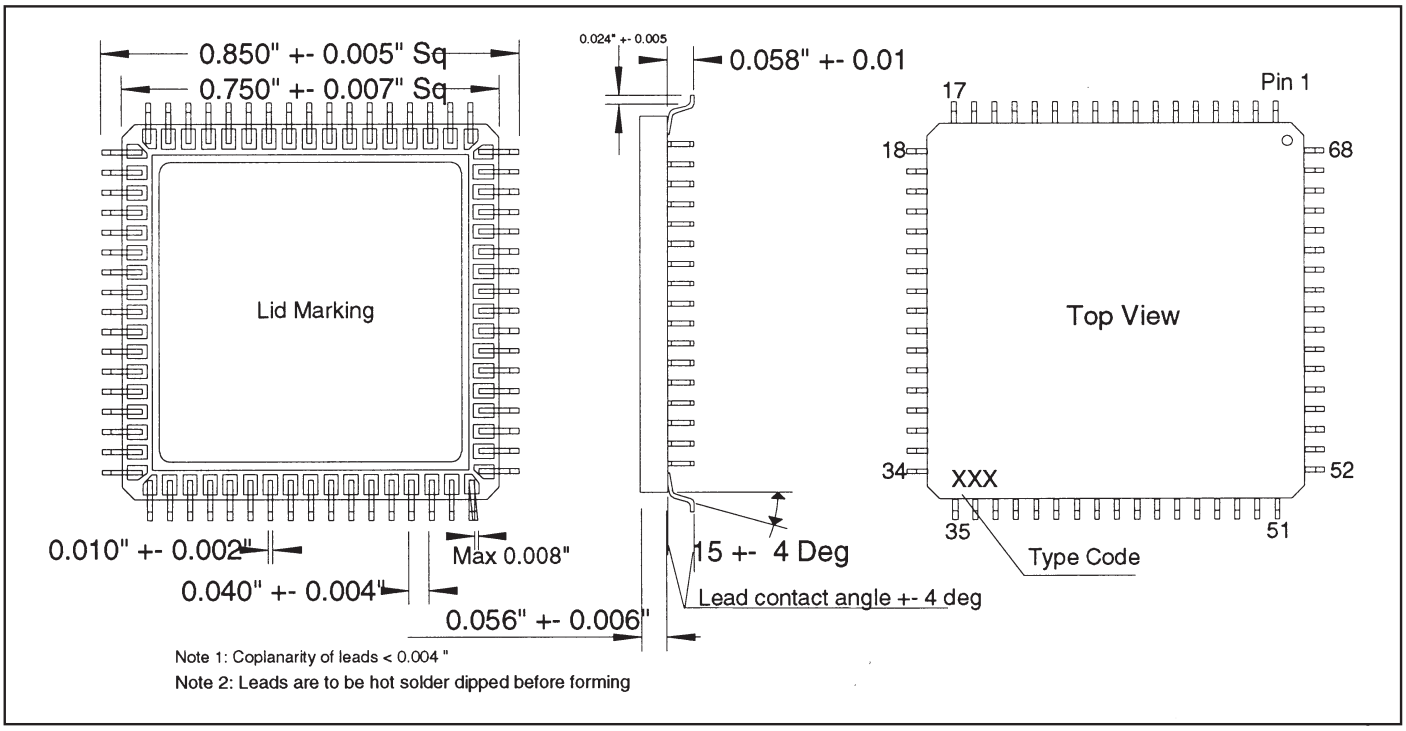


Figure 4. *DI0..DI15 Data Input Set-up and Hold with respect to CKOUT*

Symbol:	Characteristic:	Conditions:	MIN.:	TYP.:	MAX.:	UNIT:
J_{Gen}	Jitter Generation	12 kHz < f_C < 20 MHz (Note 1)			0.01	$UI_{16, RMS}$
J_{Trf}	Jitter Transfer	12 kHz < f_C < 2 MHz (Note 2)			0.01	dB
J_{Clk}	Output Clock Intrinsic Jitter	5 kHz < f < 20 MHz (Note 3) 1 MHz< f < 20 MHz (Note 3)		0.125 0.05	0.5 0.1	$UI_{16, p-p}$ $UI_{16, p-p}$
$T_{LH\ OC}$	Open Collector Output Rise Time	20 – 80 % (Note 4)		120	150	ps
$T_{HL\ OC}$	Open Collector Output Fall Time	80 – 20 % (Note 4)		120	150	ps
$T_{LH\ Clock}$	CKOUT/ CKOUN Rise Time	20 – 80 %, 50 Ω to -2 V		350	700	ps
$T_{THL\ Clock}$	CKOUT/ CKOUN Fall Time	80 – 20 %, 50 Ω to -2 V		350	700	ps
$T_{LH\ ECL}$	ECL Output Rise Time	20 – 80 %, 50 Ω to -2 V		350	700	ps
$T_{THL\ ECL}$	ECL Output Fall Time	80 – 20 %, 50 Ω to -2 V		350	700	ps
$C_{DUTY\ REFCK}$	REFCK Clock Duty Cycle	$V_{Thresh.}$= -1.3 V	40		60	%
$C_{DUTY\ CKOUT}$	Output Clock Duty Cycle	$V_{Thresh.}$= -1.3 V, 50 Ω to -2 V	45		55	%
T_{su}	DIN Set-up before CKOUT		-1600			ps
T_{ho}	DIN Hold from CKOUT				-400	ps
F_{REFCK}	REFCK, REFCN Input Frequency		144 72	155.5 77.76	163 81.5	MHz MHz
$F_{SOP,\ SON}$	Open Collector Output Bit Rate			2.488		Gbit/s
K_{VCO}	VCO Gain Constant	Measured at operating point		150		MHz/V
$N_{Parallel\ -\ Serial}$	No. of bits stored in pipe-lines				40	bits

Note 1: UI_{16} = 402ps.
Note 2: Loop filter as described in Figure 2.
Note 3: In the absence of input jitter, the intrinsic jitter at CKOUT as measured over a 60 seconds interval shall not exceed these limits.
Note 4: R_{load} = 50 Ω to *VDD*. I_{LD} = 20 mA.

Package Outline - 68BA



Device Marking

Ordering Information

Product Name:	Package Type:	Case Temperature Range:	Options:
GD16505-68BA	68 pin Ceramic (MLC)	0..85 °C	
TBD	144 pin fpBGA	0..85 °C	

GD16505, Data Sheet Rev. 04 - Date: 23 November 1998

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