*Multi*GEN™ GF9320
Scaling Processor

PRELIMINARY DATA SHEET

FEATURES

- high performance 2D scaling processor with full user independent control of horizontal and vertical scaling factors and pan positions
- support for multiple data formats up to 2048 by 2048 image resolution
- the frame rate is limited by the maximum I/O clock rate of 90MHz
- inputs support multiplexed YC or separate Y & C at 8 or 10-bits
- outputs support multiplexed YC or separate Y & C or separate RGB at 8 or 10-bits
- field merge/separation can be inserted/removed from progressive images using interlaced I/O
- 3:2/2:2 pull-down insertion and extraction
- programmable output matrix with 6dB gain range
- fully programmable colour background generator
- TRS can be inserted on all video output and illegal words removed
- seamless interface to external SDRAM for external image delays
- user configuration through dedicated serial interface
- 3.3V supply
- 352 pin TBGA

DESCRIPTION

The GF9320 Scaling Processor offers broadcast quality scaling of video images as well as graphic images up to 2048 by 2048 pixel resolution. In addition, it provides for pan, scan and zoom/shrink abilities. A fully programmable output matrix provides for colour difference over-sampling, matrix to RGB conversions, gain and hue controls. The GF9320 offers colour background and output TRS insertion.

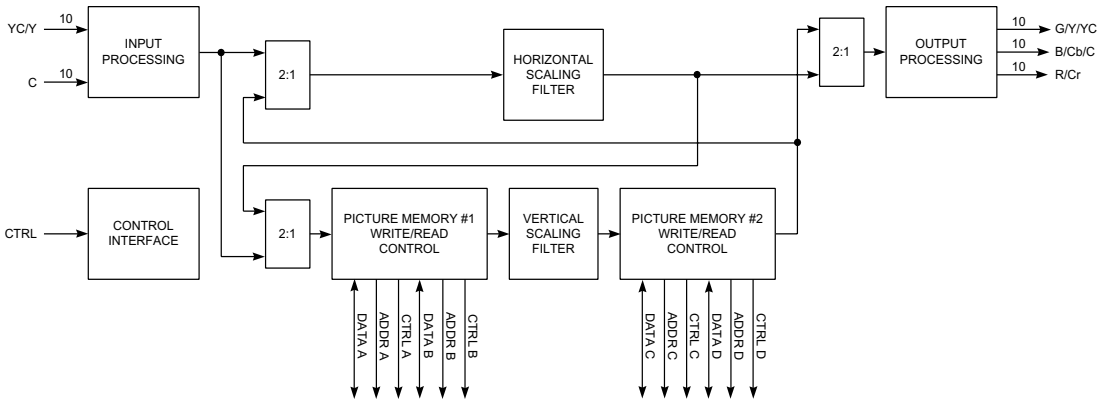
In combination with the GF9330 High Performance De-interlacer and the GF9331 Motion Co-processor, the GF9320 offers the ideal format conversion solution for those desiring broadcast quality in a three-chip solution and support for applications up to 1080P60.

APPLICATIONS

- SDTV ↔ HDTV format converters
- Aspect ratio converters
- Projection systems
- Plasma displays
- Production equipment, e.g. switches, cameras, telecines
- HD-DVD Players
- DTV set-top box
- Video walls

ORDERING INFORMATION

PART NUMBER	PACKAGE	TEMP RANGE
GF9320-CBW	352 pin TBGA	0°C to 70°C



BLOCK DIAGRAM

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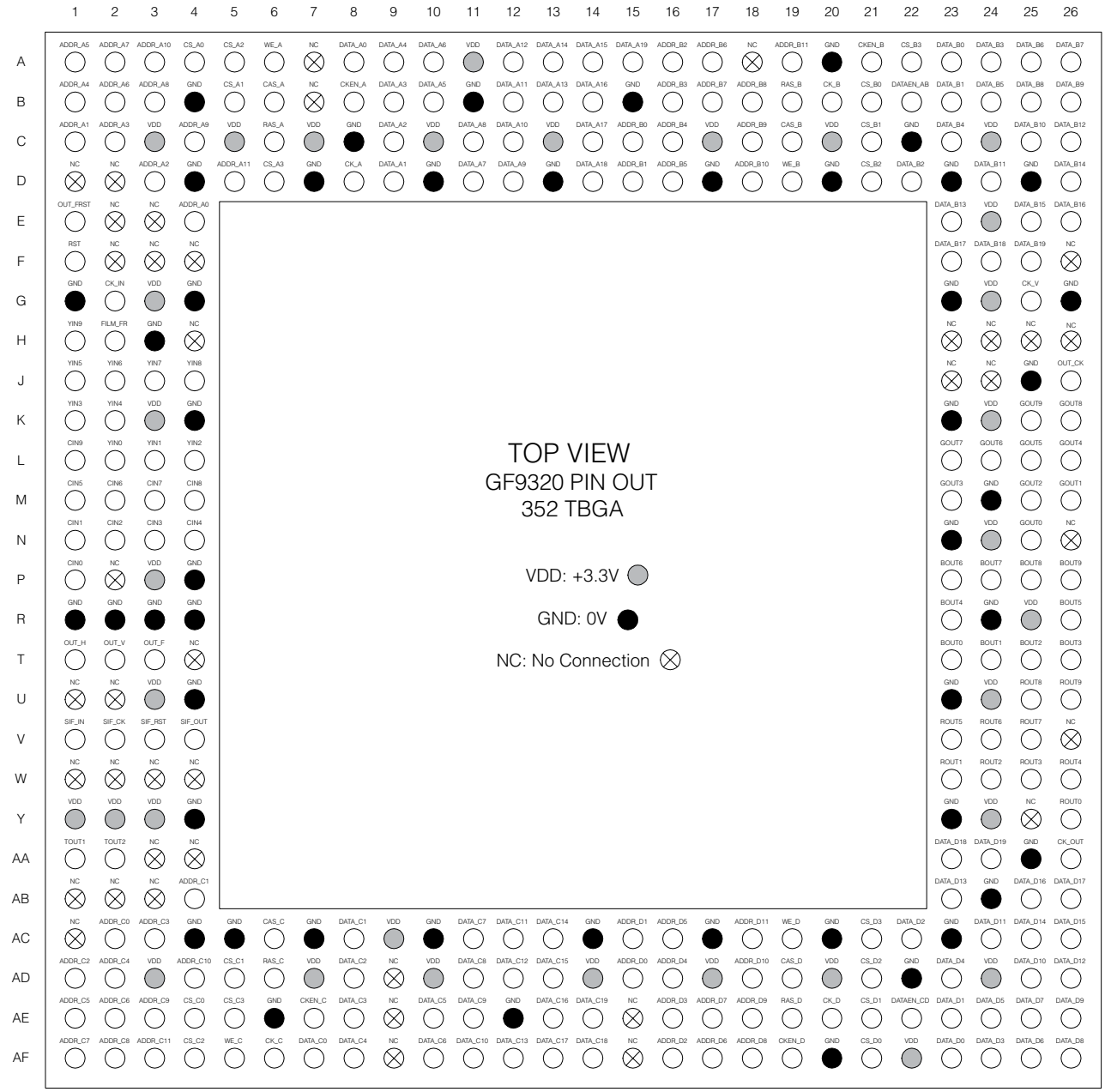

Fig. 1 GF9320 Pin Out

PIN DESCRIPTION

SYMBOL	PIN GRID	TYPE	DESCRIPTION
YIN[9:0]	H1, J4, J3, J2, J1, K2, K1, L4, L3, L2	I	10-bit multiplexed signed luminance/signed offset colour difference data input Note - either input must include TRS words
CIN[9:0]	L1, M4, M3, M2, M1, N4, N3, N2, N1, P1	I	10-bit signed offset colour difference data input
CK_IN	G2	I	Input clock Note - equals Y data rate for separate Y and C inputs and is equal to 2x Y data rate for multiplexed YC input
CK_V	G25	I	Vertical processing clock Note - usually the higher of CK_IN or CK_OUT
OUT_CK	J26	O	Output clock timed to clock output data
FILM_FR	H2	I	Input film sequence reset
OUT_FRST	E1	I	Output frame reset
RST	F1	I	Power-on reset
SIF_IN	V1	I	Serial interface control data in
SIF_OUT	V4	O	Serial interface control data out
SIF_CK	V2	I	Serial interface clock
SIF_RST	V3	I	Serial interface reset
GOUT[9:0]	K25, K26, L23, L24, L25, L26, M23, M25, M26, N25	O	8/10-bit unsigned green data output or 8/10-bit unsigned luminance data output or 8/10-bit multiplexed signed luminance/signed offset colour difference data output
BOUT[9:0]	P26, P25, P24, P23, R26, R23, T26, T25, T24, T23	O	8/10-bit unsigned blue data output or 8/10-bit signed offset (B-Y) data output
ROUT[9:0]	U26, U25, V25, V24, V23, W26, W25, W24, W23, Y26	O	8/10-bit unsigned red data output or 8/10-bit signed offset (R-Y) data output
CK_OUT	AA26	I	Output clock
OUT_F	T3	O	Output format frame/field signal
OUT_V	T2	O	Output format vertical signal
OUT_H	T1	O	Output format horizontal signal
DATA_A[19:0]	A15, D14, C14, B14, A14, A13, B13, A12, B12, C12, D12, C11, D11, A10, B10, A9, B9, C9, D9, A8	I/O	Data bus for memory array A
DATA_B[19:0]	F25, F24, F23, E26, E25, D26, E23, C26, D24, C25, B26, B25, A26, A25, B24, C23, A24, D22, B23, A23	I/O	Data bus for memory array B
DATA_C[19:0]	AE14, AF14, AF13, AE13, AD13, AC13, AF12, AD12, AC12, AF11, AE11, AD11, AC11, AF10, AE10, AF8, AE8, AD8, AC8, AF7	I/O	Data bus for memory array C
DATA_D[19:0]	AA24, AA23, AB26, AB25, AC26, AC25, AB23, AD26, AC24, AD25, AE26, AF26, AE25, AF25, AE24, AD23, AF24, AC22, AE23, AF23	I/O	Data bus for memory array D

PIN DESCRIPTION [continued]

SYMBOL	PIN GRID	TYPE	DESCRIPTION
ADDR_A[11:0]	D5, A3, C4, B3, A2, B2, A1, B1, C2, D3, C1, E4	O	Address bus for memory array A
ADDR_B[11:0]	A19, D18, C18, B18, B17, A17, D16, C16, B16, A16, D15, C15	O	Address bus for memory array B
ADDR_C[11:0]	AF3, AD4, AE3, AF2, AF1, AE2, AE1, AD2, AC3, AD1, AB4, AC2	O	Address bus for memory array C
ADDR_D[11:0]	AC18, AD18, AE18, AF18, AE17, AF17, AC16, AD16, AE16, AF16, AC15, AD15	O	Address bus for memory array D
CS_A[3:0]	D6, A5, B5, A4	O	Chip select for memory array A
CS_B[3:0]	A22, D21, C21, B21	O	Chip select for memory array B
CS_C[3:0]	AE5, AF4, AD5, AE4	O	Chip select for memory array C
CS_D[3:0]	AC21, AD21, AE21, AF21	O	Chip select for memory array D
RAS_A	C6	O	Row address strobe for memory array A
RAS_B	B19	O	Row address strobe for memory array B
RAS_C	AD6	O	Row address strobe for memory array C
RAS_D	AE19	O	Row address strobe for memory array D
CAS_A	B6	O	Column address strobe for memory array A
CAS_B	C19	O	Column address strobe for memory array B
CAS_C	AC6	O	Column address strobe for memory array C
CAS_D	AD19	O	Column address strobe for memory array D
WE_A	A6	O	Write enable for memory array A
WE_B	D19	O	Write enable for memory array B
WE_C	AF5	O	Write enable for memory array C
WE_D	AC19	O	Write enable for memory array D
CK_A	D8	O	Clock for memory array A
CK_B	B20	O	Clock for memory array B
CK_C	AF6	O	Clock for memory array C
CK_D	AE20	O	Clock for memory array D
CKEN_A	B8	O	Clock enable for memory array A

PIN DESCRIPTION [continued]

SYMBOL	PIN GRID	TYPE	DESCRIPTION
CKEN_B	A21	O	Clock enable for memory array B
CKEN_C	AE7	O	Clock enable for memory array C
CKEN_D	AF19	O	Clock enable for memory array D
DATAEN_AB	B22	O	Data enable for memory arrays A and B
DATAEN_CD	AE22	O	Data enable for memory arrays C and D
VDD	K3, C10, A11, P3, C13, U3, C17, Y3, C20, AD3, G3, AD7, AC9, AD10, AD14, AD17, C24, AD20, AF22, AD24, E24, Y24, G24, K24, C5, N24, C3, U24, R25, C7, Y1, Y2	I	
GND	R24, U23, N23, K23, G26, G23, Y23, D25, AC20, AF20, AC17, D23, AC14, AC10, AC7, AC5, AC4, D20, A20, Y4, D17, B15, U4, D13, P4, B11, D10, K4, D7, G4, B4, D4, AC23, C8, H3, J25, AE6, C22, AE12, M24, AD22, G1, AB24, AA25, R1, R2, R3, R4	I	
NC	H26, W2, W3, J23, W4, T4, U1, U2, J24, A7, A18, AA3, AA4, W1, AB1, AB2, F26, AC1, AB3, N26, Y25, F2, V26, F3, P2, B7, D2, AD9, E3, H24, AE9, D1, AF9, E2, AE15, AF15, F4, H23, H25, H4, AA1, AA2		No connection

1. ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	CONDITIONS	RATED VALUE	UNITS
Power Supply Voltage	V_{DD}		-0.5 to +4.6	V
Input Voltage	V_I	VI < VDD + 0.5 V	-0.5 to +4.6	V
Output Voltage	V_O	VO < VDD + 0.5 V	-0.5 to +4.6	V
Output Current	I_O		40	mA
Operating Temperature	T_A		0 to +70	°C
Storage Temperature	T_{STG}		-65 to +150	°C

Recommend Operating Conditions

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Power Supply Voltage	V_{DD}		3.0	3.3	3.6	V
High-Level Input Voltage	V_{IH}	TTL Interface	2.0	-	V_{DD}	V
Low-Level Input Voltage	V_{IL}	TTL Interface	0.0	-	0.8	V
Positive Trigger Voltage	V_P		1.5	-	2.7	V
Negative Trigger Voltage	V_N		0.6	-	1.4	V
Hysteresis Voltage	V_H		1.1	-	1.5	V
Input Rise Time	t_{ri}	Normal Input	0	-	200	ns
Input Fall Time	t_{fi}	Normal Input	0	-	200	ns

DC Characteristics

V_{DD} = 3.3V ±0.3V; T_A = 0 to +70°C

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Static Current Consumption	I_{DDS}	VI = V_{DD} or GND		10	200	mA
Input Leakage Current	I_I	VI = V_{DD} or GND		$\pm10^{-4}$	±10	µA
Low-Level Output Current	I_{OL}	VOL = 0.4V	12.0	-	-	mA
High-Level Output Current	I_{OH}	VOH = 2.4V	-2.0	-	-	mA
Low-Level Output Voltage	V_{OL}	IOL = 0 mA	-	-	0.1	V
High-Level Output Voltage	V_{OH}	IOH = 0 mA	VDD - 0.1	-	-	V
Off-State Output Current	I_{OZ}	VO = VDD or GND	-	-	±10	µA
Output Short-Circuit Current	I_{OS}	VO = GND	-	-	-250	mA

Capacitance

T_A = +25°C; f =1Mhz

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Capacitance	C_I		4.0		6.4	pF
Output Capacitance	C_O		4.0		6.0	pF
I/O Capacitance	C_{IO}		4.0		6.0	pF

Operating Current

V_{DD} = 3.3V ± 0.3V; T_A = 0 to +70°C

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Operating Current	I_{CC}	CK_IN @ 90 MHz CK_OUT @ 90 MHz CK_V @ 88 MHz			9.10	mA

AC Characteristics

V_{DD} = 3.3V ± 0.3V; T_A = 0 to +70°C

SIGNAL NAME	SETUP		HOLD		REFERENCE CLOCK	UNITS
	MIN	MAX	MIN	MAX		
YIN[9:0]	2	-	1	-	CK_IN	ns
CIN[9:0]	2	-	1	-	CK_IN	ns
FILM_FR	-	-	2	-	CK_IN	ns
SIF_IN	1	-	2	-	SIF_CK	ns
SIF_RST	1	-	2	-	SIF_CK	ns
OUT_FRST	1	-	2	-	CK_OUT	ns
DATA_A	2	-	0	-	CK_A	ns
DATA_B	2	-	0	-	CK_B	ns
DATA_C	2	-	0	-	CK_C	ns
DATA_D	2	-	0	-	CK_D	ns
Signal Name			Pulse Width			
			Min		Max	
RST			110 *			µs

NOTE: * The minimum pulse width is for 64Mb SDRAMs. If 16Mb is used them 10µs width can be used.

Output Signal Timing Specifications

SIGNAL NAME	CLK TO VALID OUTPUT DELAY		REFERENCE CLOCK
	Min	Max	
GOUT[9:0]	0.15 ns	3 ns	OUT_CK*
BOUT[9:0]	0.15 ns	3 ns	OUT_CK*
ROUT[9:0]	0.15 ns	3 ns	OUT_CK*
ADDR_A, RAS_A, CAS_A, WE_A, CKEN_A, DATA_A	1.25 ns	6 ns	CK_A
ADDR_B, RAS_B, CAS_B, WE_B, CKEN_B, DATA_B	1.25 ns	6 ns	CK_B
ADDR_C, RAS_C, CAS_C, WE_C, CKEN_C, DATA_C	1.25 ns	6 ns	CK_C
ADDR_D, RAS_D, CAS_D, WE_D, CKEN_D, DATA_D	1.25 ns	6 ns	CK_D

NOTE: * CK_OUT to OUT_CK delay is 1.81(min); 3.97(max)

Clock Frequency

CLOCK NAME	FREQUENCY	
	Min	Max
CK_IN	1 MHz	90 MHz
CK_V	1 MHz	88 MHz
CK_OUT	1 MHz	90 MHz
SIF_CK	-	90 MHz

2. DEVICE OVERVIEW

A system level block diagram is shown on page 1.

2D scaling is performed by cascading two 1D-scaling filters.

If the number of horizontal input samples is greater than the number of horizontal output samples (i.e. down sampling), then it is advantageous to perform horizontal resizing first. Otherwise, horizontal resizing is performed last. This minimizes the number of operations required and minimizes the intermediate image size. External SDRAMs are used for field/frame buffering and transposing the video data.

In addition, the SDRAMs are used for field merge or separation operations to perform simple frame rate conversions (e.g. 30 ↔ 60 and 48 ↔ 60) for film applications. This minimizes the on chip memory required to perform 2D format conversion and by using commodity SDRAM parts provides a low-cost high-quality format conversion solution.

Dependant upon the conversion mode, the GF9320 has 2 fields/frames of delay.

Input processing, vertical processing, and output processing perform simultaneous operation on 3 fields/frames of video data.

Input processing is performed on field/frame N, vertical processing is performed on field/frame (N-1) and output processing is performed on field/frame (N-2).

The input processor decodes the input TRS to determine input video timing information. An area of the input video is selected according to the downloaded parameters. The input video is resized horizontally if down sampling is indicated.

The video is passed to picture memory control #1 and stored in SDRAM. Field/frame (N-1) is read out of picture memory #1, processed vertically, and stored in picture memory #2. In order to process the video vertically the read address to picture memory #1 transposes the video data while the write address to picture memory #2 transposes the video data back. This transpose operation allows the vertical processing to be done as rows instead of columns.

Field/frame (N-2) is read out of picture memory #2 and resized horizontally if up sampling is indicated.

The output processor can be selected to perform colour difference over sampling, matrix to RGB, colour background insertion and output TRS insertion.

3. SERIAL INTERFACE CONTROL

The serial interface download control parameters are grouped into 5 sets as given in Table 1. All parameters may be downloaded at once or each set can be downloaded individually.

This grouping allows for quick downloading of dynamic parameters (e.g. zoom, pan, gain, etc.) and only requires that the static parameters be downloaded once.

The GF9320 parameters are downloaded using a 3-pin serial interface. The serial interface consists of a clock, data and a reset as shown in Figure 3. The serial interface reset (SIF_RST) is provided to re-synchronise the download operation in the event that it is interrupted.

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TABLE 1: Serial Interface Download Groups

NAME	CMD ID	No. OF BYTES	NUMBER OF BITS	DESCRIPTION	WORD
All Parameters[1]	0 00000000^2	147	1176	A download of all parameters	AP[1175:0]
I/O Format Parameters	1 00100000^2	11	7+14+66+1 (fill) =88	Input and Static Output Parameters These parameters tend to remain fixed once the input and output format is selected	IO[87:0]
Scaling Parameters	2 01000000^2	19	149+3 (fill) = 152	Resizing Parameters These parameters change with zoom, pan, and crop controls	RS[151:0]
Dynamic Output Parameters	3 01100000^2	20	157 +3 (fill) = 160	Dynamic Output Parameters These parameters change with gain, H position, line advance, etc. controls	OD[159:0]
Horizontal Filter Coefficients	4 10000000^2	43	344+0 (fill) = 344	Horizontal filter	HF[343:0]
Vertical Filter Coefficients	5 10100000^2	54	428+ 4 (fill) =432	Vertical filter	VF[431:0]

NOTES:

1 The GF9320 download parameters are grouped into 5 sets.

2 Each group will be extended with zeros to make an integer number of bytes. In each group the LSB is sent first. So, for instance, the I/O format parameter group sends 1 zero fo-llowed by the PROC_8_BITS bit followed by the OUT_8_BITS bit. A download of all parameters (CMD ID = 0) sends the word:

AP[1175:0] = IO[87:0] I RS[151:0] I OD[159:0] I HF[343:0] I VF[431:0]

where "I" represents concatenation

As with all other words the LSB of AP[1175:0] is sent first. The CMD_ID word is listed above in binary form from MSB to LSB. As with all other words the CMD_ID is sent LSB first. So, a download of the dynamic output parameters (CMD_ID=3) sends 5 zeros followed by 2 ones followed by 1 zero followed by OD0 followed by OD1 followed by OD2....OD159.

Note that all CMD_IDs have 5 zeros as the 5 least significant bits so that each download command starts with 5 zeros.

TABLE 2: Serial Interface Download Parameters

PARAMETER NAME	No. OF BITS	DESCRIPTION	WORD POSITION	USED BY	TIME FRAME
I/O FORMAT PARAMETERS	88 TOTAL				
INPUT FORMAT PARAMETERS	7 SUB-TOTAL				
IN_PROGRESSIVE	1	Indicates that the input is progressive 0 - Interlaced 1 - Progressive	IO[87]	INPUT CONTROL	0
IN_TOP_ACT_FLD	1	Used for interlaced formats only. Indicates which field contains the first active line in a frame (i.e. which field is on top) 0 - Field 0 is on top 1 - Field 1 is on top	IO[86]	INPUT CONTROL	0
IN_TOP_ACT_LONGER	1	Used for interlaced formats only. Indicates if the top field is one line longer than the bottom field 0 - Top and Bottom fields contain the same number of active lines 1 - Top field has one more active line	IO[85]	INPUT CONTROL	0
IN_YC_MUXED	1	Indicates if the input bus is one 10-bit bus for muxed Y&C data 0 - Two 10-bit buses for Y and C_bC_r 1 - Y & C Muxed data on a 10-bit bus	IO[84]	INPUT CONTROL	0
IN_FILM_RATE	2	Input film frame rate. Used for film inputs only 00 - Input is from film with 3:2 pull-down 01 - Input is from film with 2:2 pull-down 10 - Input is at film rate (24/25 Hz) 11 - Not from film	IO[83:82]	INPUT CONTROL	0
IN_REFR_LEFT	1	This indicates a left memory array refresh is required and normally indicates that the input is from film 0 - No refresh 1 - Refresh	IO[81]	MEMORY CONTROL	0
MEMORY CONFIGURATION	14 SUB-TOTAL				
MEM_CONFIG_LEFT	2	Indicates the number of SDRAMs in left bank excluding chips needed for LSBs if necessary (i.e. 8-bit processing) 00 - 4 chips 01 - 3 chips 10 - 2 chips 11 - 1 chip	IO[80:79]	MEMORY CONTROL	0

TABLE 2: Serial Interface Download Parameters [continued]

PARAMETER NAME	No. OF BITS	DESCRIPTION	WORD POSITION	USED BY	TIME FRAME
MODE_16_LEFT	1	Maximum number of left bank SDRAM memory rows used to store a horizontal active line. 0 - 8 memory rows 1 - 16 memory rows	IO[78]	MEMORY CONTROL	0
MEM_CONFIG_RIGHT	2	Indicates the number of SDRAMs in right bank excluding chips needed for LSBs if necessary (i.e. 8 bit processing) 00 - 4 chips 01 - 3 chips 10 - 2 chips 11 - 1 chip	IO[77:76]	MEMORY CONTROL	0
MODE_16_RIGHT	1	Maximum number of right bank SDRAM memory rows used to store a horizontal active line 0 - 8 memory rows 1 - 16 memory rows	IO[75]	MEMORY CONTROL	0
PIX2READ	7	Number of pixels to be pre-read. Vertical processing requires pre-reading samples so that no hits occur while processing a column of data	IO[74:68]	MEMORY CONTROL	0
OUT_REFR_RIGHT	1	This indicates a right memory array refresh is required and normally indicates that the input is from film 0 - No refresh 1 - Refresh	IO[67]	MEMORY CONTROL	0
STATIC OUTPUT FORMAT PARAMETERS	67 SUB-TOTAL				
OUT_HLEN_TOT	12	The total number of samples per line (e.g. 2200)	IO[66:55]	OUTPUT TIMING	0
OUT_VLEN_TOT	12	The total number of output lines in a frame (e.g. 1125)	IO[54:43]	OUTPUT TIMING	0
OUT_HLEN_ACT	11	The number of active samples per line minus 1 (e.g. 1919 implies 1920 active samples)	IO[42:32]	OUTPUT TIMING	0
OUT_VLEN_ACT	11	The number of active output lines minus 1 (e.g. 1079 implies 1080 active lines)	IO[31:21]	OUTPUT TIMING	0
OUT_PROGRESSIVE	1	Indicates that the output is progressive 0 - Interlaced 1 - Progressive	IO[20]	OUTPUT TIMING/ INPUT CONTROL	0
OUT_TOP_ACT_FLD	1	Used for interlaced formats only. Indicates which field contains the first active line in a frame (i.e. which field is on top) 0 - Field 0 is on top 1 - Field 1 is on top	IO[19]	OUTPUT TIMING	0

TABLE 2: Serial Interface Download Parameters [continued]

PARAMETER NAME	No. OF BITS	DESCRIPTION	WORD POSITION	USED BY	TIME FRAME
OUT_TOP_ACT_LONGER	1	Used for interlaced formats only. Indicates if the top field is one line longer than the bottom field 0 - Both fields have the same number of active lines 1 - Top field has one more active line	IO[18]	OUTPUT TIMING	0
OUT_VACT_POS	8	The position of the first active output line relative to the start of the frame. For interlaced inputs this implies field 0	IO[17:10]	OUTPUT TIMING	0
OUT_FLD_LONGER	1	For interlaced formats only. Indicates which field is longer. Interlaced formats contain an odd number of lines. So one field contains more lines 0 - Field 0 is longer 1 - Field 1 is longer	IO[9]	OUTPUT TIMING	0
OUT_REF	1	0 - Input TRS 1 - Output Reset pin on GF9320 (OUT_FRST)	IO[8]	OUTPUT TIMING	0
OUT_FILM_RATE	2	Output film frame rate 00 - Output has a 3:2 pull-down sequence 01 - Output has a 2:2 pull-down sequence 10 - Output is at a film rate (24/25 Hz) 11 - Output is not to a film rate or sequence	IO[7:6]	OUTPUT TIMING/ INPUT CONTROL	0
OUT_MODE	2	Indicates output port configuration 00 - 4:4:4 GBR Triple output 01 - 4:4:4 YC_bC_r Triple output 10 - 4:2:2 YC_bC_r Muxed single output 11 - 4:2:2 YC_bC_r Muxed dual output	IO[5:4]	OUTPUT	0
OUT_TRS_ON	1	Indicates if TRS is inserted into the output 0 - TRS not inserted 1 - TRS inserted	IO[3]	OUTPUT	0
OUT_8_BITS	1	Indicates that the output is rounded to 8 bits 0 - 10-bit output 1 - 8-bit output	IO[2]	OUTPUT	0
PROC_8_BITS	1	Indicates that H&V processing is rounded to 8-bits 0 - 10-bit processing (Requires LSB memory) 1 - 8-bit processing	IO[1]	INT. FILTERS	0
IO_FILL	1	Not used	IO[0]		

TABLE 2: Serial Interface Download Parameters [continued]

PARAMETER NAME	No. OF BITS	DESCRIPTION	WORD POSITION	USED BY	TIME FRAME
RESIZING PARAMETERS	152 TOTAL				
H_PROC_FIRST	1	Indicates horizontal processing is performed first 0 - Horizontal processing last (H_ZOOM_RATIO < 524288) 1 - Horizontal processing first (H_ZOOM_RATIO >= 524288)	RS[151]	GLUE LOGIC (MUX)/ MEM CONTROL	1 2
H_FLT_DEC	1	Horizontal filter decimate 0 - Non-decimate mode 1 - Decimate mode	RS[150]	H CONTROL/ HBL FILTER	1/3 1/3
H_ZOOM_RATIO	22	Horizontal zoom ratio H_ZOOM_FACTOR = H_ZOOM_RATIO/ (4096*128)	RS[149:128]	H CONTROL	1/3
IN_HSTART_PHASE	7	Indicates the starting horizontal phase to be used for resampling	RS[127:121]	H CONTROL	1/3
IN_HSTART	11	Indicates the first sample to be used for resampling	RS[120:110]	INPUT TIMING/H CONTROL/ MEM CONTROL	1 1/3 2
IN_HSTOP	11	Indicates the last sample to be used for resampling	RS[109:99]	INPUT TIMING/H CONTROL/ MEM CONTROL	1 1/3 2
OUT_HSTART	11	Indicates the placement of the first output sample with live data. This value must be even.	RS[98:88]	OUTPUT TIMING/H CONTROL/ MEM CONTROL	3 1/3 2
OUT_HSTOP	11	Indicates the placement of the last output sample with live data. This value must be odd	RS[87:77]	OUTPUT TIMING/H CONTROL/ MEM CONTROL	3 1/3 2
V_FLT_DEC	1	Vertical filter decimate 0 - Non-decimate mode 1 - Decimate mode	RS[76]	VBL FILTER	2
V_ZOOM_RATIO	22	Vertical zoom ratio V_ZOOM_FACTOR = V_ZOOM_RATIO/ (4096*128)	RS[75:54]	V CONTROL	2
IN_VSTART_PHASE	7	Indicates the starting vertical phase to be used for resampling	RS[53:47]	V CONTROL	2
IN_VSTART	11	Indicates the first line to be used for resampling	RS[46:36]	INPUT TIMING/V CONTROL	1 2

TABLE 2: Serial Interface Download Parameters [continued]

PARAMETER NAME	No. OF BITS	DESCRIPTION	WORD POSITION	USED BY	TIME FRAME
IN_VSTOP	11	Indicates the last line to be used for resampling	RS[35:25]	INPUT TIMING/V CONTROL	1 2
OUT_VSTART	11	Indicates the placement of the first output line with live data	RS[24:14]	OUTPUT TIMING/V CONTROL	3 2
OUT_VSTOP	11	Indicates the placement of the last output line with live data	RS[13:3]	OUTPUT TIMING/V CONTROL	3 2
RS_FILL	3	Not Used.	RS[2:0]		
DYNAMIC OUTPUT PARAMTERS[1]	160 TOTAL				
MATRIX COEFFICIENTS		The matrix coefficient format is ±2.10 i.e. 1 sign bit, 2 integer bits and 10 fractional bits			
G1	13	Matrix coefficient $G = G1*Y + G2*C_b + G3*C_r$	OD[159:147]	OUTPUT	1
G2	13	Matrix coefficient $G = G1*Y + G2*C_b + G3*C_r$	OD[146:134]	OUTPUT	1
G3	13	Matrix coefficient. $G = G1*Y + G2*C_b + G3*C_r$	OD[133:121]	OUTPUT	1
B1	13	Matrix coefficient $B = B1*Y + B2*C_b + B3*C_r$	OD[120:108]	OUTPUT	1
B2	13	Matrix coefficient $B = B1*Y + B2*C_b + B3*C_r$	OD[107:95]	OUTPUT	1
B3	13	Matrix coefficient $B = B1*Y + B2*C_b + B3*C_r$	OD[94:82]	OUTPUT	1
R1	13	Matrix coefficient $R = R1*Y + R2*C_b + R3*C_r$	OD[81:69]	OUTPUT	1
R2	13	Matrix coefficient $R = R1*Y + R2*C_b + R3*C_r$	OD[68:56]	OUTPUT	1
R3	13	Matrix coefficient $R = R1*Y + R2*C_b + R3*C_r$	OD[55:43]	OUTPUT	1
BACKGROUND COLOUR					
Y_BKGD	8	Background colour for Y Unsigned integer	OD[42:35]	OUTPUT	1
CB_BKGD	8	Background colour for C_b Signed integer	OD[34:27]	OUTPUT	1
CR_BKGD	8	Background colour for C_r Signed integer	OD[26:19]	OUTPUT	1

TABLE 2: Serial Interface Download Parameters [continued]

PARAMETER NAME	No. OF BITS	DESCRIPTION	WORD POSITION	USED BY	TIME FRAME
OUTPUT TIMING					
LINE_ADV	4	Line advance with respect to input timing	OD[18:15]	OUTPUT TIMING	0'
H_POS	12	Horizontal position with respect to input timing	OD[14:3]	OUTPUT TIMING	0'
OD_FILL	3	Not Used	OD[2:0]		
FILTER COEFFICIENTS	776 TOTAL				
HORIZONTAL FILTER	344 SUB-TOTAL				
H_Y_FLT_COEF HYBANK: 12|12|11|10|10|9|9|9|9|8|8 = 107 2 filters * (107 bits) = 214	214	Horizontal Y Filter coefficients Center Coefficient is ±1.10 i.e. 1 sign bit, 1 integer bit and 10 fractional bits	HY[343:130] (See Note 2)	H Y FILTER	1
H_C_FLT_COEF HCBANK: 12|11|9|9|8|8|8 = 65 2 filters * (65 bits) = 130	130	Horizontal C Filter coefficients Center Coefficient is ±1.10 i.e. 1 sign bit, 1 integer bit and 10 fractional bits	HY[129:0] (See Note 2)	H C FILTER	1
VERTICAL FILTER	432 SUB-TOTAL				
V_Y_FLT_COEF HYBANK: 12|12|11|10|10|9|9|9|9|8|8 = 107 2 filters * (107 bits) = 214	214	Vertical Y Filter coefficients Center Coefficient is ±1.10 i.e. 1 sign bit, 1 integer bit and 10 fractional bits	VY[431:218] (See Note 3)	V Y FILTER	1
V_C_FLT_COEF HCBANK: 12|12|11|10|10|9|9|9|9|8|8 = 107 2 filters * (107 bits) = 214	214	Vertical C Filter coefficients Center Coefficient is ±1.10 i.e. 1 sign bit, 1 integer bit and 10 fractional bits	VY[217:4] (See Note 3)	V C FILTER	1
VYF_FILL	4	Not Used	VY[3:0]		

NOTES:

1. The resizing parameters, dynamic output parameters, and the filter coefficients are adjustable (dynamic). The I/O Format parameters are static, i.e. once an input and output format is selected the I/O format parameters tend to remain fixed.

2. Horizontal coefficient download format:

HF[343:0] = HYBANK1[106:0] | HYBANK0[106:0] | HCBANK1[64:0] | HCBANK0[64:0]

2.1 In non-decimate mode (H_FLT_DEC = 0):

HYBANK0 contains the coefficients for a 21-tap symmetric FIR filter and HCBANK0 contains the coefficients for a 13-tap symmetric FIR filter. HYBANK1 and HCBANK1 are not used when H_FLT_DEC is 0 and should contain 0's.

HYBANK0[106:0] = HYT0[11:0] | HYT1[11:0] | HYT2[10:0] | HYT3[9:0] | HYT4[9:0] | HYT5[8:0] | HYT6[8:0] | HYT7[8:0] | HYT8[8:0] | HYT9[7:0] | HYT10[7:0]

HYBANK1[106:0] = 0

HCBANK0[64:0] = HCT0[11:0] | HCT1[10:0] | HCT2[8:0] | HCT3[8:0] | HCT4[7:0] | HCT5[7:0] | HCT6[7:0]

HCBANK1[64:0] = 0

2.2 In decimate mode (H_FLT_DEC = 1):

HYBANK0 and HYBANK1 contain the coefficients for a 41-tap symmetric decimation filter while HCBANK0 and HCBANK1 contain the coefficients for a 25-tap symmetric decimation filter. BANK0's contain the center tap (tap 0) and all odd taps (e.g. 1, 3, 5....) while the BANK1's contain a zero and all even taps (e.g. 2, 4, 6....).

HYBANK0[106:0] = HYT0[11:0] | HYT1[11:0] | HYT3[10:0] | HYT5[9:0] | HYT7[9:0] | HYT9[8:0] | HYT11[8:0] | HYT13[8:0] | HYT15[8:0] | HYT17[7:0] | HYT19[7:0]

HYBANK1[106:0] = "000000000000" | HYT2[11:0] | HYT4[10:0] | HYT6[9:0] | HYT8[9:0] | HYT10[8:0] | HYT12[8:0] | HYT14[8:0] | HYT16[8:0] | HYT18[7:0] | HYT20[7:0]

HCBANK0[64:0] = HCT0[11:0] | HCT1[10:0] | HCT3[8:0] | HCT5[8:0] | HCT7[7:0] | HCT9[7:0] | HCT11[7:0]

HCBANK1[64:0] = "000000000000" | HCT2[10:0] | HCT4[8:0] | HCT6[8:0] | HCT8[7:0] | HCT10[7:0] | HCT12[7:0]

Further information on the horizontal filter coefficients is given in FIR Filter Parameters (section 5.2.2).

3. Vertical coefficient download format:

VF[431:0] = VYBANK1[106:0] | VYBANK0[106:0] | VCBANK1[106:0] | VCBANK0[106:0] | "0000"

3.1 In non-decimate mode (V_FLT_DEC = 0):

VYBANK0 and VCBANK0 both contain the coefficients for a 21-tap symmetric FIR filter. VYBANK1 and VCBANK1 are not used when V_FLT_DEC is 0 and should contain 0's.

VYBANK0[106:0] = VYT0[11:0] | VYT1[11:0] | VYT2[10:0] | VYT3[9:0] | VYT4[9:0] | VYT5[8:0] | VYT6[8:0] | VYT7[8:0] | VYT8[8:0] | VYT9[7:0] | VYT10[7:0]

VYBANK1[106:0] = 0

VCBANK0[106:0] = VCT0[11:0] | VCT1[11:0] | VCT2[10:0] | VCT3[9:0] | VCT4[9:0] | VCT5[8:0] | VCT6[8:0] | VCT7[8:0] | VCT8[8:0] | VCT9[7:0] | VCT10[7:0]

VCBANK1[106:0] = 0

3.2 In decimate mode (V_FLT_DEC = 1):

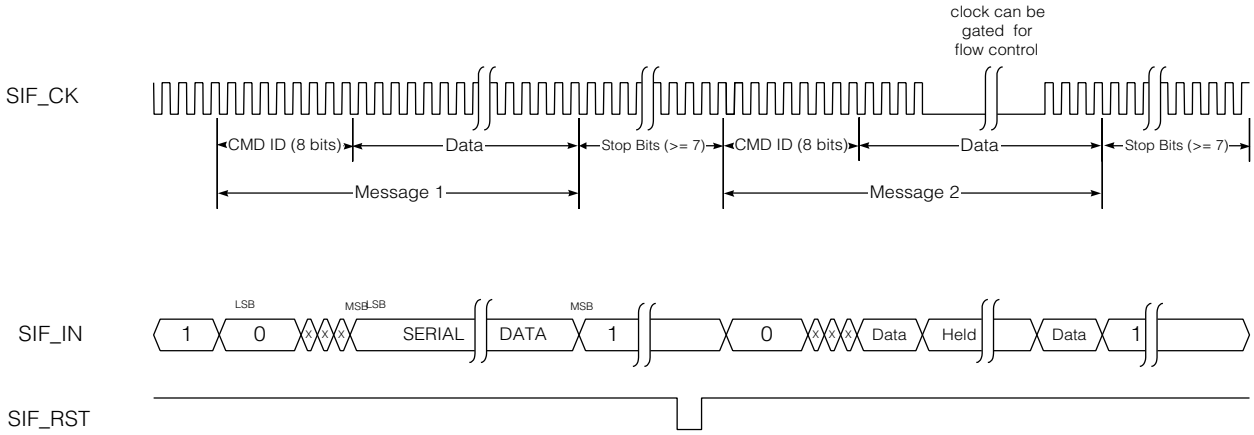
VYBANK0 and VYBANK1 together contain the coefficients for a 41-tap symmetric decimation filter while VCBANK0 and VCBANK1 together also contain the coefficients for a 41-tap symmetric decimation filter. BANK0's contain the center tap (tap 0) and all odd taps (e.g. 1, 3, 5....19) while the BANK1's contain a zero and all even taps (e.g. 2, 4, 6....20).

VYBANK0[106:0] = VYT0[11:0] | VYT1[11:0] | VYT3[10:0] | VYT5[9:0] | VYT7[9:0] | VYT9[8:0] | VYT11[8:0] | VYT13[8:0] | VYT15[8:0] | VYT17[7:0] | VYT19[7:0]

VYBANK1[106:0] = "000000000000" | VYT2[11:0] | VYT4[10:0] | VYT6[9:0] | VYT8[9:0] | VYT10[8:0] | VYT12[8:0] | VYT14[8:0] | VYT16[8:0] | VYT18[7:0] | VYT20[7:0]

VCBANK0[106:0] = VCT0[11:0] | VCT1[11:0] | VCT3[10:0] | VCT5[9:0] | VCT7[9:0] | VCT9[8:0] | VCT11[8:0] | VCT13[8:0] | VCT15[8:0] | VCT17[7:0] | VCT19[7:0]

VCBANK1[106:0] = "000000000000" | VCT2[11:0] | VCT4[10:0] | VCT6[9:0] | VCT8[9:0] | VCT10[8:0] | VCT12[8:0] | VCT14[8:0] | VCT16[8:0] | VCT18[7:0] | VCT20[7:0]



NOTES:
1) SIF_IN: Serial Data Input. Must be held high (logic 1) if no message is being sent and SIF_CLK is running. First byte sent is the CMD_ID. All data including CMD_ID is sent LSB first. Valid choices for CMD_ID are:
LSB ... MSB
01234567
0 (00000000) : A download of all parameters (1176 data bits)
1 (00000100): A download of the I/O parameters (88 data bits)
2 (00000010): A download of the resizing parameters (152 data bits)
3 (00000110): A download of the Dynamic Output parameters (160 data bits)
4 (00000001): A download of the Horizontal Filter coefficients (344 data bits)
5 (00000101): A download of the Vertical Filter coefficients (432 data bits)

2) SIF_CK: Serial Clock. All data from SIF_IN is clocked on the positive edge of SIF_CK. SIF_CK may be held low to pause transmission (i.e. implement flow control).

3) SIF_RST: Message Reset. Active low and asynchronous. Used to recover from a transmission error or message abort. Can be asserted between each message to ensure correct initialization of the download, but is not necessary in general as long as the correct message format (as indicated above) is followed.

Fig. 3 Serial Interface Download Signal Specification

4. INPUT PROCESSING

The input processor decodes the input TRS from the luminance data input. This provides input video timing information to the GF9320. An area of the input video data is selected for scaling according to the downloaded parameters (i.e. IN_HSTART, IN_HSTOP, IN_VSTART, and IN_VSTOP). This operation is called the windowing operation. Based on the input field/frame timing and the I/O format parameters a memory enable signal is generated by the input controller. This signal controls the field/frame switching of the SDRAM memory controller. Also, a frame-reset signal is sent to the output controller for use in internal lock mode (OUT_REF=0). The frame reset signal and the field/frame switch point is based on input TRS F-bit in interlaced modes (non-film). Otherwise, (i.e. progressive and all film modes) the frame reset signal and the field/frame switch point is based on one line after input TRS V-bit. Note that in film modes the frame reset signal and field/frame switch point vary according the input and output frame rates.

5. SCALING PROCESSOR

At the heart of the GF9320 is the scaling processor. It is here where the raw input image selected from the input video is translated into a raw output image of selected size according to user controlled scaling parameters. As described in Section 2, general 2D scaling is performed by cascading two 1D-scaling filters. This section describes both the horizontal and vertical scaling filters. A block diagram of the horizontal resizing filter is shown in Figure 4. A block diagram of the vertical resizing filter is shown Figure 5.

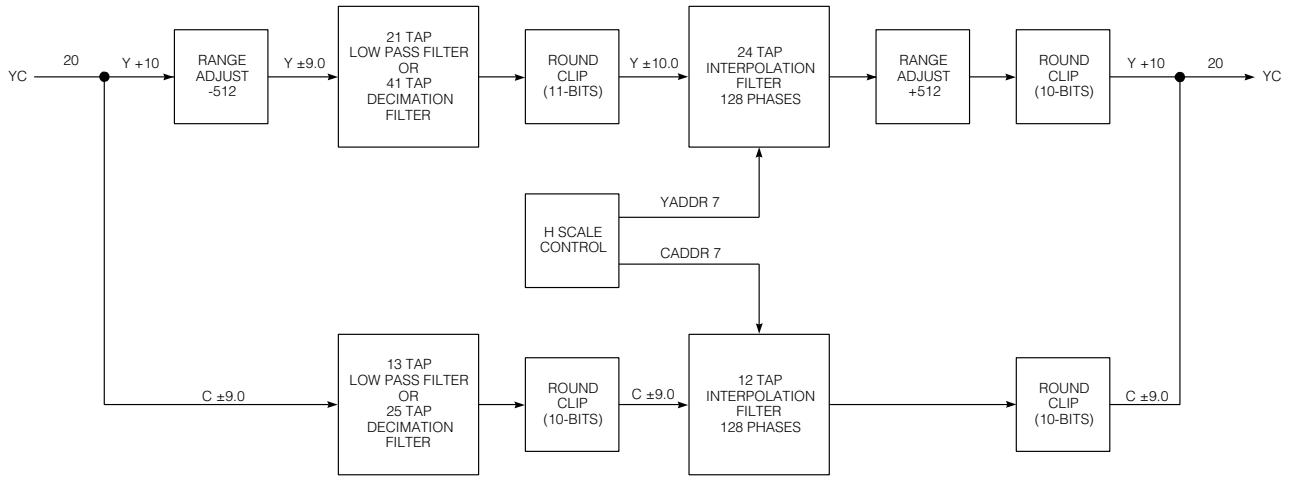


Fig. 4 Horizontal Scaling Filter

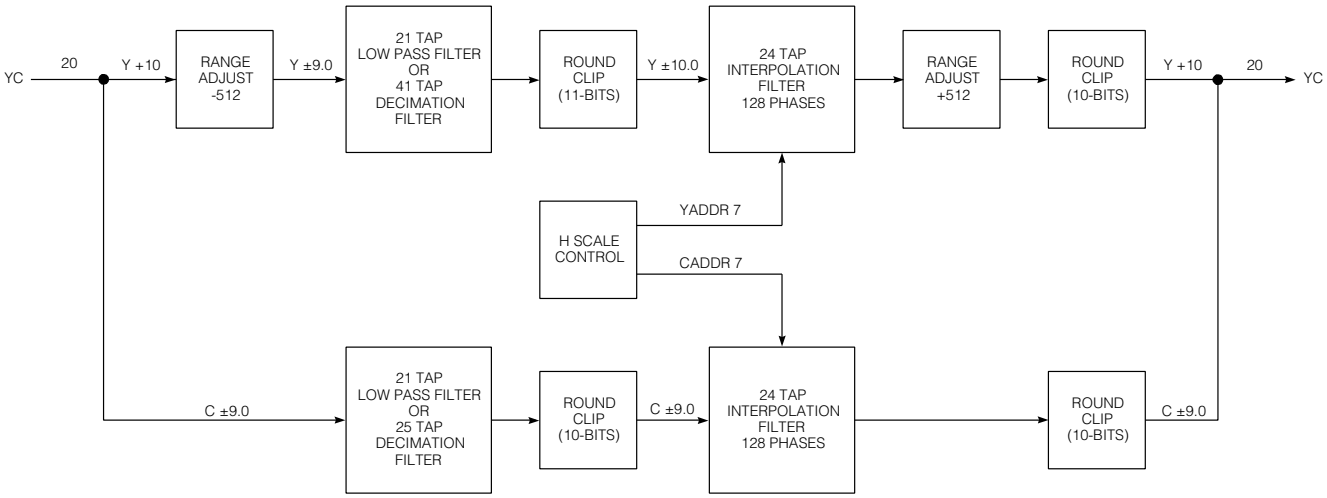


Fig. 5 Vertical Scaling Filter

5.1 SCALER PROCESSING

General 1D scaling is performed by cascading an FIR filter with an interpolation filter. The FIR filter is needed to band limit the input signal when the output Nyquist frequency is less than the input Nyquist frequency. The interpolation filter is used to resample the input signal to the new output rate.

5.1.1 FIR Filter

The purpose of the FIR filters is to band limit or shape the input signal. Each filter is user programmable, with the coefficients derived depending on the required frequency response. The FIR filter can be used in one of two modes:

1. Non-decimate mode

2. Decimate mode

Decimate mode can be used when the output rate is half the input rate. The advantage to using decimate mode is that the number of taps is approximately doubled by using two input clocks to compute one output sample. In non-decimate mode the filter is 21 taps (13 for horizontal colour difference due to the 4:2:2 input video structure). In decimate mode the filter is 41 taps (25 for horizontal colour difference).

The filter operation is described by:

$$HY_O(n)\cdot 1024=\begin{cases} HYT0\_0\cdot HY_I(n)+\sum_{k=1}^{k=10} HYT\langle 2k-1|k\rangle\cdot[HY_I(n-k)+HY_I(n+k)] & H\_FLT\_DEC=0 \\ HYT0\_0\cdot HY_I(n)+\sum_{k=1}^{k=10} HYT\langle 2k-1|k\rangle\cdot[HY_I(n-2k+1)+HY_I(n+2k-1)] & H\_FLT\_DEC=1 \\ \quad +\sum_{k=1}^{k=10} HYT\langle 2k\rangle\cdot[HY_I(n-2k)+HY_I(n+2k)] & \end{cases}$$

$$HC_O(n)\cdot 1024=\begin{cases} HCT0\_0\cdot HC_I(n)+\sum_{k=1}^{k=6} HCT\langle 2k-1|k\rangle\cdot[HC_I(n-k)+HC_I(n+k)] & H\_FLT\_DEC=0 \\ HCT0\_0\cdot HY_I(n)+\sum_{k=1}^{k=6} HCT\langle 2k-1|k\rangle\cdot[HC_I(n-2k+1)+HC_I(n+2k-1)] & H\_FLT\_DEC=1 \\ \quad +\sum_{k=1}^{k=6} HCT\langle 2k\rangle\times[HC_I(n-2k)+HC_I(n+2k)] & \end{cases}$$

$$VY_O(n)\cdot 1024=\begin{cases} VYT0\_0\cdot VY_I(n)+\sum_{k=1}^{k=10} VYT\langle 2k-1|k\rangle\cdot[VY_I(n-k)+VY_I(n+k)] & V\_FLT\_DEC=0 \\ VYT0\_0\cdot VY_I(n)+\sum_{k=1}^{k=10} VYT\langle 2k-1|k\rangle\cdot[VY_I(n-2k+1)+VY_I(n+2k-1)] & V\_FLT\_DEC=1 \\ \quad +\sum_{k=1}^{k=10} VYT\langle 2k\rangle\cdot[VY_I(n-2k)+VY_I(n+2k)] & \end{cases}$$

$$VC_O(n)\cdot 1024=\begin{cases} VCT0\_0\cdot VY_I(n)+\sum_{k=1}^{k=10} VCT\langle 2k-1|k\rangle\cdot[VC_I(n-k)+VC_I(n+k)] & V\_FLT\_DEC=0 \\ VCT0\_0\cdot VY_I(n)+\sum_{k=1}^{k=10} VCT\langle 2k-1|k\rangle\cdot[VC_I(n-2k+1)+VC_I(n+2k-1)] & V\_FLT\_DEC=1 \\ \quad +\sum_{k=1}^{k=10} VCT\langle 2k\rangle\cdot[VC_I(n-2k)+VC_I(n+2k)] & \end{cases}$$

where $HY_I(n)$, $HC_I(n)$, $VY_I(n)$ and $VC_I(n)$ are the FIR filter inputs, $HY_O(n)$, $HC_O(n)$, $VY_O(n)$ and $VC_O(n)$ are the FIR filter outputs, HYT, HCT, VYT, and VCT are the filter coefficients as given in Tables 3 and 4, and 1024 is the DC gain of the filter. In non-decimate mode only one bank of coefficients are used (Bank 0), but in decimate mode both banks of coefficients are used (Bank 0 and Bank 1).

5.1.2 Interpolation filter

After FIR filtering the video data is passed to the interpolation filter where the rate conversion is performed. The interpolation filter is a polyphase filter that allows the output phase to be adjusted every clock cycle. The interpolation filter contains 128 phases (64 phases for horizontal colour difference). The phase selection allows generation of an output anywhere between two inputs with 1/128 input pixel resolution (1/64 for horizontal colour difference). The scaling control unit takes as input the scaling ratio (input/output), and starting phase (starting position of the first output pixel with respect to the input). With these parameters, the scaling control chooses the correct phasing sequence for the interpolator, determines which input samples should be held and for how long (up sampling), which interpolator outputs should be discarded (down sampling), and generates the new output.

5.2 RESIZING PARAMETERS

In order to understand how to program the GF9320 to perform the necessary conversions an explanation of the window parameters, the zoom parameters and the filter parameters is necessary.

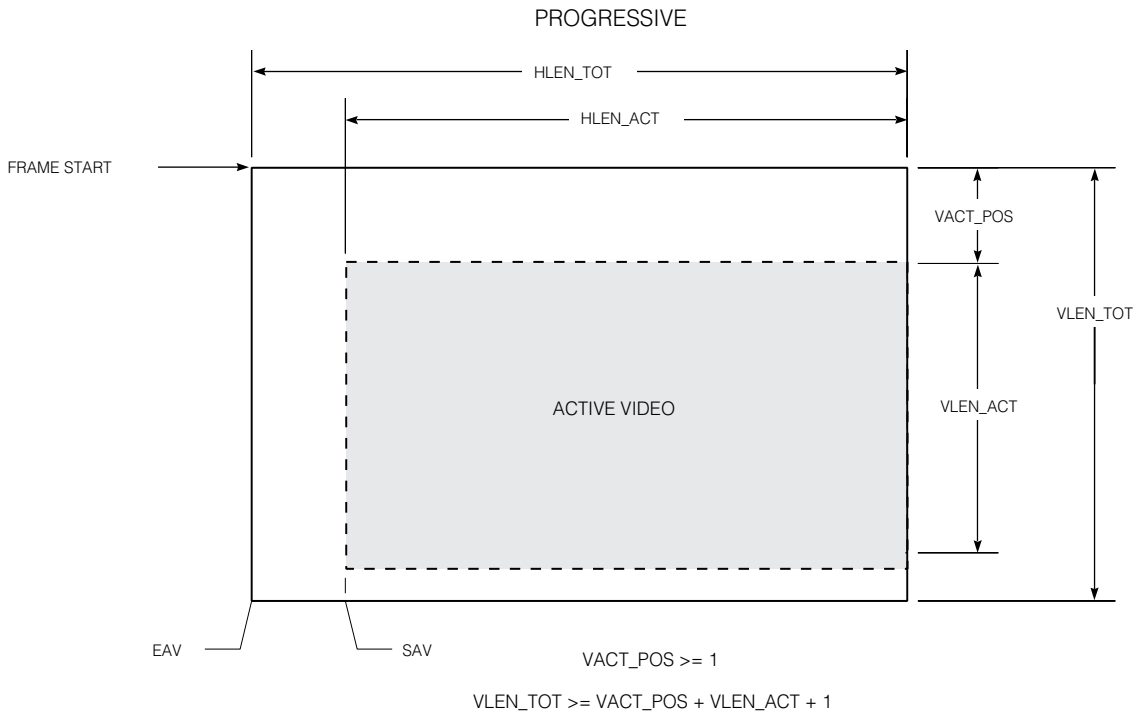


Fig. 6 Input WIndow Definition - Progressive

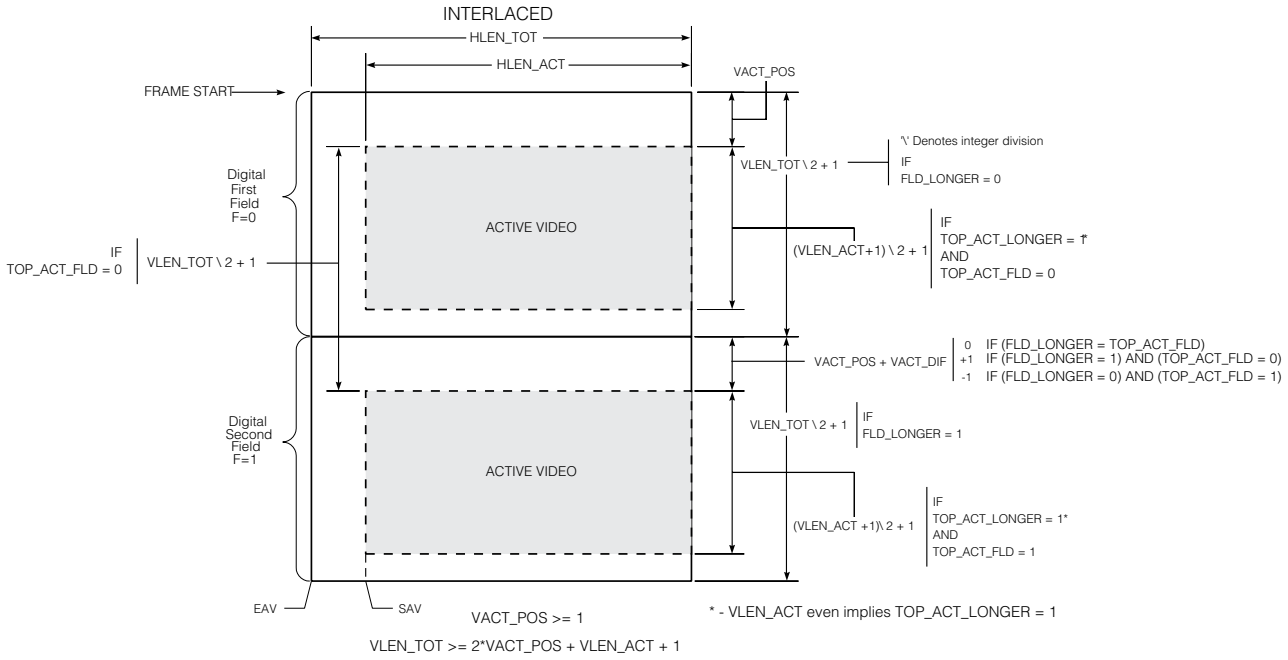


Fig. 7 Input Window Definition - Interlaced

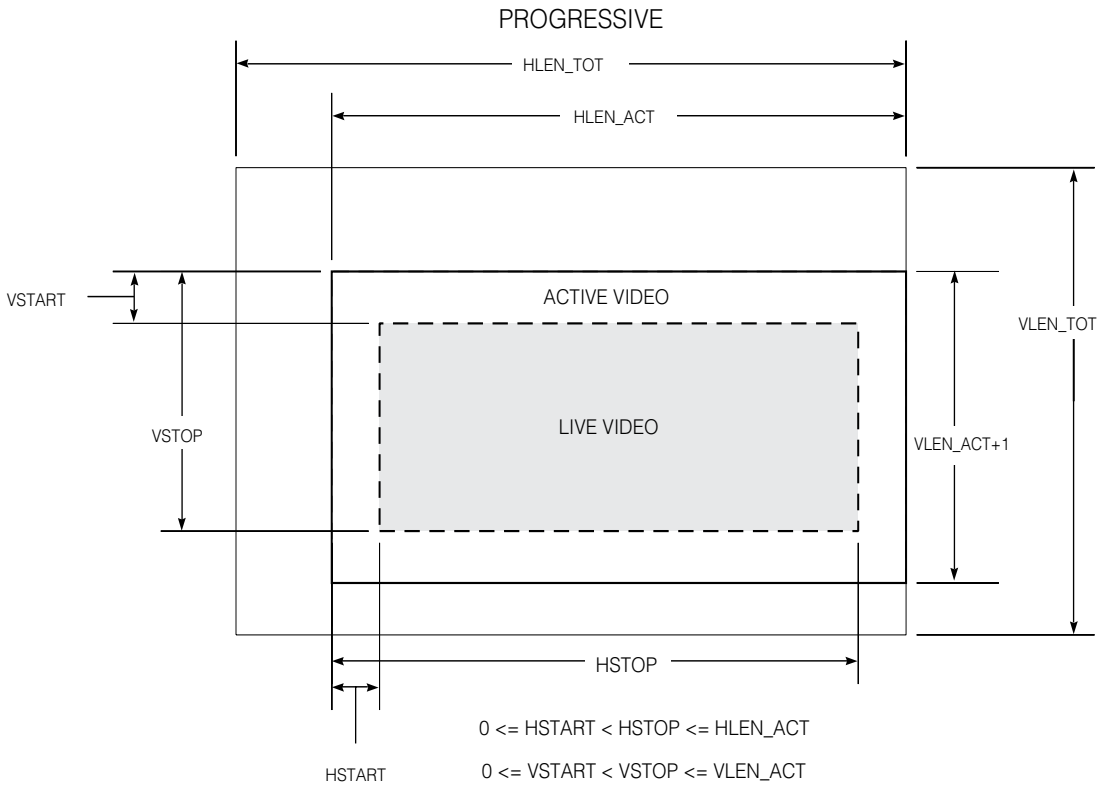


Fig. 8 Output Window Definition - Progressive

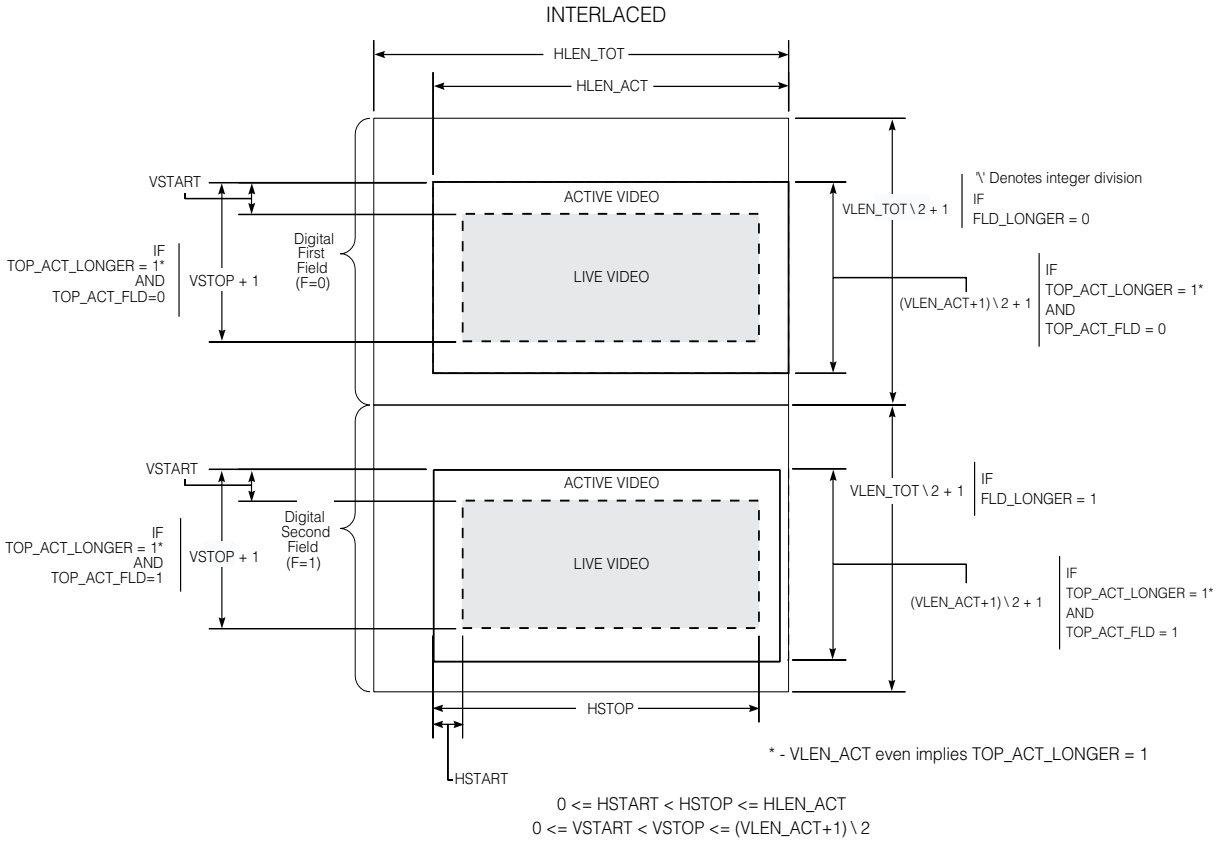


Fig. 9 Output Window Definition - Interlaced

5.2.1 Window Parameters

Figures 8 and 9 show how the GF9320 places a window over the input and output active video. This window is selected by using offsets from the active video area (HSTART, HSTOP, VSTART, VSTOP). Please note that VSTART and VSTOP for interlaced video refers to field based offsets. The windowed portion is referred to as the live video and can cover the entire active video or just a portion of it. The size of the windowed portion is HLIVE by VLIVE pixels where

$$HLIVE = HSTOP - HSTART + 1$$

$$VLIVE = VSTOP - VSTART + 1$$

For interlaced video one field may have one more active line that the other. This means that VLIVE is longer for that field. Also, in interlaced film modes VSTART and VSTOP are still field-based offsets but VLIVE is frame based since the fields are merged and processed as a frame.

The input video window is determined by IN_HSTART, IN_HSTOP, IN_VSTART, and IN_VSTOP. The size of the input windowed portion is IN_HLIVE by IN_VLIVE pixels.

The output video window is determined by OUT_HSTART, OUT_HSTOP, OUT_VSTART, and OUT_VSTOP. The size of the output windowed portion is OUT_HLIVE by OUT_VLIVE pixels.

5.2.2 FIR Filter Parameters

The FIR filter shape is programmable by downloading the filter coefficients. The horizontal filter coefficients and download positions are given in Table 3. The vertical filter coefficients are given in Table 4. The overall gain of the FIR filter is 1024, but the range of coefficients is larger to permit implementation of enhancement filters. Note that the coefficients change meaning depending on the filter structure (i.e. if the filter is in decimate mode or not). The filter structure is determined by the FLT_DEC parameter. If H_FLT_DEC is 1, then the horizontal FIR filter is configured in decimate mode. If H_FLT_DEC is 0, then the horizontal FIR filter is configured in non-decimate mode. If V_FLT_DEC is 1, then the vertical FIR filter is configured in decimate mode. If V_FLT_DEC is 0, then the vertical FIR filter is configured in non-decimate mode.

TABLE: 3 Horizontal Filter Coefficients

PARAMETER	No. OF BITS	RANGE	WORD POSITION
twelve_zeros	12	[0, 0]	HF[343:332]
HYT2	12	[-2048, 2047]	HF[331:320]
HYT4	11	[-1024, 1023]	HF[319:309]
HYT6	10	[-512, 511]	HF[308:299]
HYT8	10	[-512, 511]	HF[298:289]
HYT10	9	[-256, 255]	HF[288:280]
HYT12	9	[-256, 255]	HF[279:271]
HYT14	9	[-256, 255]	HF[270:262]
HYT16	9	[-256, 255]	HF[261:253]
HYT18	8	[-128, 127]	HF[252:245]
HYT20	8	[-128, 127]	HF[244:237]
HYT0_0	12	[-2048, 2047]	HF[236:225]
HYT1_1	12	[-2048, 2047]	HF[224:213]
HYT3_2	11	[-1024, 1023]	HF[212:202]
HYT5_3	10	[-512, 511]	HF[201:192]
HYT7_4	10	[-512, 511]	HF[191:182]
HYT9_5	9	[-256, 255]	HF[181:173]
HYT11_6	9	[-256, 255]	HF[172:164]
HYT13_7	9	[-256, 255]	HF[163:155]
HYT15_8	9	[-256, 255]	HF[154:146]
HYT17_9	8	[-128, 127]	HF[145:138]
HYT19_10	8	[-128, 127]	HF[137:130]
twelve_zeros	12	[0, 0]	HF[129:118]
HCT2	11	[-1024, 1023]	HF[117:107]
HCT4	9	[-256, 255]	HF[106:98]
HCT6	9	[-256, 255]	HF[97:89]
HCT8	8	[-128, 127]	HF[88:81]
HCT10	8	[-128, 127]	HF[80:73]
HCT12	8	[-128, 127]	HF[72:65]
HCT0_0	12	[-2048, 2047]	HF[64:53]
HCT1_1	11	[-1024, 1023]	HF[52:42]
HCT3_2	9	[-256, 255]	HF[41:33]
HCT5_3	9	[-256, 255]	HF[32:24]
HCT7_4	8	[-128, 127]	HF[23:16]
HCT9_5	8	[-128, 127]	HF[15:8]
HCT11_6	8	[-128, 127]	HF[7:0]

TABLE 4: Vertical Filter Coefficients

Parameter	Number of Bits	Range	Word Position
twelve_zeros	12	[0, 0]	VF[431:420]
VYT2	12	[-2048, 2047]	VF[419:408]
VYT4	11	[-1024, 1023]	VF[407:397]
VYT6	10	[-512, 511]	VF[396:387]
VYT8	10	[-512, 511]	VF[386:377]
VYT10	9	[-256, 255]	VF[376:368]
VYT12	9	[-256, 255]	VF[367:359]
VYT14	9	[-256, 255]	VF[358:350]
VYT16	9	[-256, 255]	VF[349:341]
VYT18	8	[-128, 127]	VF[340:333]
VYT20	8	[-128, 127]	VF[332:325]
VYT0_0	12	[-2048, 2047]	VF[324:313]
VYT1_1	12	[-2048, 2047]	VF[312:301]
VYT3_2	11	[-1024, 1023]	VF[300:290]
VYT5_3	10	[-512, 511]	VF[289:280]
VYT7_4	10	[-512, 511]	VF[279:270]
VYT9_5	9	[-256, 255]	VF[269:261]
VYT11_6	9	[-256, 255]	VF[260:252]
VYT13_7	9	[-256, 255]	VF[251:243]
VYT15_8	9	[-256, 255]	VF[242:234]
VYT17_9	8	[-128, 127]	VF[233:226]
VYT19_10	8	[-128, 127]	VF[225:218]
twelve_zeros	12	[0, 0]	VF[217:206]
VCT2	12	[-2048, 2047]	VF[205:194]
VCT4	11	[-1024, 1023]	VF[193:183]
VCT6	10	[-512, 511]	VF[182:173]
VCT8	10	[-512, 511]	VF[172:163]
VCT10	9	[-256, 255]	VF[162:154]
VCT12	9	[-256, 255]	VF[153:145]
VCT14	9	[-256, 255]	VF[144:136]
VCT16	9	[-256, 255]	VF[135:127]
VCT18	8	[-128, 127]	VF[126:119]
VCT20	8	[-128, 127]	VF[118:111]
VCT0_0	12	[-2048, 2047]	VF[110:99]
VCT1_1	12	[-2048, 2047]	VF[98:87]

TABLE 4: Vertical Filter Coefficients [continued]

Parameter	Number of Bits	Range	Word Position
VCT3_2	11	[-1024, 1023]	VF[86:76]
VCT5_3	10	[-512, 511]	VF[75:66]
VCT7_4	10	[-512, 511]	VF[65:56]
VCT9_5	9	[-256, 255]	VF[55:47]
VCT11_6	9	[-256, 255]	VF[46:38]
VCT13_7	9	[-256, 255]	VF[37:29]
VCT15_8	9	[-256, 255]	VF[28:20]
VCT17_9	8	[-128, 127]	VF[19:12]
VCT19_10	8	[-128, 127]	VF[11:4]
fill	4	[0, 0]	VF[3:0]

5.2.3 Zoom Parameters

The zoom parameters (IN_HSTART_PHASE, IN_VSTART_PHASE, H_ZOOM_RATIO, and V_ZOOM_RATIO) specify the precise conversion from the input live video to the output live video. IN_HSTART_PHASE and IN_VSTART_PHASE allows for starting the interpolator with sub-pixel accuracy. This allows for maintaining the true center of picture when zooming and panning. The zoom ratio is approximately

$$H\_ZOOM\_RATIO \approx \begin{cases} \dfrac{IN\_HLIVE \cdot 524288}{OUT\_HLIVE} & H\_FLT\_DEC = 0 \\ \dfrac{IN\_HLIVE \cdot 524288 \cdot 2}{OUT\_HLIVE} & H\_FLT\_DEC = 1 \end{cases}$$

$$V\_ZOOM\_RATIO \approx \begin{cases} \dfrac{IN\_VLIVE \cdot 524288}{OUT\_VLIVE} & V\_FLT\_DEC = 0 \\ \dfrac{IN\_VLIVE \cdot 524288 \cdot 2}{OUT\_VLIVE} & V\_FLT\_DEC = 1 \end{cases}$$

The above equations hold only *approximately* because the zoom ratio must be adjusted to maintain the true center of picture.

5.3 DYNAMIC ZOOM AND PAN CONSIDERATIONS

The GF9320 is designed to perform frame accurate zooming and panning. Some of the downloaded zoom and pan parameters are used by multiple blocks within the GF9320. These blocks operate on the video data at different time frames. For instance, the input control block operates on the video data on frame/field (N) while the vertical scaling block operates on the video data on frame/field (N-1). Both these blocks need the IN_VSTART parameter. So, the IN_VSTART parameter must be used by the scaling block one field/frame later than the input block. Registering the IN_VSTART parameter on the field/frame boundary before the scaling block uses it does this.

While most dynamic zoom and pan situations are taken care of automatically by the GF9320, some dynamic zoom and pan conditions require special downloading.

5.3.1 HPROC_FIRST Switching

The H_PROC_FIRST download bit is special because it actually changes the configuration of the GF9320. In particular, changing the H_PROC_FIRST bit from 1 to 0 makes the horizontal filter switch from operating on field/frame (N) to operating on field/frame (N-2) and vice versa. Note that changing the H_PROC_FIRST bit from 1 to 0 is changing from down sampling to up sampling. In order to handle this special case smoothly, a 1:1 horizontal zoom factor must be downloaded.

The recommended sequence for switching from H_PROC_FIRST equal to 1 to 0 (i.e. down sampling to up sampling) is:

1. Keep H_PROC_FIRST equal to 1 and download H_ZOOM_RATIO equal to 524,288 (down sampling).
2. Wait at least 2 frames/fields.
3. Change H_PROC_FIRST to 0 and download H_ZOOM_RATIO equal to 524,287 (up sampling).
4. Change to the desired H_ZOOM_RATIO.

The recommended sequence for switching from H_PROC_FIRST equal to 0 to 1 (i.e. up sampling to down sampling) is:

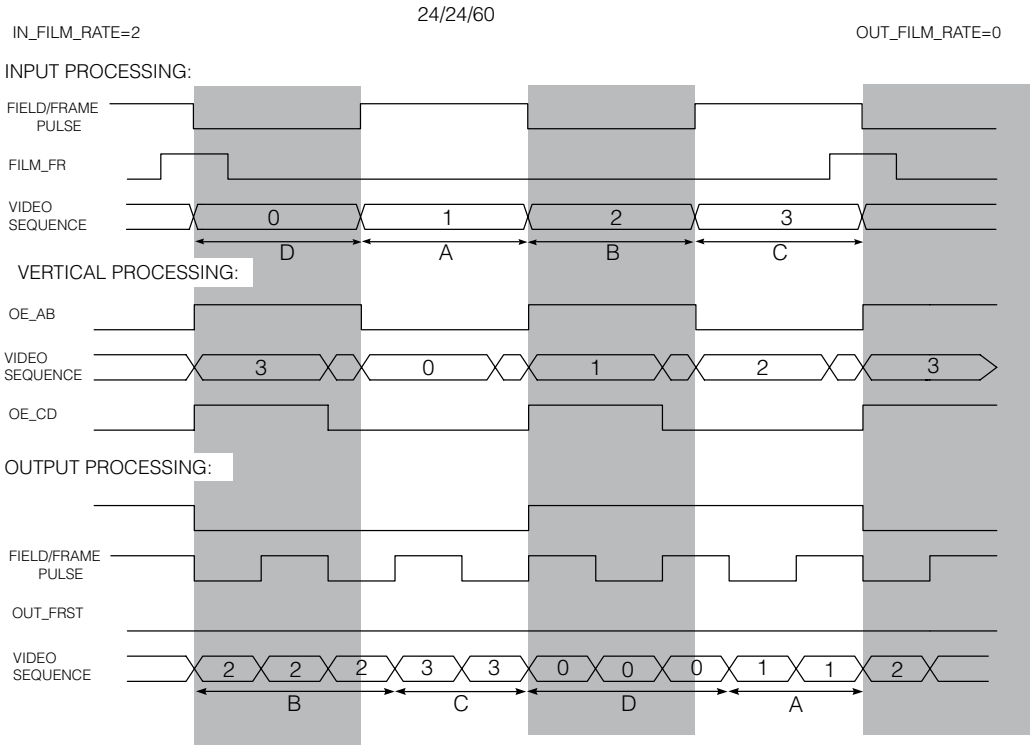
1. Keep H_PROC_FIRST equal to 0 and download a H_ZOOM_RATIO equal to 524,287 (up sampling).
2. Change H_PROC_FIRST to 1 and download H_ZOOM_RATIO equal to 524,288 (down sampling).
3. Change to the desired H_ZOOM_RATIO.

5.3.2 V_FLT_DEC Switching

The vertical filter operates on field/frame (N-1), but the vertical filter coefficients operate on field/frame (N). When the V_FLT_DEC is switched from 0 to 1 or vice versa, the vertical filter coefficients must be delayed by one field/frame so that they operate on the same time frame. This is necessary because the filter coefficients are used differently in decimation mode and a non-decimation filter would be used in decimation mode and vice versa. This would most directly affect the DC gain of the filter that may be perceived as a brightness change in the output video. The horizontal coefficients do not need to be delayed when switching H_FLT_DEC because the horizontal filter and the horizontal coefficients operate on the same frame/field (N). Even though H_FLT_DEC is switched, down sampling (H_PROC_FIRST=1) is indicated. Delaying the vertical filter coefficients may not be necessary depending on the application.

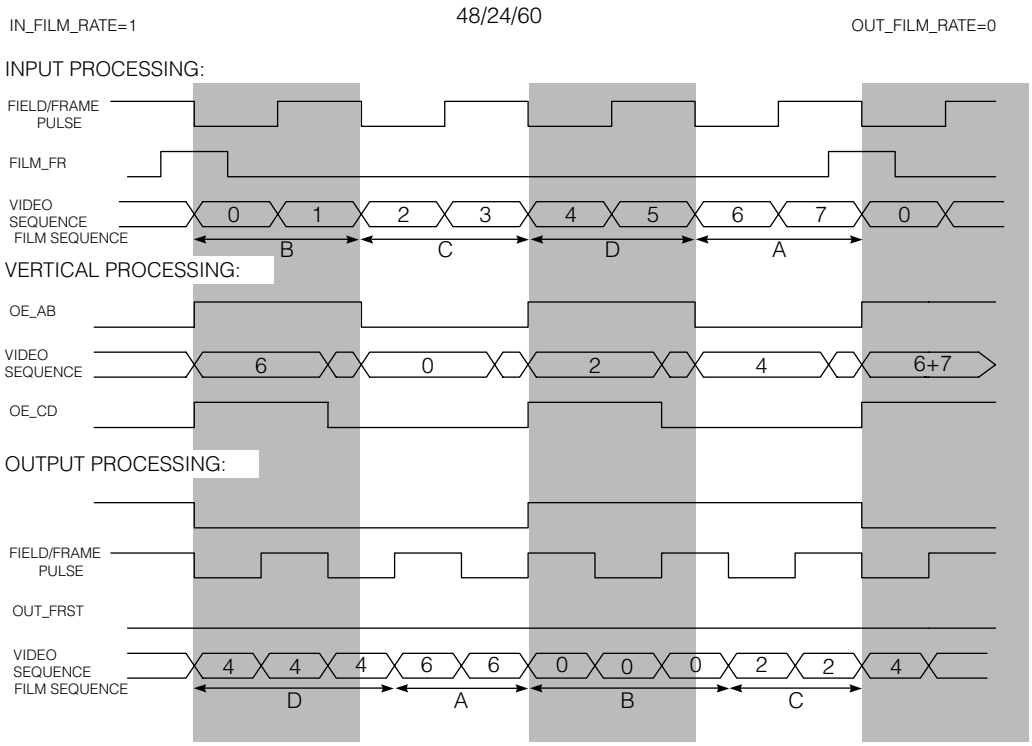
5.3.3 Pseudo Synchronous Film Mode Conversions

This section applies to any film mode conversion when the input frame rate or the output film rate is 3:2 pull-down, but the input rate is not (i.e. 48→60, 24→60). In these cases the zoom and pan update rate is restricted to every other film frame as shown in Figure 10 and Figure 11. This is because the output circuit must be updated on an output field/frame boundary.



Do not download in the shaded regions (OE_AB=1). If the GF9320 is downloaded in the shaded region, the output circuit will be updated in the middle of an output field/frame and will cause one field/frame of the output to be invalid.

Fig.10 24/24/60 Download Restrictions



Do not download in the shaded regions (OE_AB=1). If the GF9320 is downloaded in the shaded region, the output circuit will be updated in the middle of an output field/frame and will cause one field/frame of the output to be invalid.

Fig.11 48/24/60 Download Restrictions

6. SDRAM MEMORY INTERFACE

6.1 MEMORY INTERFACE DESCRIPTION

To achieve high quality scaling of images in two dimensions, separate processing has to be done in the horizontal and vertical dimensions using one dimensional filter banks. Hence, the input image has to be transposed before and after vertical processing and uses SDRAMs to achieve real-time transposition of digital video images using high quality filters.

The SDRAM controller within the GF9320 acts as the master controller of the memory arrays. To perform a transpose operation the memory controller writes the entire image from one field into the image buffer and then reads it out during the next field. Further, during film mode processing, the controller can put two consecutive image fields together and read them out in the next frame as a single progressive frame. The latter technique is used for processing film material with 3:2 pull-down. We can also separate even and odd fields from a progressive frame to create film material with 3:2 pull-down. The memory organization for transposing images at high data rates is shown in Figure 12.

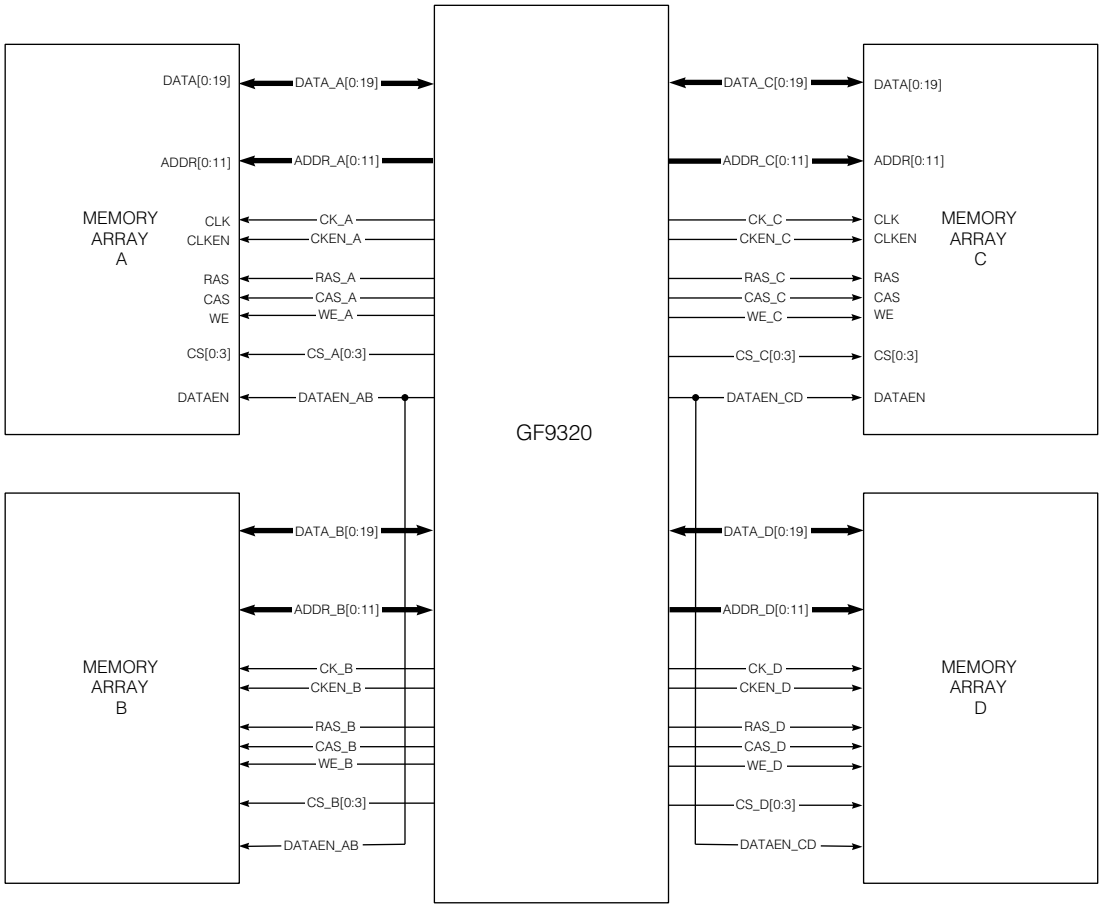


Fig. 12 Memory Interface

The memory organization consists of four arrays of memories communicating with the GF9320. Each array can contain anywhere between one to five SDRAMs based on format conversion mode. To achieve high bandwidth, the memory arrays are arranged in an interleaved fashion. That is, when one field in written into memory array A, the other field will be read out of memory array B. The sequence of read/write operations that takes place in non-film applications is shown in Figure 13.

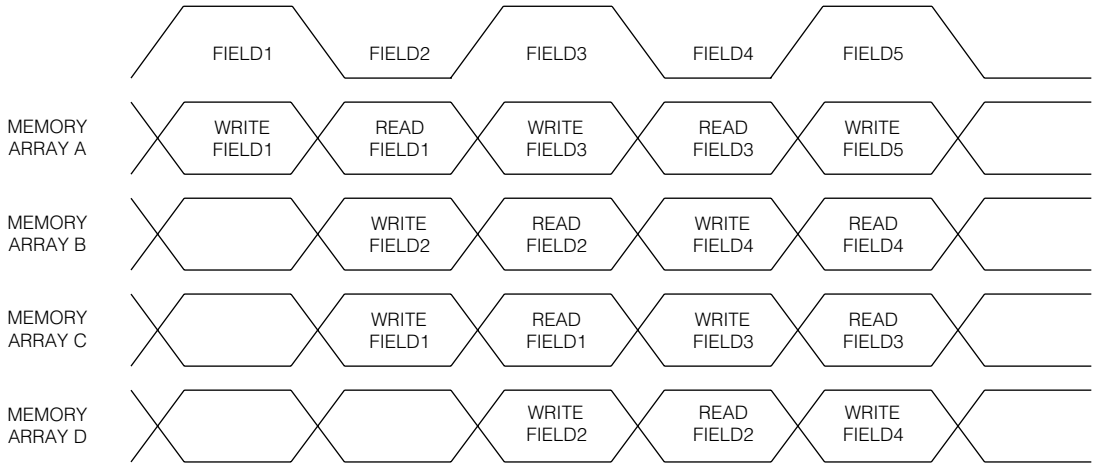


Fig. 13 Timing Diagram of Data between GF9320 and SDRAMs

The data from an odd field is written into memory array A during Field3. At the same time data from the previous (even) field will be read out as a transposed image from memory array B. The horizontal rows of data read out from memory array B will then be processed (vertical processing) within the GF9320 and written into memory array D. Simultaneously, the vertically processed image data from two fields back which was written into memory array C will be read out. When the image is read out from memory array C, it went through another image transposition so that the image is back to its original orientation. Effectively, there is a two field/frame delay when we are processing non-film material is processed.

The GF9320 experiences significantly more processing time in the vertical processing section due to the bandwidth limitations of the SDRAMs. For some conversions the processing time might exceed the available time. This condition can be circumvented by either increasing the number of memories in the array or by increasing the processing clock rate.

If the system is already running at its full capacity in terms of memories and processing clock rate, then the GF9320 cannot handle the specified conversion. This condition (vertical processing time greater than available time) occurs because of the bandwidth limitations of SDRAM.

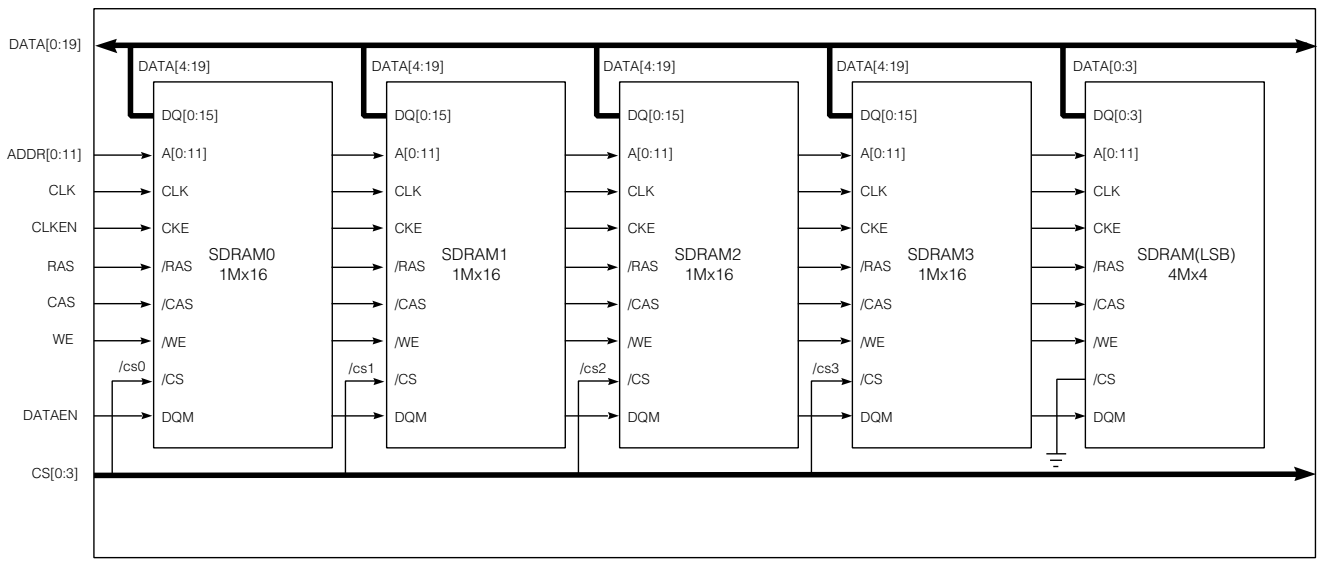


Fig. 14 Architecture of Memory Array with four 1Mx16 and one 4Mx4 SDRAMs

During vertical processing, the GF9320 pre-reads (number of pixels = pix2read) into its internal FIFO, before the beginning of every scan line so that it can supply the pixels from the FIFO into the one-dimensional filter in an uninterrupted way. The number of pixels to be pre-read is chosen based on several I/O parameters so that it is high enough to supply data continuously to the filter but low enough to complete the vertical processing in the available time.

80Mbits or 5 x 16Mbit SDRAMs are required to store 2048 x 2048 x 20 bits (maximum image size). The memory array has a 20-bit data bus path, supported by blocks of four 1Mx16 SDRAMs and one 4Mx4 used in parallel, sharing a common address/control bus. 1Mx16 SDRAMs store the upper significant bits of luminance Y[10:2] and colour difference C[10:2]. 4Mx4 SDRAM stores the lower significant bits Y[1:0] and C[1:0].

All elements in the array can be simultaneously selected for command execution by activating the chip select signals or commands can be directed to a particular element in the array by activating the chip select signal for that element and deactivating the chip select signal for the others. Figure 15 shows the pin connections required for 64M SDRAMs within a memory array. The number of memories for a given format conversion remains the same independent of memory (16M or 64M) being used.

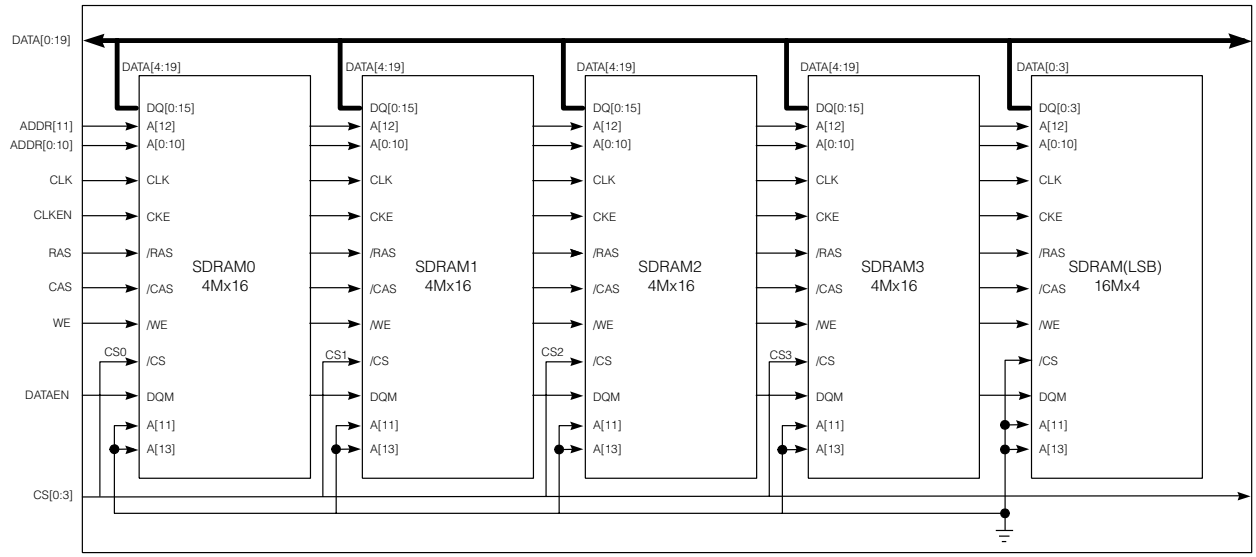


Fig. 15 Architecture of Memory Array with Four 4Mx16 and One 16Mx4 SDRAMs

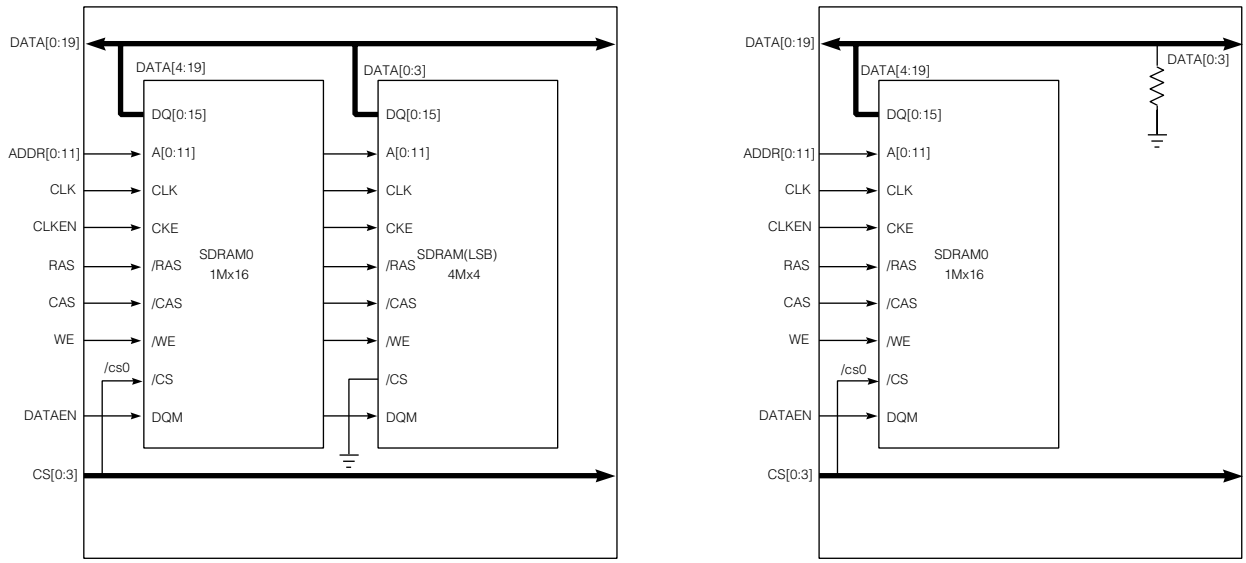
To reduce system cost, the memory array architecture is made scalable. That is, when transposing smaller image sizes or when processing 8-bit images, a lesser number of SDRAMs per memory array are required.

Table 5 shows the memory requirements for various format conversions. Figure 16 shows the memory array architecture when the number of SDRAMs is reduced to 2 SDRAMS and one SDRAM (8 bit processing) per memory array.

TABLE 5: Minimum SDRAM Configurations for Mode 8 (default model)

IMAGE WIDTH (max) x max (Input Image Height, Output Image Height)[1]	NUMBER OF SDRAMS REQUIRED / BANK (2 banks per transpose)		DOWNLOAD PARAMETERS			
	[Y, C] 10-bits	[Y, C] 8-bits	MDL[2]	MCL[3]	MDR[4]	MCR[5]
2048 x 2048	4 (1Mx16) and 1 (4Mx4)	4 (1Mx16)	0	00	0	00
2048 x 1536	3 (1Mx16) and 1 (4Mx4)	3 (1Mx16)	0	01	0	01
2048 x 1024	2 (1Mx16) and 1 (4Mx4)	2 (1Mx16)	0	10	0	10
2048 x 512	1 (1Mx16) and 1 (4Mx4)	1 (1Mx16)	0	11	0	11

NOTES:
1. max(a, b) = a when a >= b, else b when a < b.
2. MDL stands for the parameter MODE_16_LEFT
3. MCL stands for the parameter MEM_CONFIG_LEFT
4. MDR stands for the parameter MODE_16_RIGHT
5. MCR stands for the parameter MEM_CONFIG_RIGHT



a) Two SDRAMs per Array one for MSB and for LSB

b) One SDRAMs per Array one for 8 bit proccessing --LSB are pulled down with 1K resistor to ground

Fig. 16 Architecture of Memory Array with Lesser Number of SDRAMs per Array

6.3 SDRAM SPECIFICATIONS

The speed grade of the SDRAM is chosen depending on the processing clock frequency. For example, if the processing clock is running at 74.25MHz, SDRAM with a speed grade of -10 or 100MHz should be selected.

6.4 SPECIAL PROCESSING

6.4.1 Model 16

To further decrease the memory requirements at the expense of processing time an additional mode is available. Table 6 summarizes the memory requirements for various format conversions in this mode.

6.5 FILM PROCESSING

During film processing the GF9320 uses the external signals FILM_FR and OUT_FRST to encode or decipher the 3:2 pull-down sequence. The timing of these signals for different modes (film and non-film) is shown in Figure 17 through Figure 42. When the input video is from a film material with 3:2 pull-down, the GF9320 processes the image vertically after combining the even and odd fields to achieve better quality resizing. Duplicate fields in the input sequence are rejected by not writing into the memory. Note that in film modes memory switching does not occur at every field/frame boundary. It depends on the input and output film formats. For example, when the input is video with 3:2 pull-down, the left array of memories switch only

TABLE 6: Minimum SDRAM Configurations for Mode 16

IMAGE WIDTH (max) x max (Input Image Height, Output Image Height)[1]	NUMBER OF SDRAMS REQUIRED / BANK (2 banks per transpose)		DOWNLOAD PARAMETERS			
	[Y, C] 10-bits	[Y, C] 8-bits	MDL[2]	MCL[3]	MDR[4]	MCR[5]
1024 x 2048	2 (1Mx16) and 1 (4Mx4)	2 (1Mx16)	1	10	1	10
1024 x 1024	1 (1Mx16) and 1 (4Mx4)	1 (1Mx16)	1	11	1	11

NOTES:
1. max (a, b) = a when a >= b, else b when a < b.
2. MDL stands for the parameter MODE_16_LEFT
3. MCL stands for the parameter MEM_CONFIG_LEFT
4. MDR stands for the parameter MODE_16_RIGHT
5. MCR stands for the parameter MEM_CONFIG_RIGHT

after even and odd fields have been put together. The switching point is shown in the timing diagram by OE_AB and OE_CD signals that are, respectively, the output enable signals for left and right arrays. The GF9320 achieves 3:2 pull-down at the output by separately reading out the even and odd fields.

The film sequences shown in Figure 17 through Figure 42 are not the only film frame sequences that the GF9320 can generate. Other input/output film sequences are possible. The input control uses the rising edge of FILM_FR to set the input film sequence and the film frame reset sent to the output controller. The first TRS V-bit after the rising edge of FILM_FR marks the beginning of a 3:2 (starting with 3) or 2:2 film sequences. The falling edge of FILM_FR is only used in 48→60 (IN_FILM_RATE=1 and OUT_FILM_RATE=3) and 24→60 (IN_FILM_RATE=2 and OUT_FILM_RATE=3) applications. In these applications it sets the output 3:2 film sequence (starting with the 3). The FILM_FR reset should be chosen based on the desired film application.

During film processing there is a possibility that for some conversions the GF9320 could violate the refresh period (64 ms) of the SDRAM. If a violation is found (IN_REFR_LEFT or OUT_REFR_RIGHT = '1'), then the appropriate (left/right) refresh bit should be activated in the download stream of parameters to the GF9320. Alternatively, Table 7 can be used to determine which input and output formats require refresh bits to be active.

Table 7: Input and Output Formats Requiring Refresh

INPUT FORMAT IN_REFR_LEFT=1	OUTPUT FORMAT OUT_REFR_RIGHT=1
24P/25P	24P/25P
48P/50P	
60I/60P with 3:2 pull-down	

6.6 PROCESSING DELAY

Processing delay for video through the GF9320 depends on the conversion. Table 8 shows the processing delay for different film and non-film modes.

Table 8: Processing Delay for Various Conversions

CONVERSION	DELAY (input frames/fields)
[frame/field modes - 60Hz V processing rate] Note: All other frame rates are identical with appropriate time scaling	
60I → 60I	1/30 seconds (2 fields)
60I → 60P	1/30 seconds (2 fields)
60P → 60I	1/30 seconds (2 frames)
60P → 60P	1/30 seconds (2 frames)
[2:2 modes - 30Hz V processing rate]	
60I → 30P	1/15 seconds (4 fields)
60P →30P	1/15 seconds (4 frames)
30P → 60I	1/15 seconds (2 frames)
30P → 60P	1/15 seconds (2 frames)
60I → 60I	1/15 seconds (4 fields)
60I → 60P	1/15 seconds (4 fields)
[3:2 modes - 24Hz V processing rate]	
60I → 60I	1/10-1/12sec (5-6 fields)
60i → 60p	1/10-1/12sec (5-6 fields)

Table 8: Processing Delay for Various Conversions

CONVERSION	DELAY (input frames/fields)
60I → 24P	3/40-1/12sec (4.5-5 fields)
60I → 48I	3/40-1/12sec (4.5-5 fields)
60P → 24P	3/40-1/12sec (4.5-5 fields)
60P → 48I	3/40-1/12sec (4.5-5 fields)
48I → 60I	3/40-1/12sec (3.6-4 fields)
48I → 60P	3/40-1/12sec (3.6-4 fields)
24P → 60I	3/40-1/12sec (1.8-2 frames)
24P → 60P	3/40-1/12sec (1.8-2 frames)

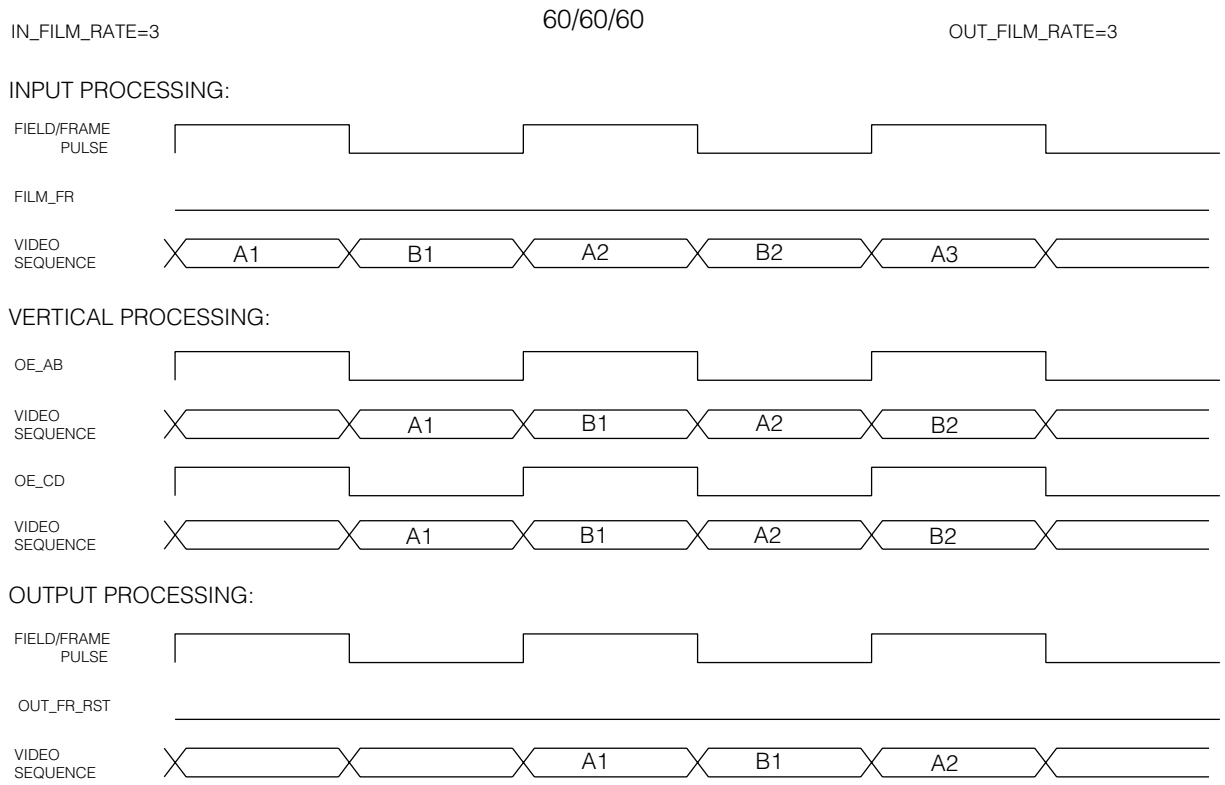


Fig. 17 60/6060/ Processing

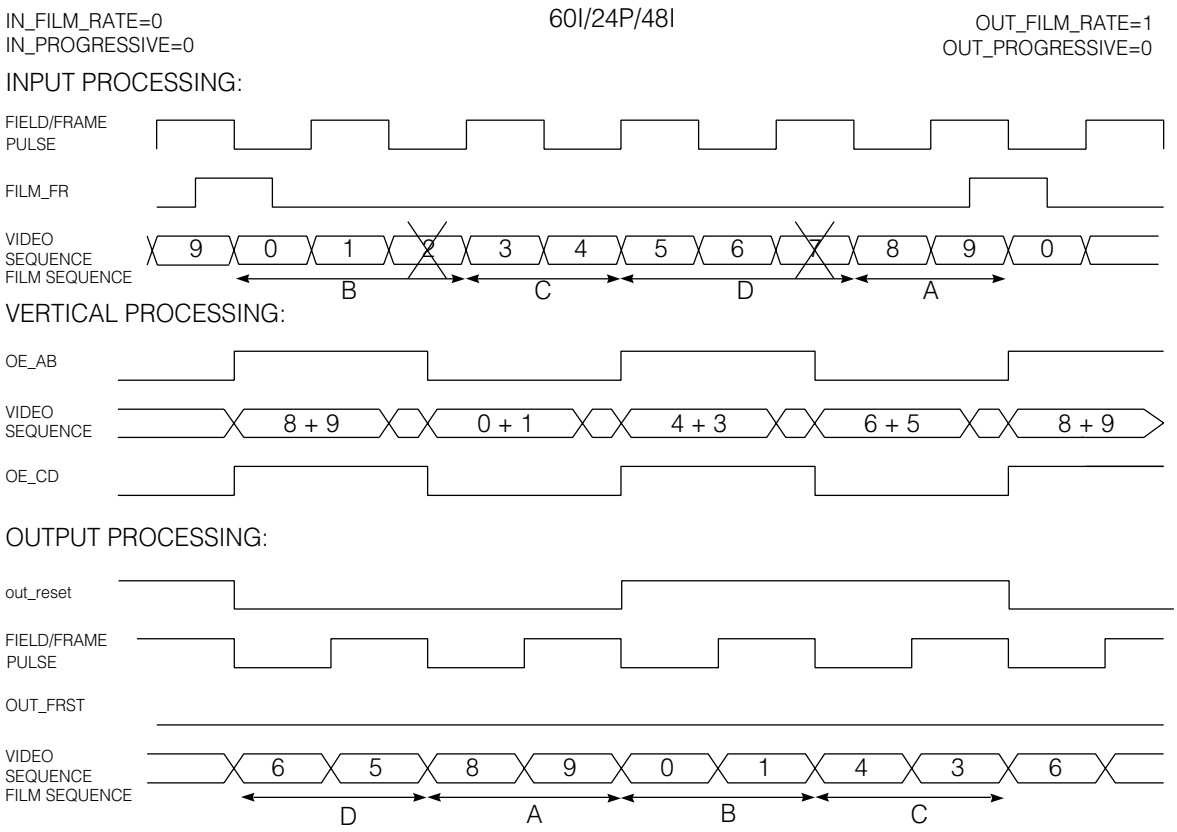


Fig. 18 60I/24P/48I Processing

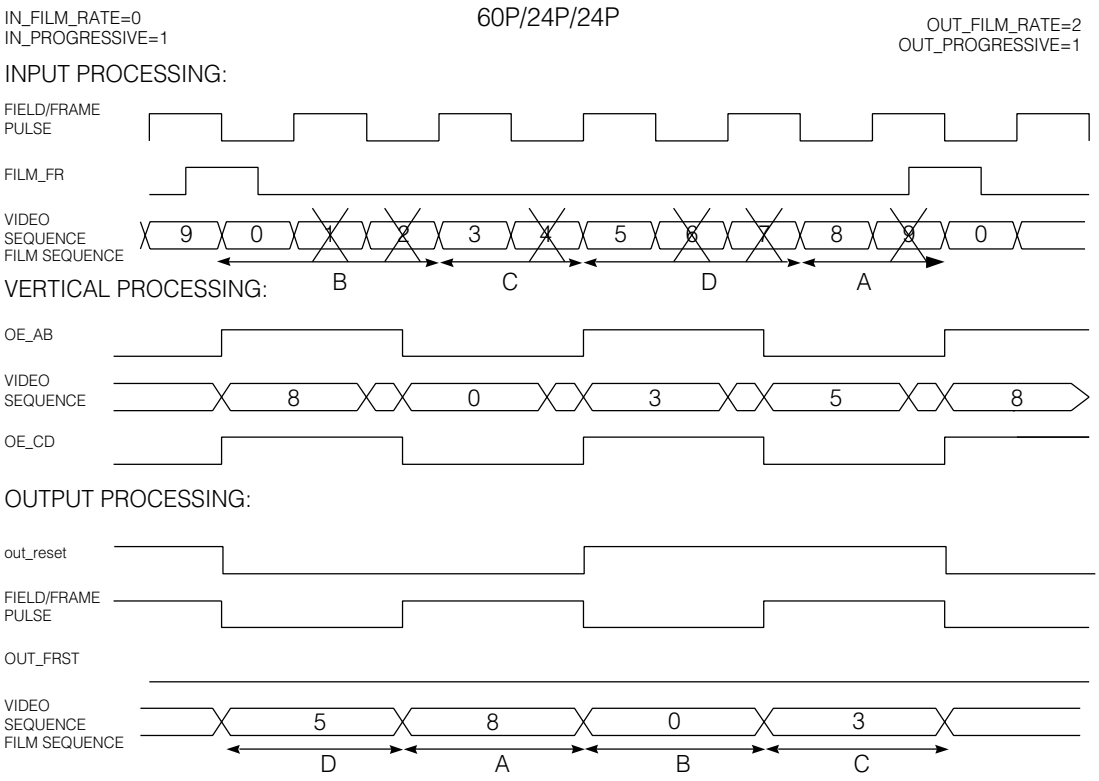


Fig. 19 60P24P/24P Processing

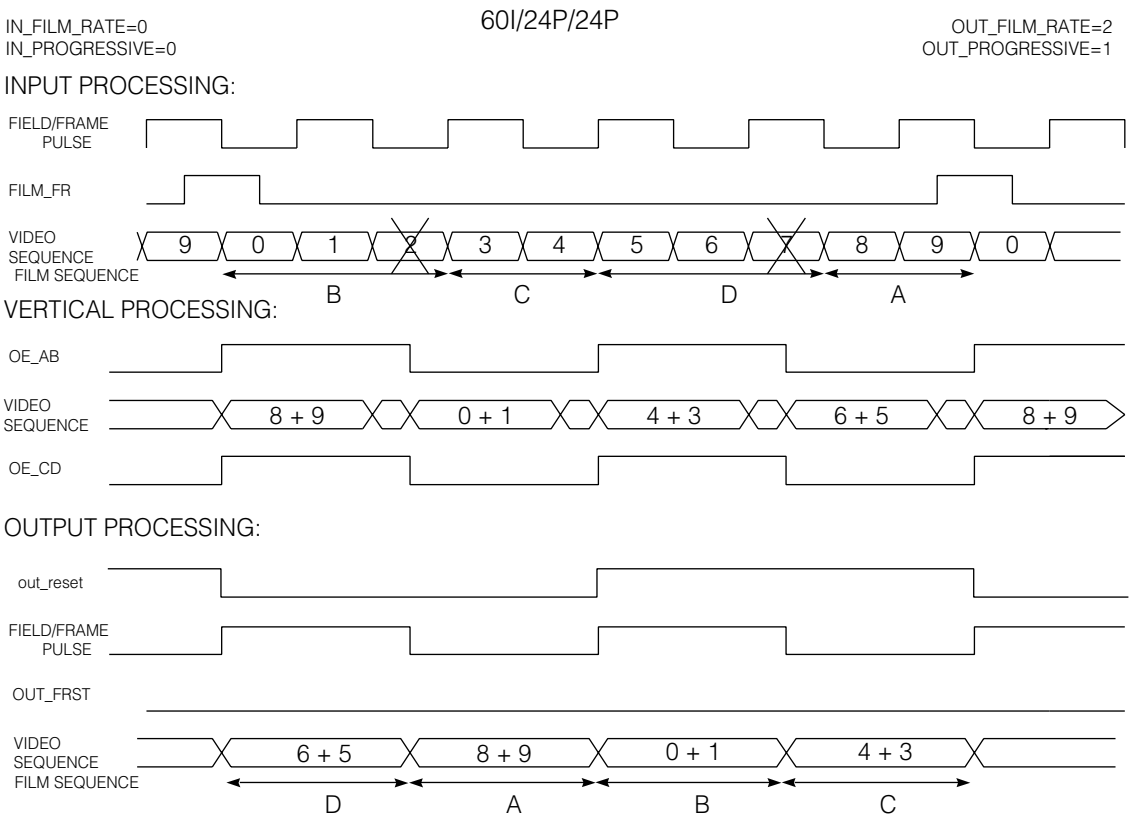
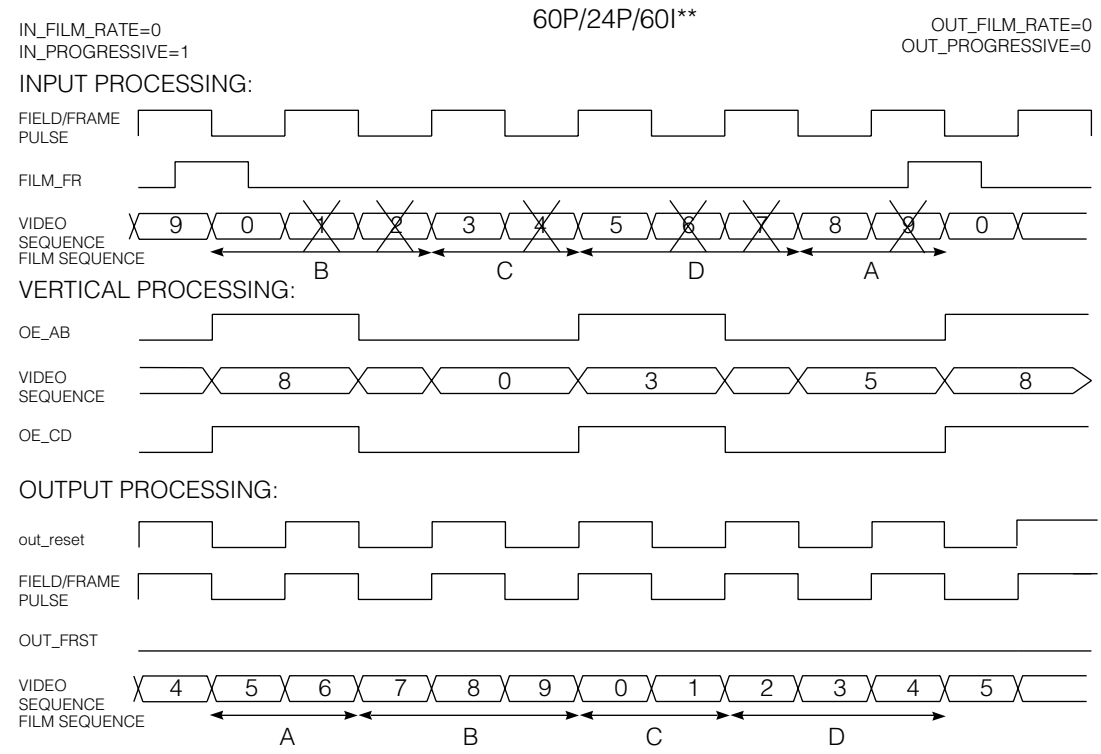
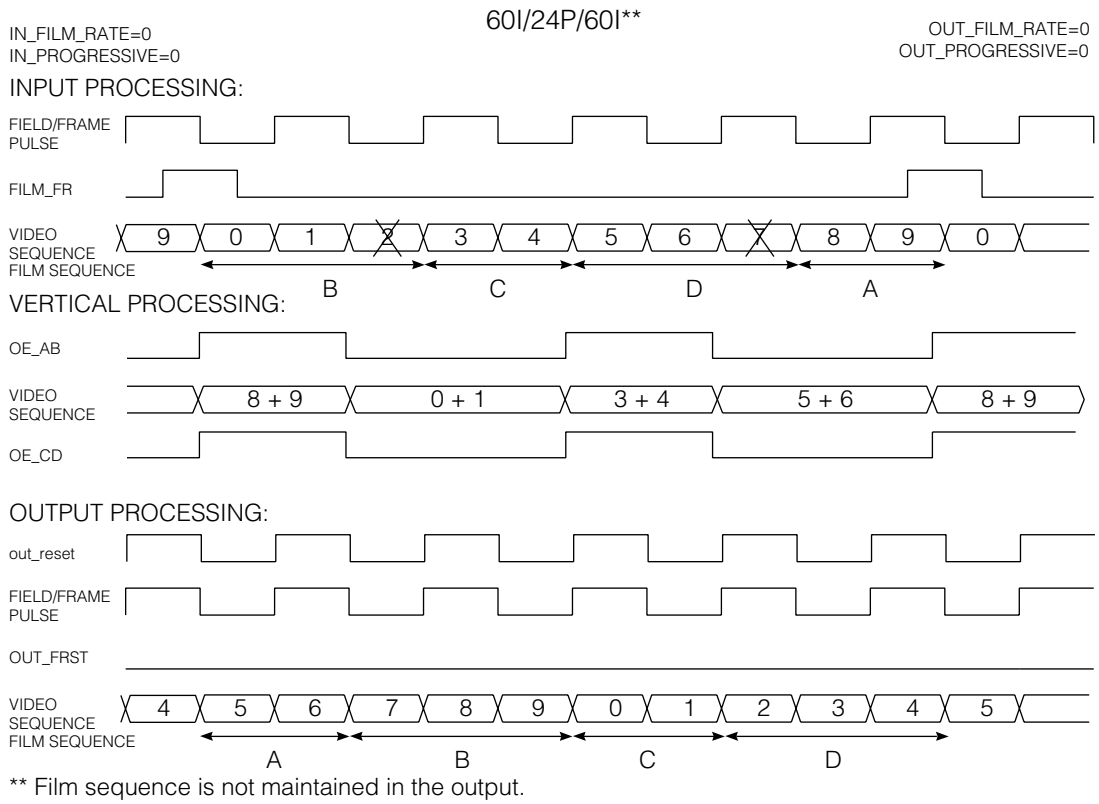


Fig. 20 60I/24P/24P Processing



** Film sequence is not maintained in the output

Fig. 21 60P/24P/60I Processing



** Film sequence is not maintained in the output.

Fig. 22 60I/24/60I Processing

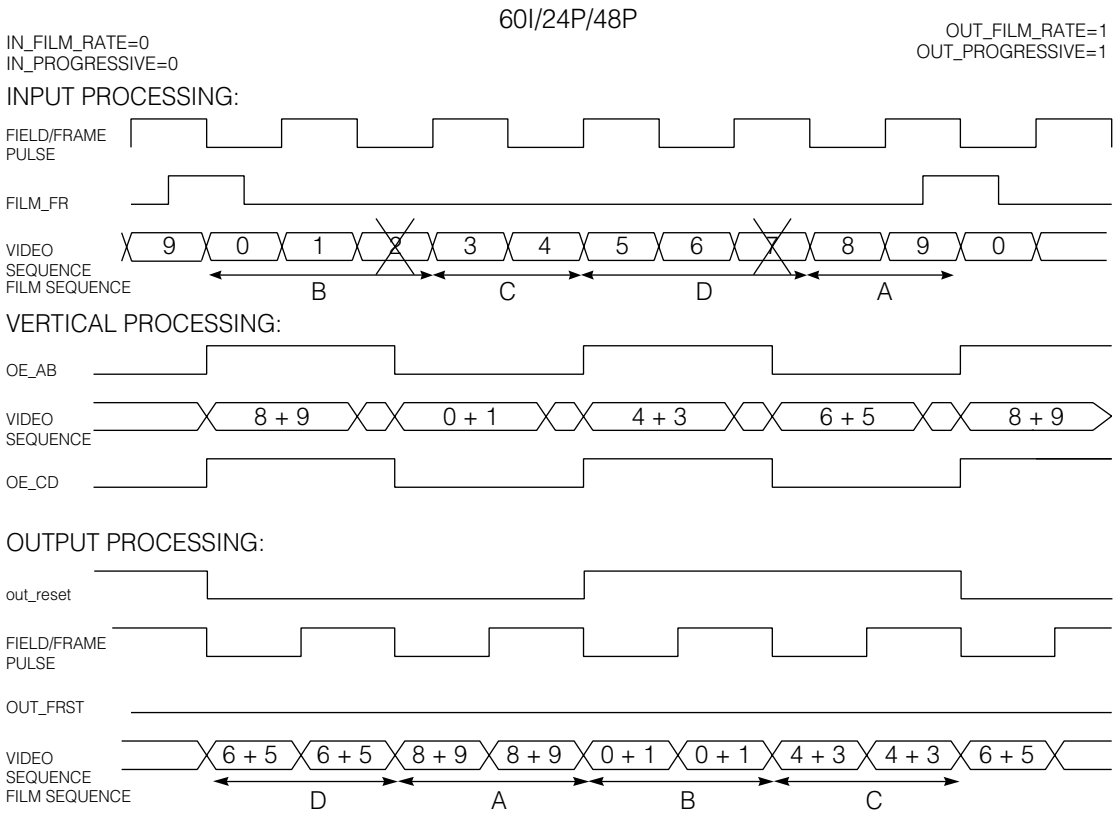


Fig. 23 60I/24P/48P Processing

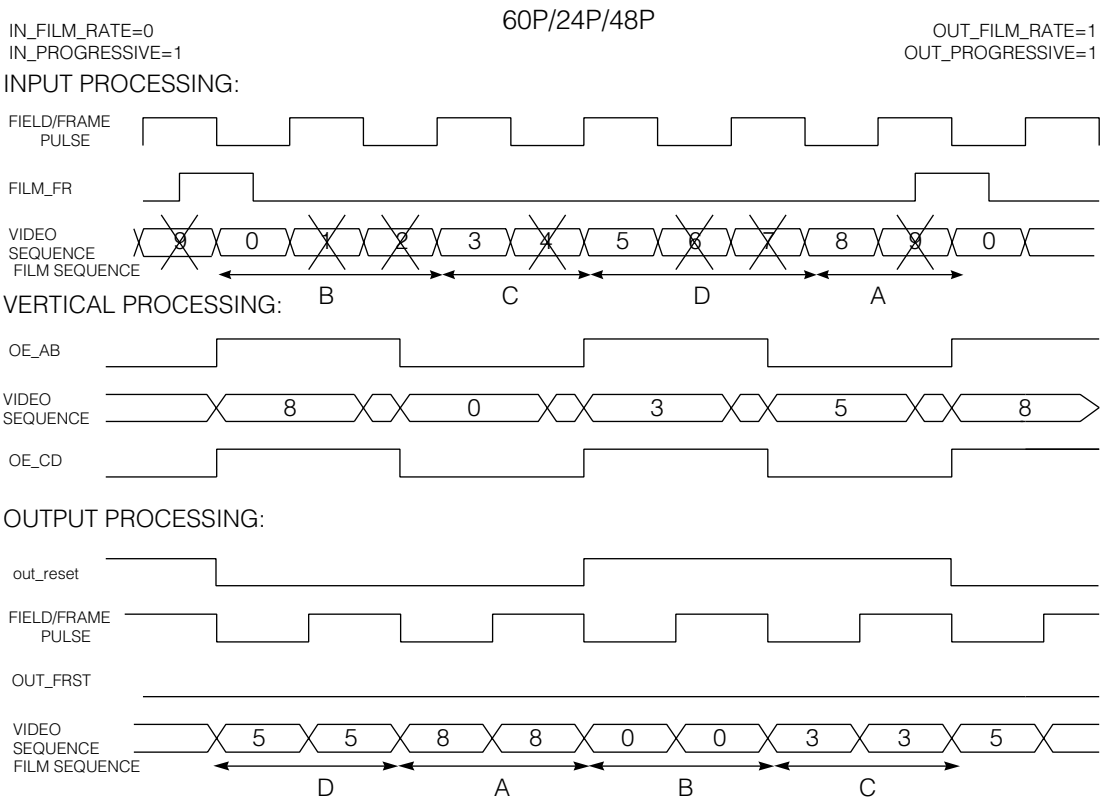


Fig. 24 60P/24P/48P Processing

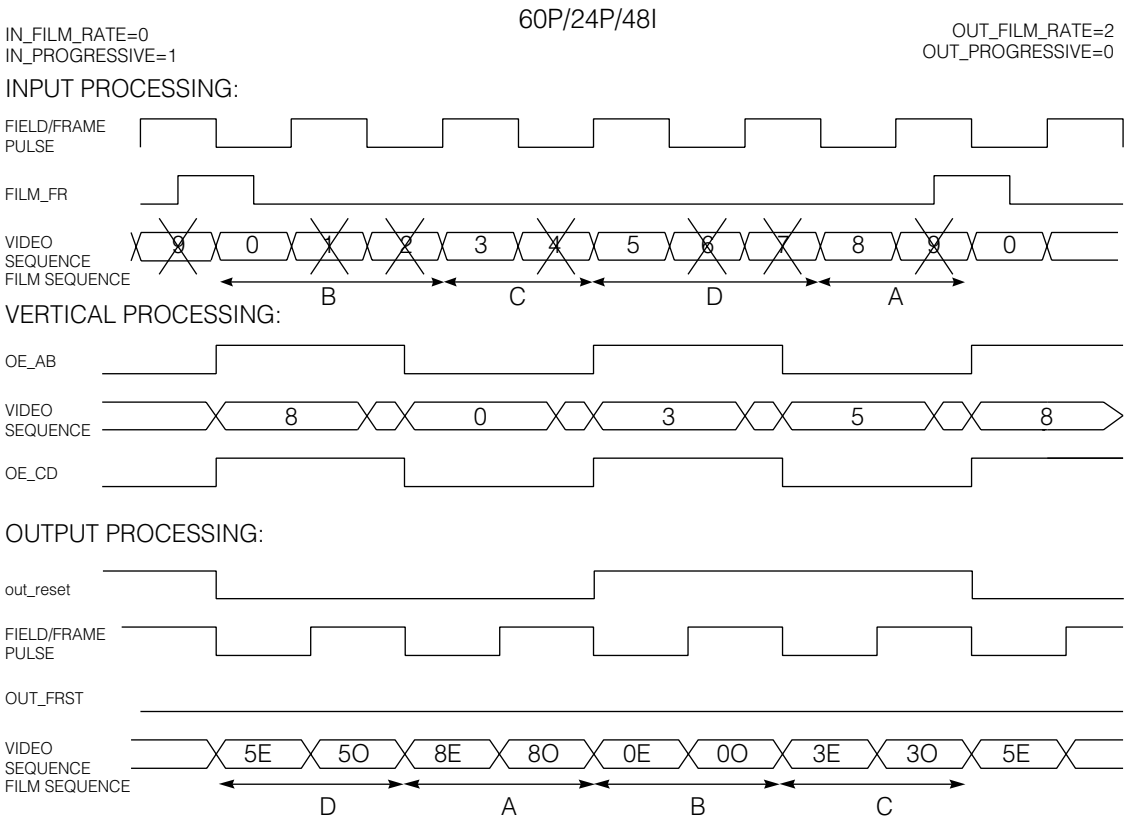


Fig. 25 60P/24P/48I Processing

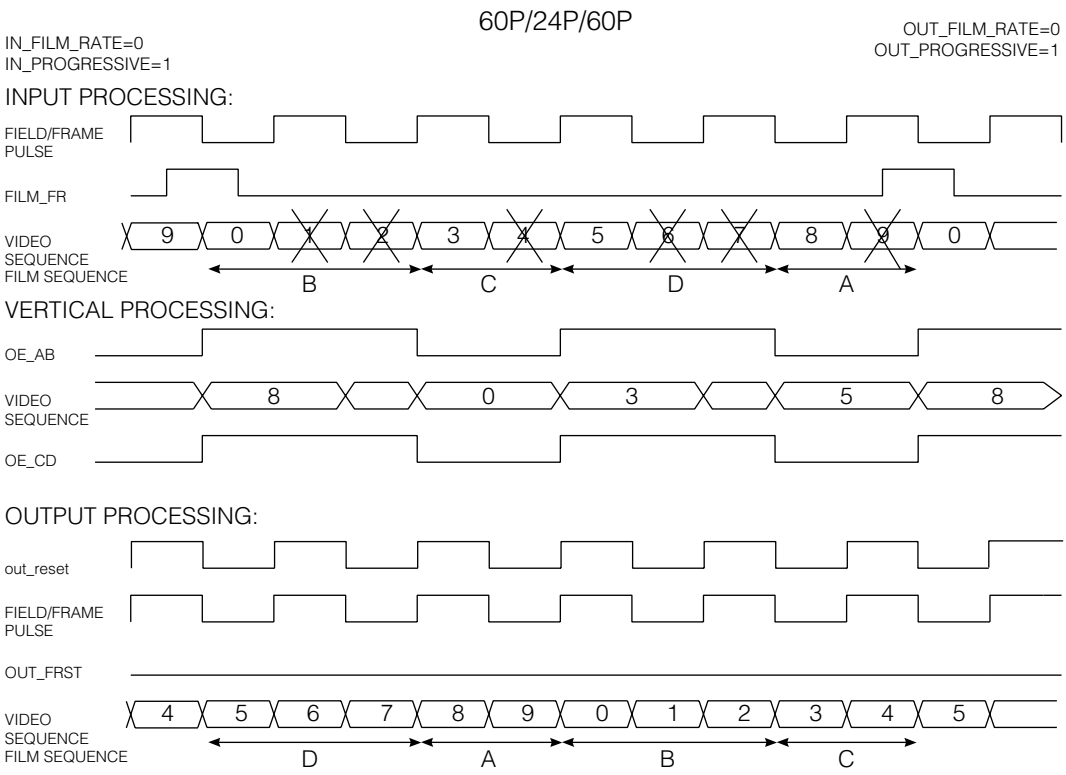
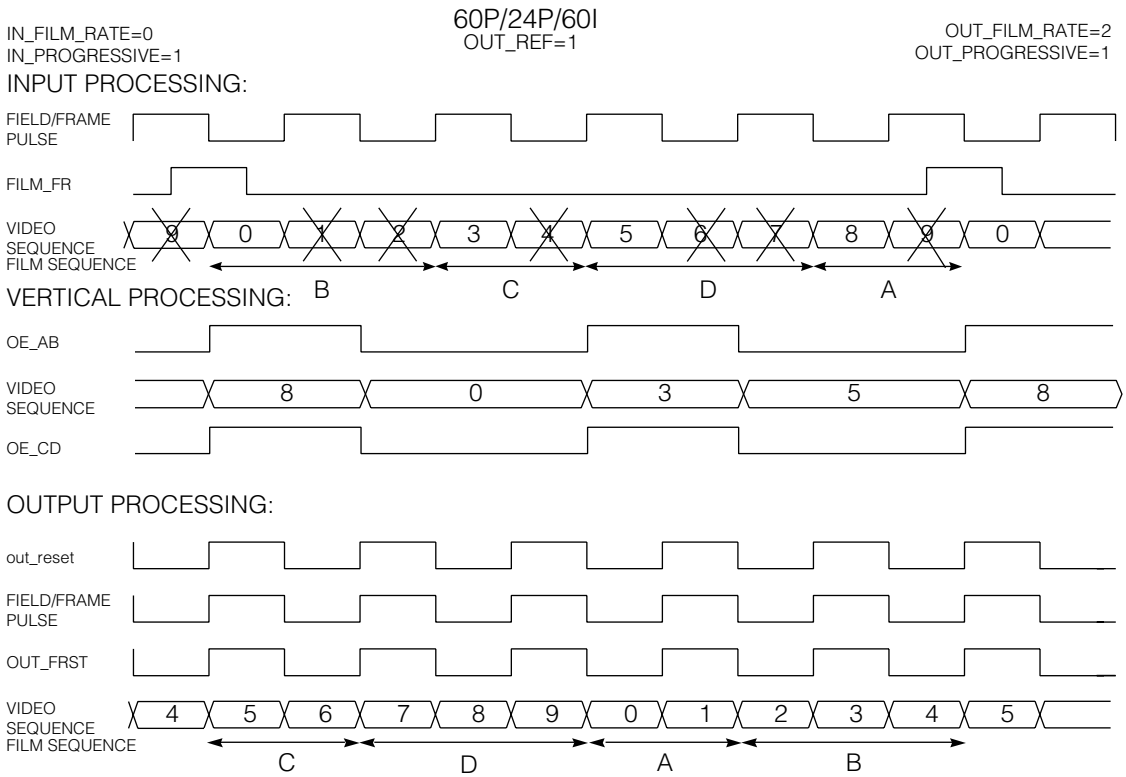
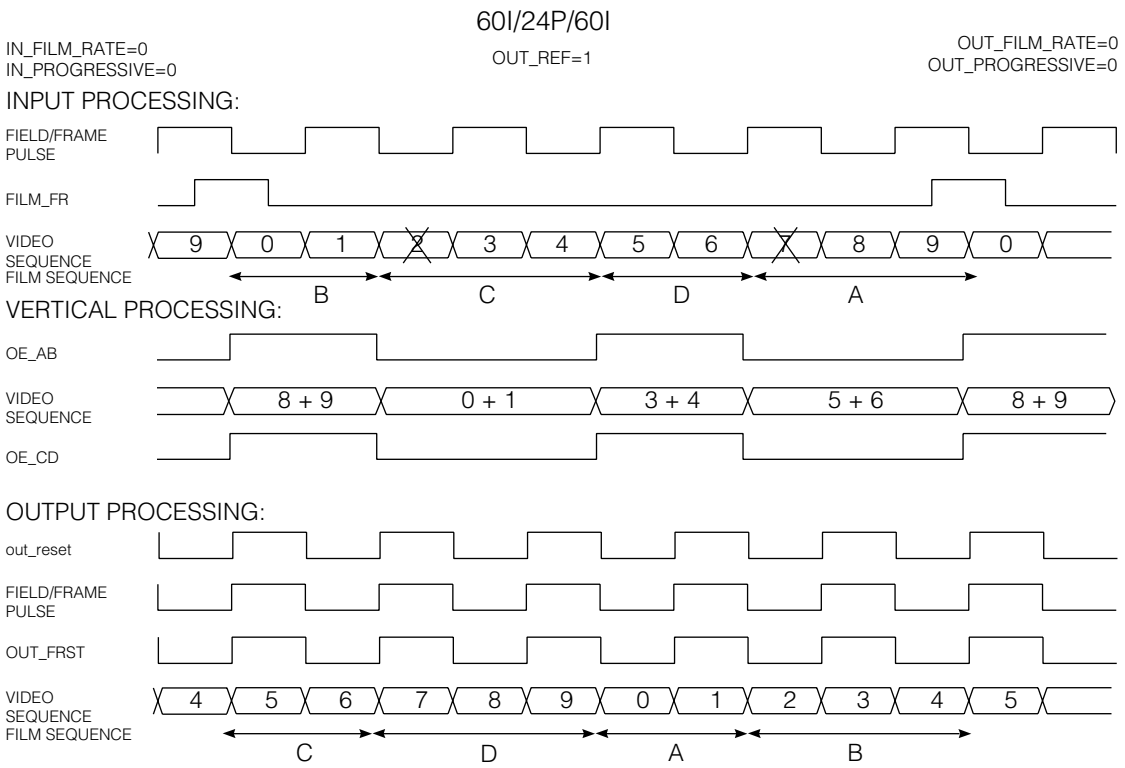


Fig. 26 60P/24P/60P Processing



*** Film sequence at the output is same as the input. (OUT_REF = 1)

Fig. 27 60P/24P/60I (OUT_REF = 1) Processing



***film sequence at the output is same as the input (OUT_REF= 1)

Fig. 28 60P/24P/60I (OUT_REF = 1) Processing

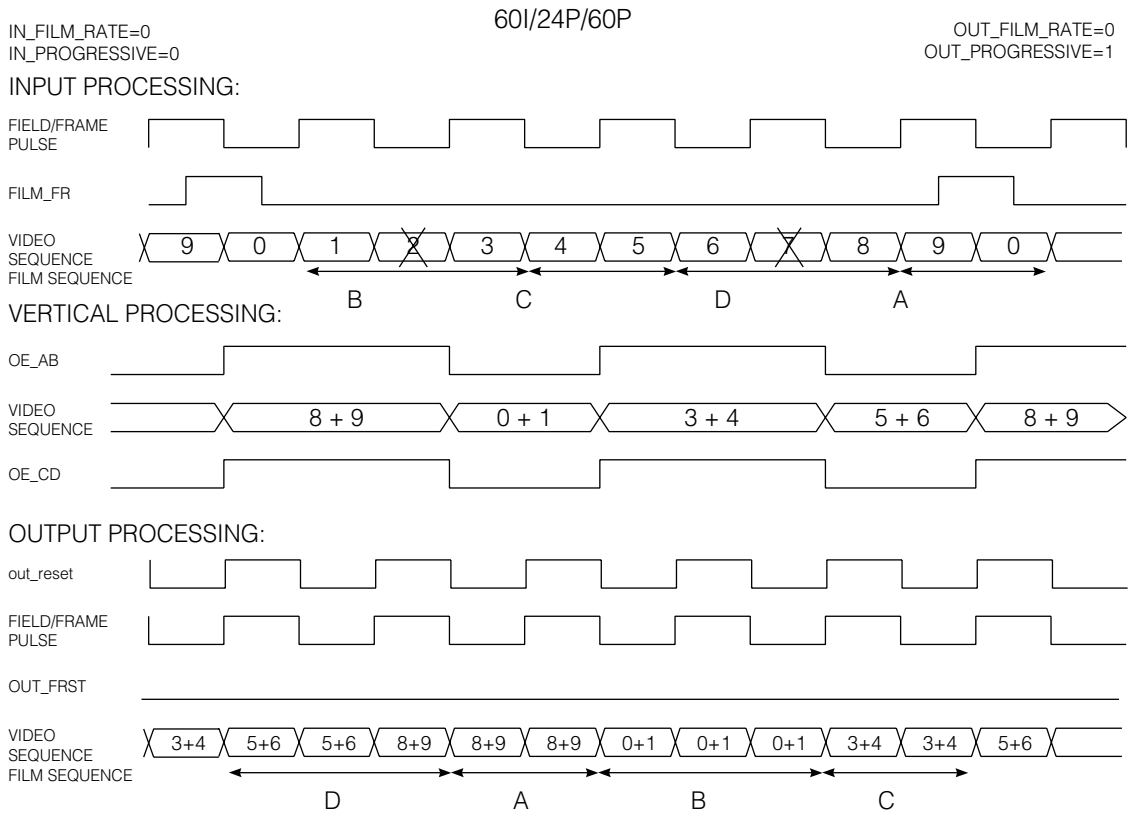


Fig. 29 60I/24P/60P Processing

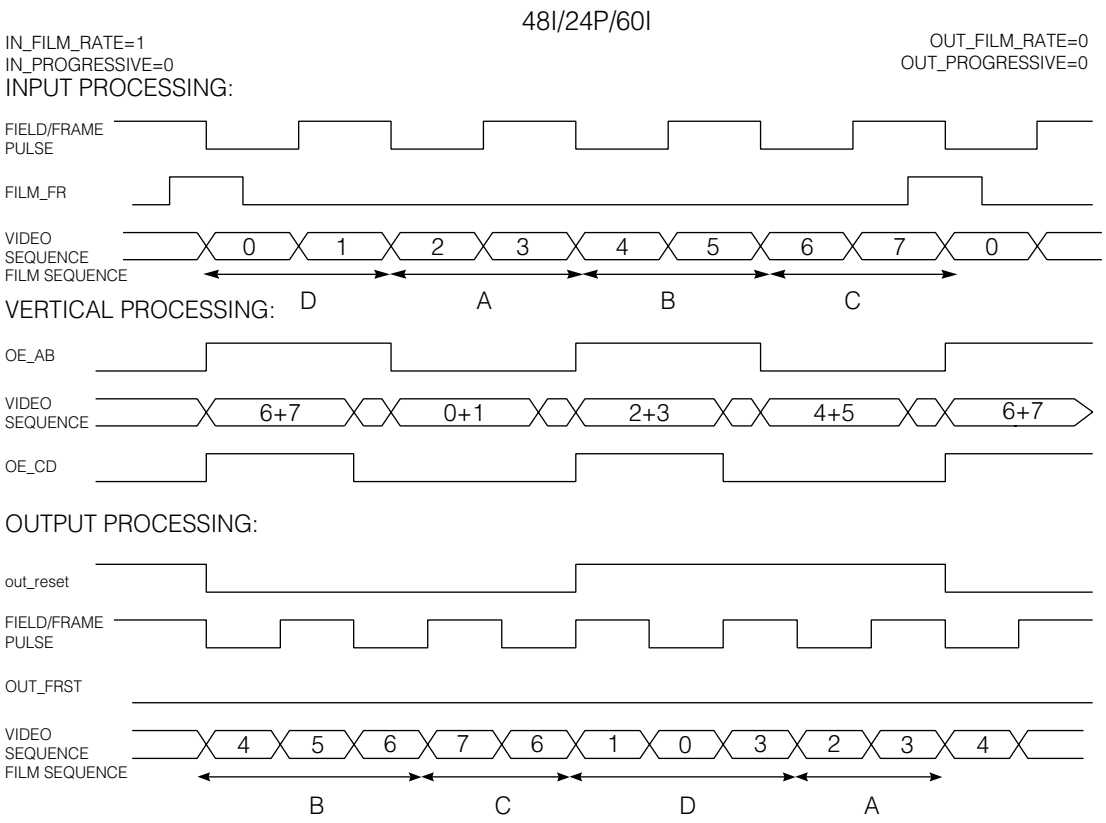


Fig. 30 48I/24P/60I Processing

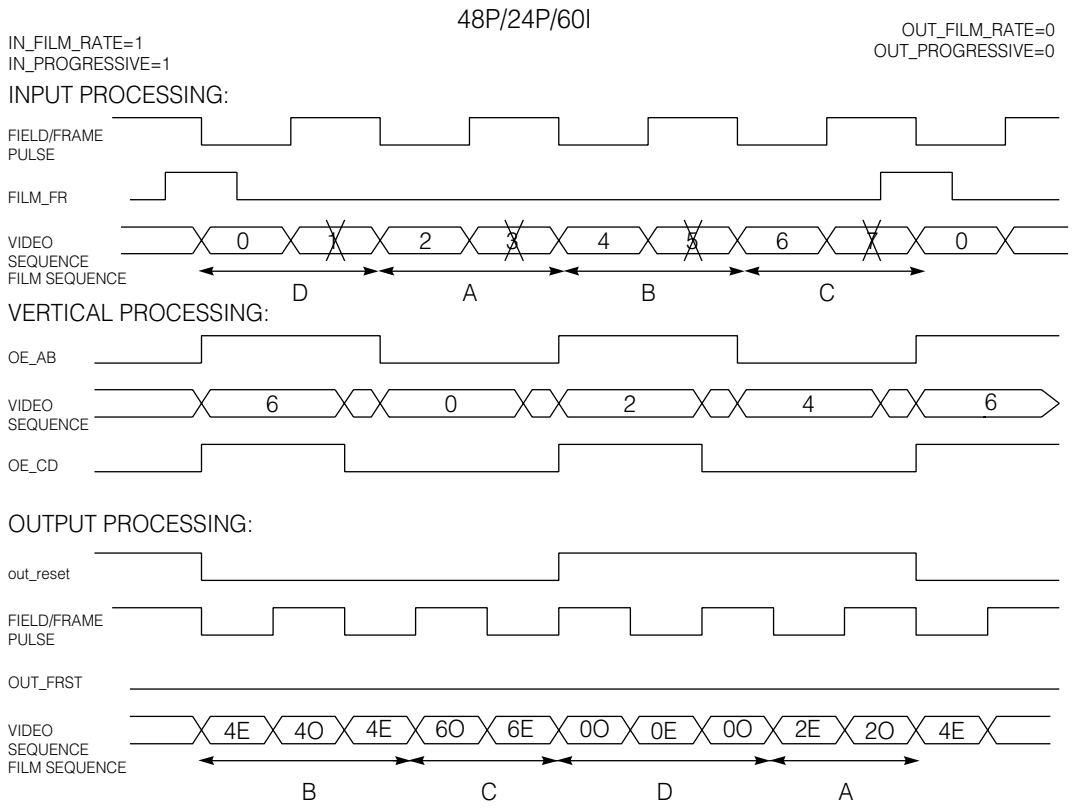


Fig. 31 48P/24P/60I Processing

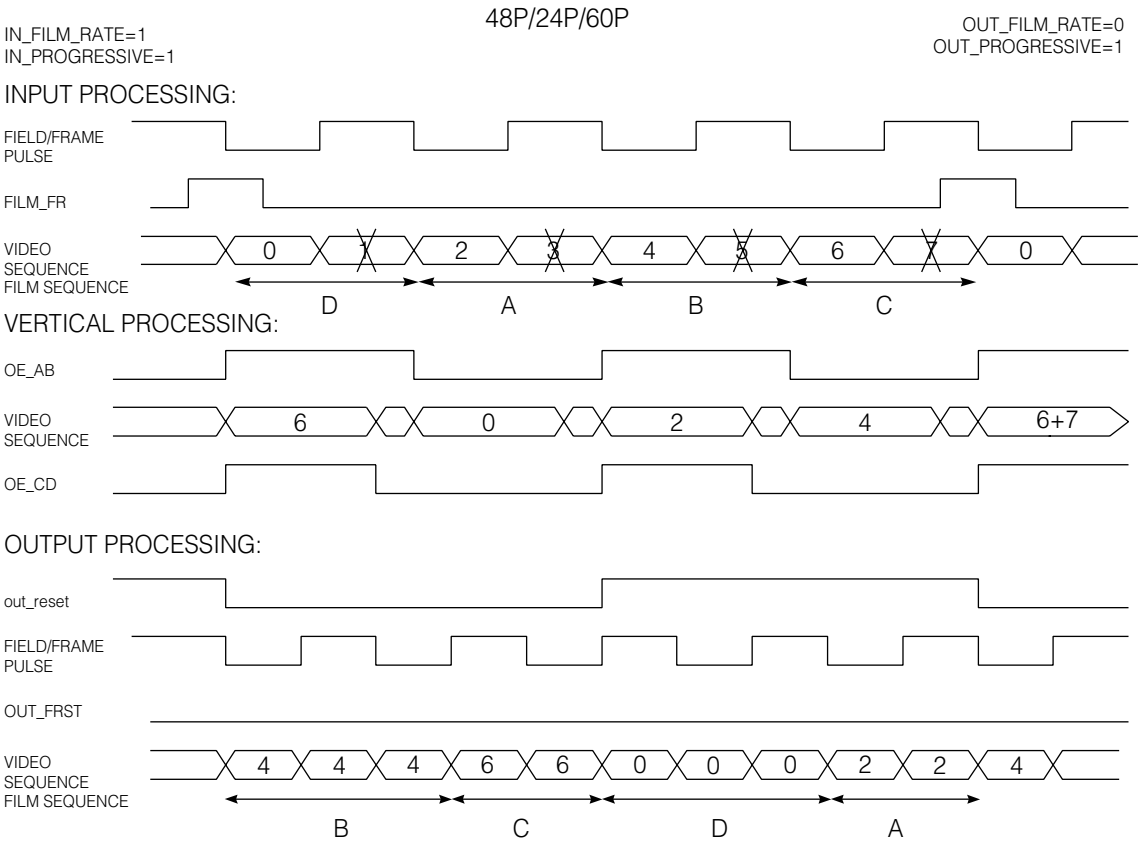


Fig. 32 48P/24P/60P Processing

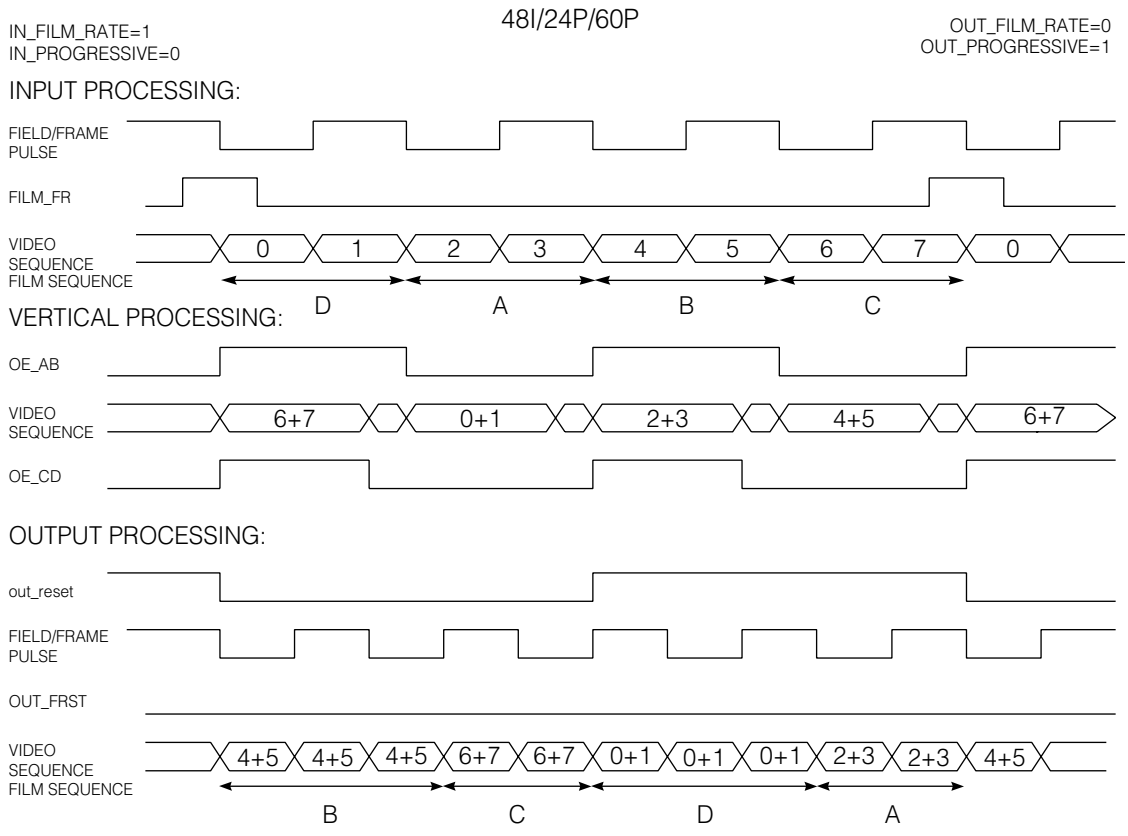


Fig. 33 48I/24P/60P Processing

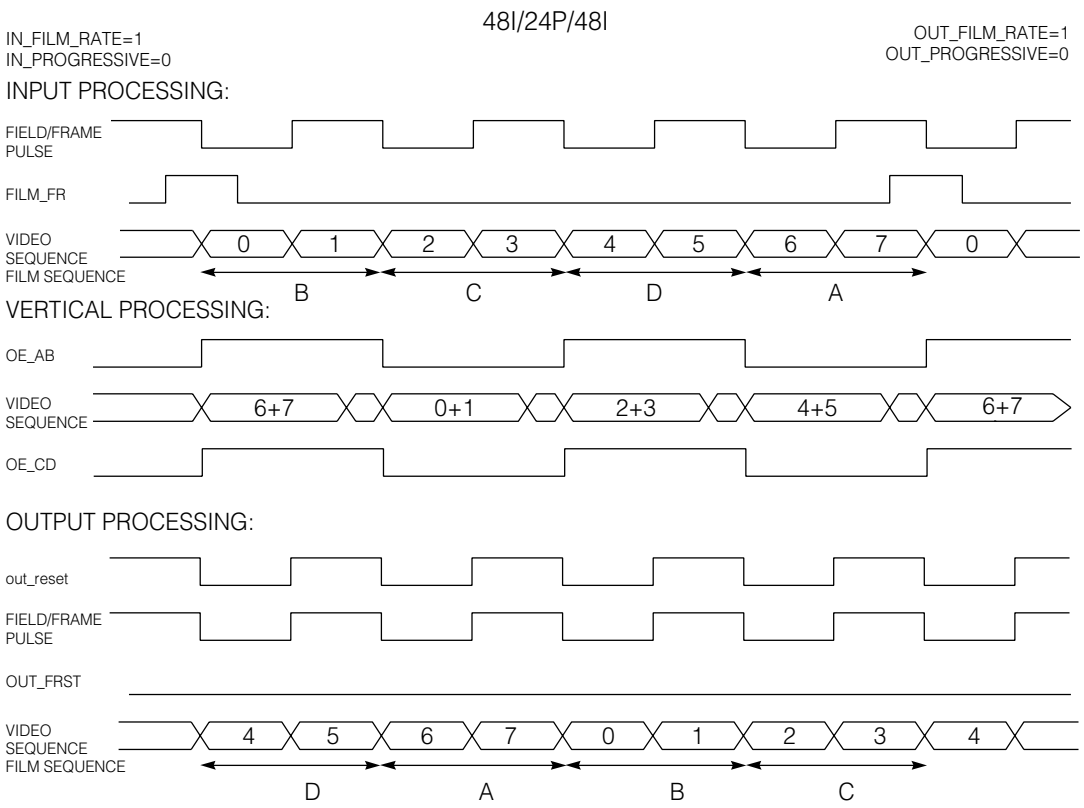


Fig. 34 48I/24P/48I Processing

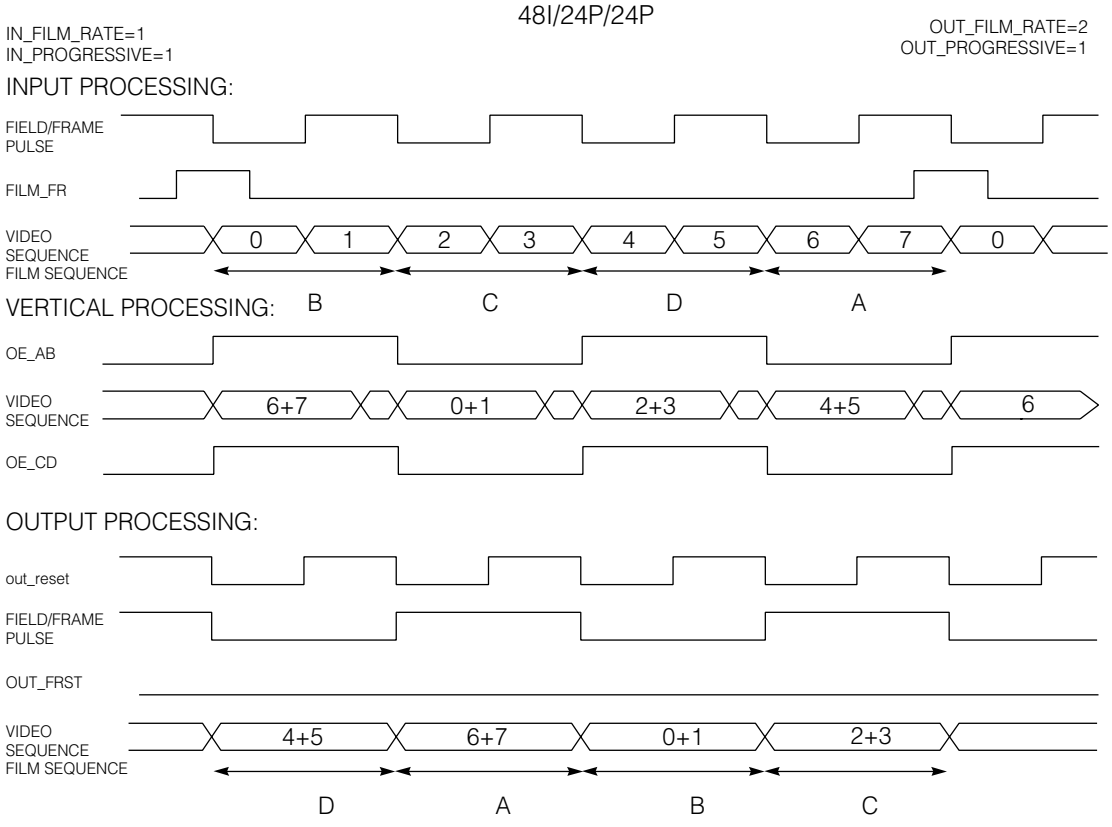


Fig. 35 48I/24P/24P Processing

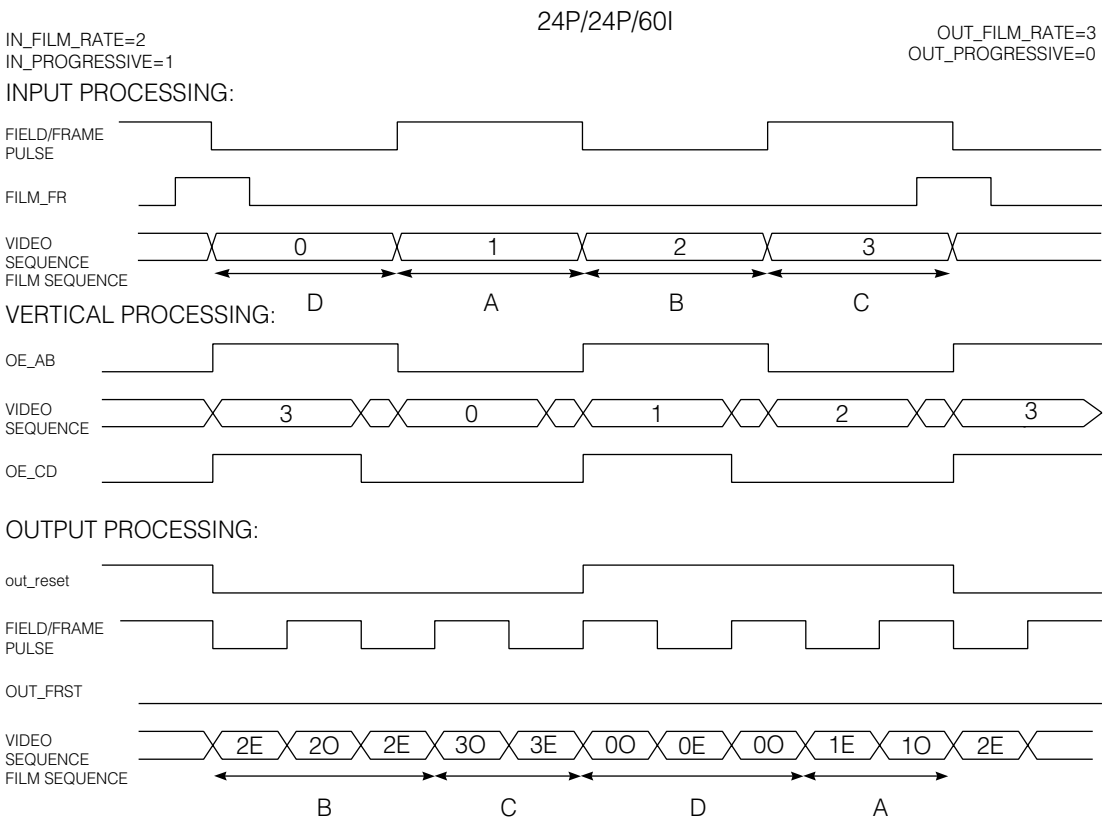


Fig. 36 24P/24P/60I Processing

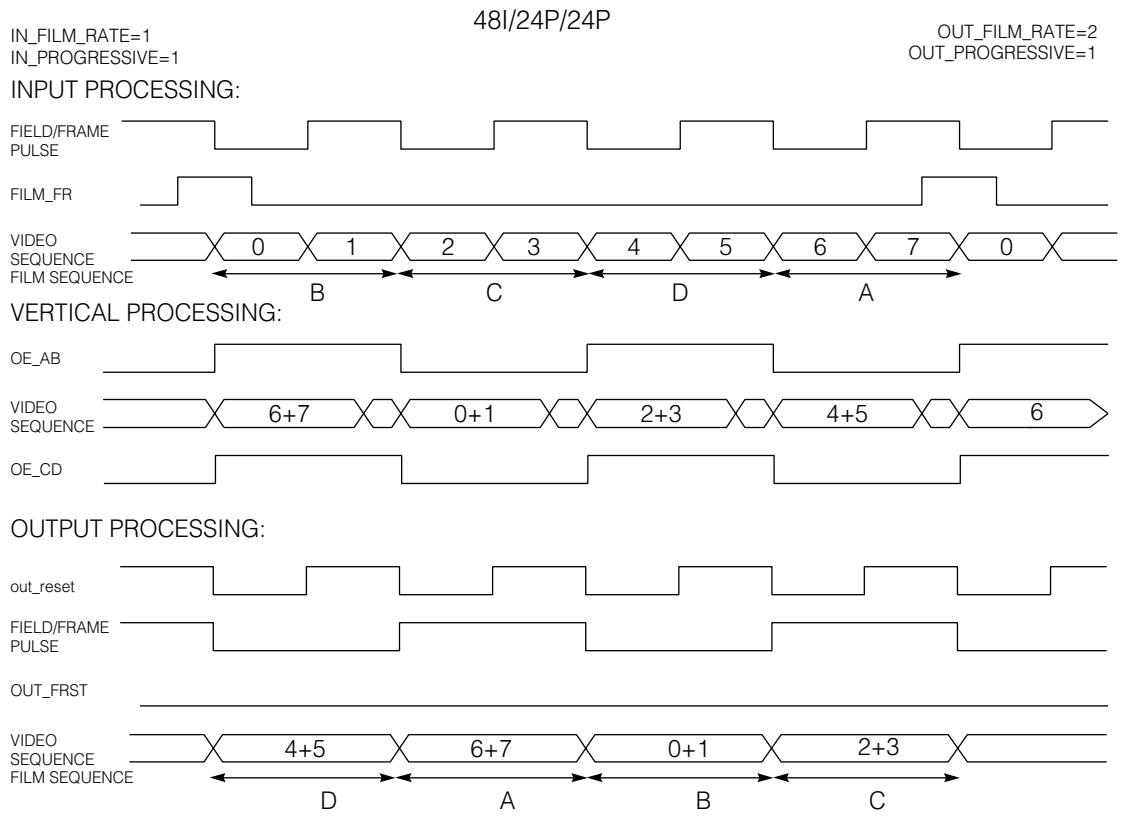


Fig. 37 48I/24P/24P Processing

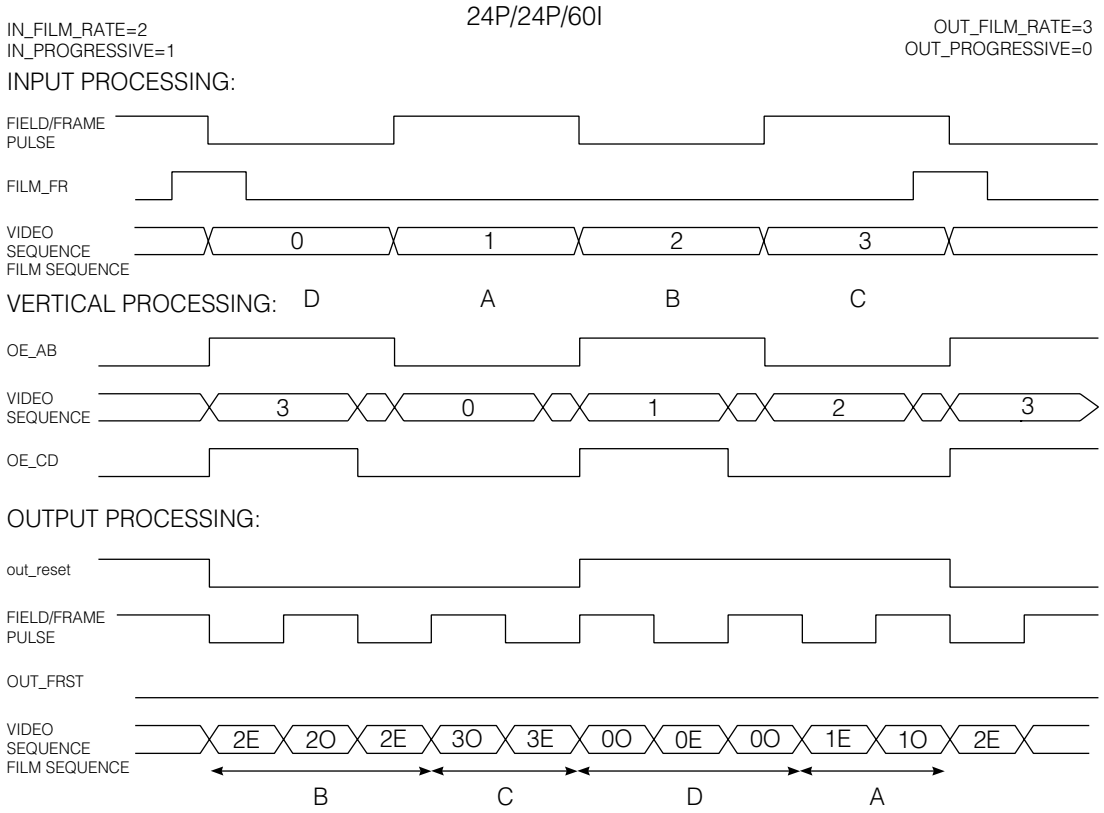


Fig. 38 24P/24P/60I Processing

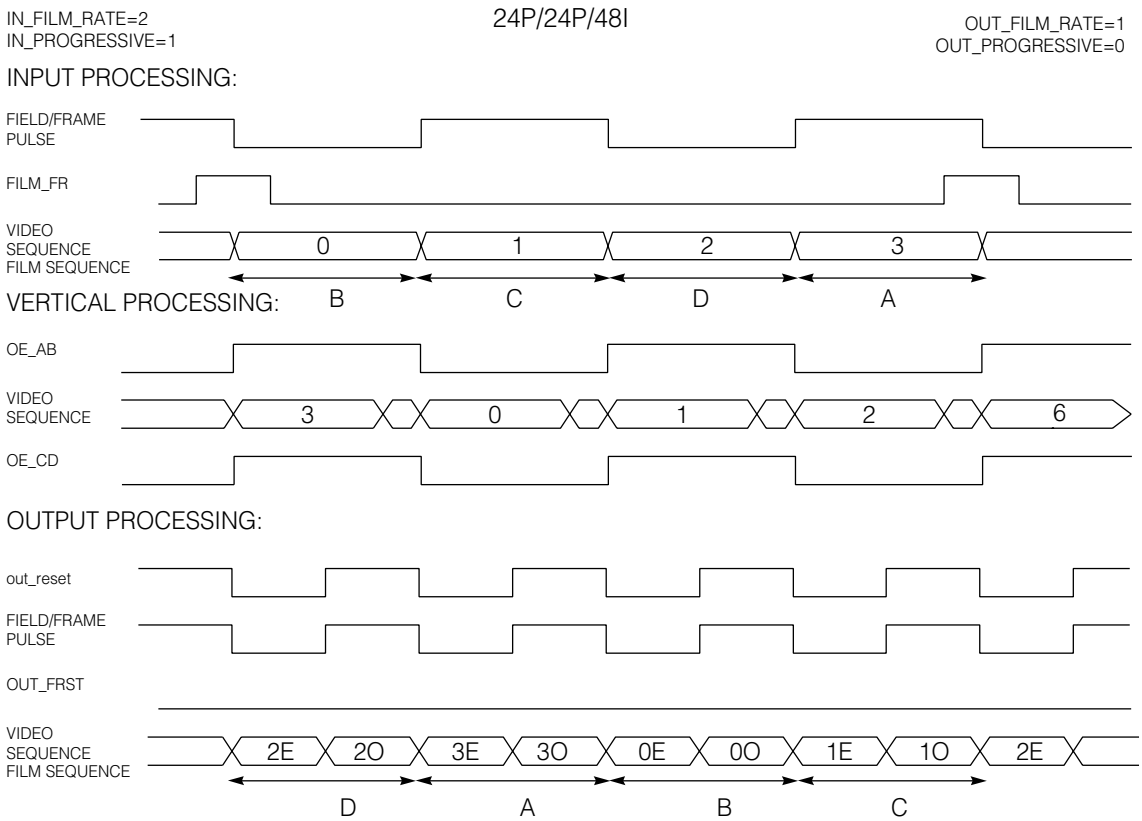


Fig. 39 24P/24P/48I Processing

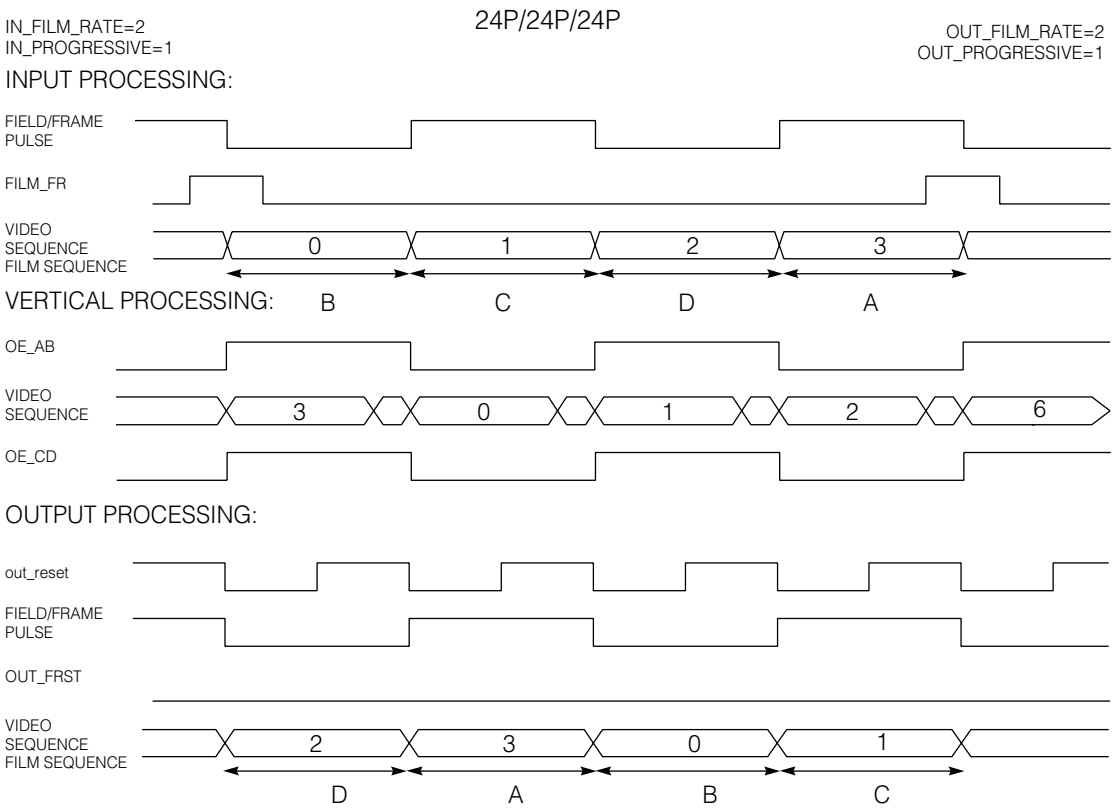


Fig. 40 24P/24P/24P Processing

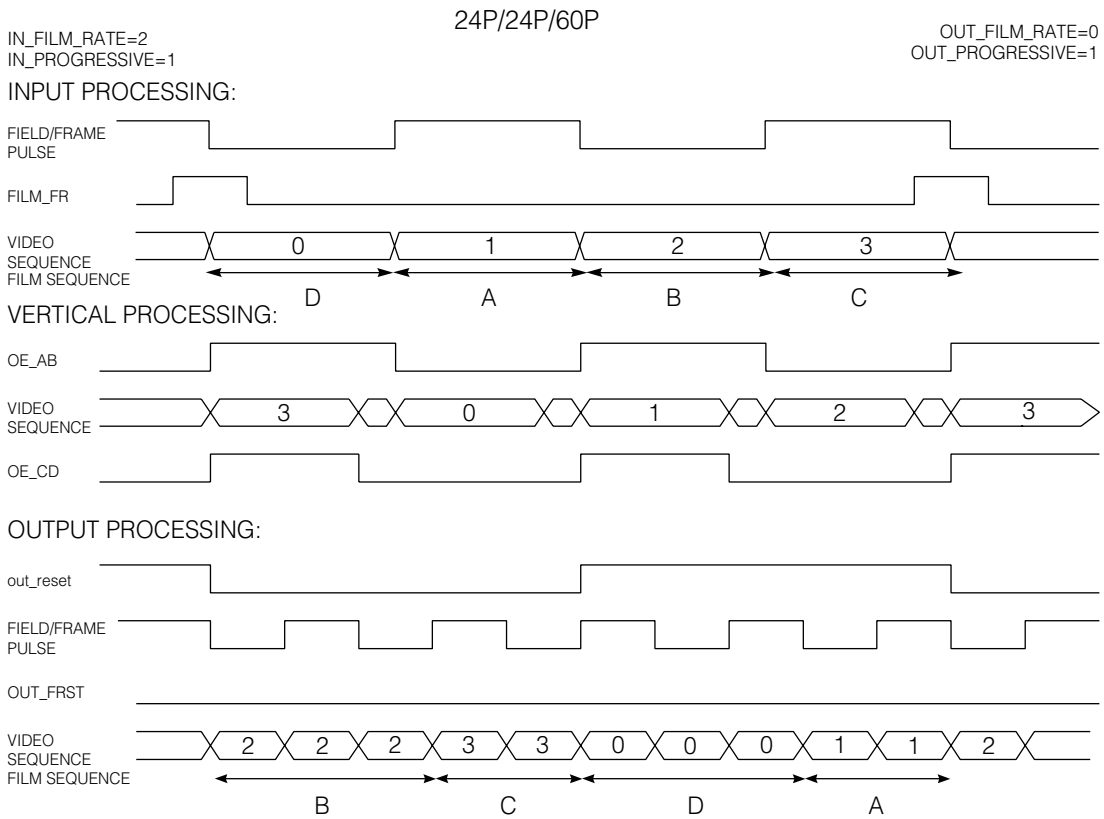


Fig. 41 24P/24P/60P Processing

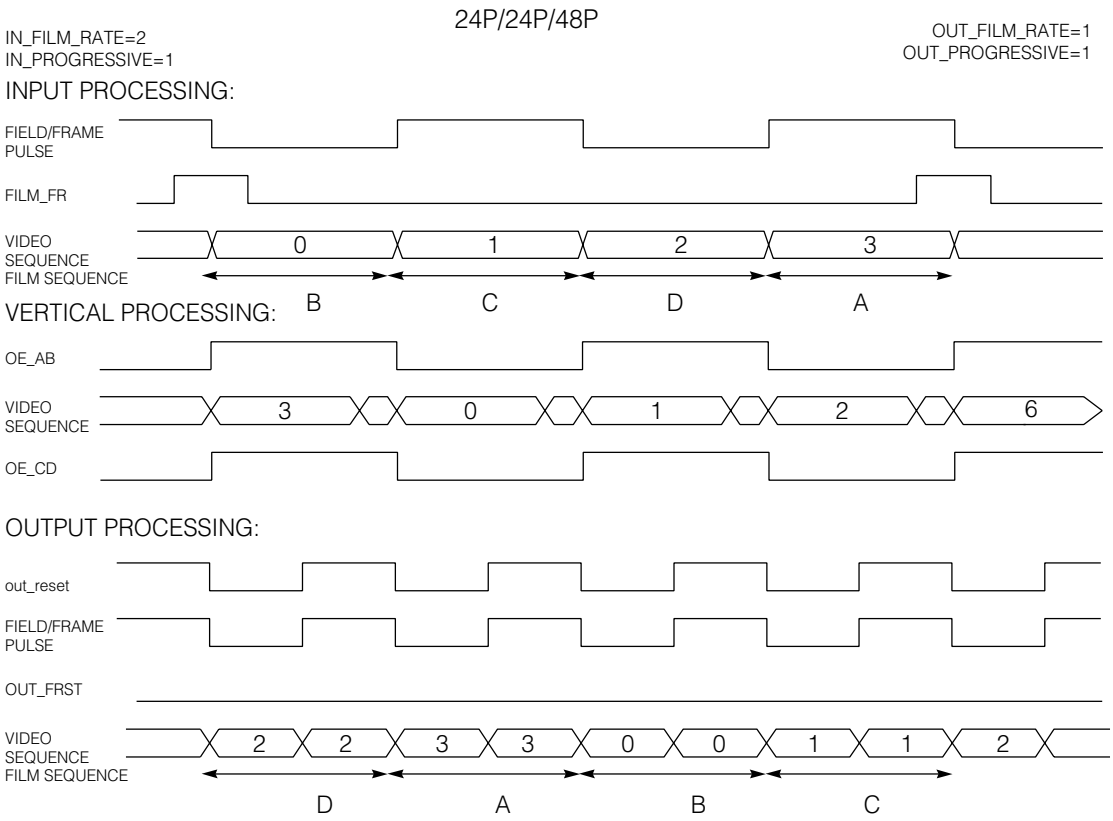


Fig. 42 24P/24P/48P Processing

6.7 Pin Descriptions

The GF9320 uses the transpose memory bus interface signals to communicate with external memory (SDRAMs). The GF9320 is the master device on the bus interface and it controls the timing of the address and data flow. Each signal in the bus interface is described as follows:

6.7.1 Address Bus

- ADDR_A[11:0], ADDR_B[11:0], ADDR_C[11:0], ADDR_D[11:0]
  The address bus is shared by all the memories in the array. The address bus bit ADDR_A11 (Bank Select) selects which bank is to be active in memory array. ADDR_A11 low selects bank A and ADDR_A11 high selects bank B within the memory. During a bank activate command cycle, ADDR_A[10:0] defines the row address when sampled at the rising clock edge. During a read/write cycle, ADDR_A[9:0] defines the column address when sampled at the rising clock edge. In addition to the column address ADDR_A10 is used to invoke auto-precharge operation.

  Similarly, ADDR_B[11:0], ADDR_C[11:0], ADDR_D[11:0] form the address bus of memory arrays B, C and D respectively.

5.7.2 Data Bus

- DATA_A[19:0], DATA_B[19:0], DATA_C[19:0], DATA_D[19:0]
  The data bus is bi-directional. Valid data is driven on the data bus by the GF9320 during write cycle, which is accepted back by the GF9320 during the read cycles. These cycles involve transfers of bursts of data between the SDRAM core and registers of GF9320. Luminance data Y[9:2] are available on DATA_A/B/C/D[19:12] while least significant bits Y[1:0] are available on DATA_A/B/C/D[3:2]. Colour difference data C[9:2] are available on DATA_A/B/C/D[11:4] while least significant bits C[1:0] are available on DATA_A/B/C/D[1:0].

6.7.3 Command Bus

- [RAS_A, CAS_A, WE_A], [RAS_B, CAS_B, WE_B], [RAS_C, CAS_C, WE_C], [RAS_D, CAS_D, WE_D]
  These bus signals are asserted by the GF9320 when commands have to be executed on the SDRAM memory array A. Similarly, [RAS_B, CAS_B, WE_B], [RAS_C, CAS_C, WE_C] and [RAS_D, CAS_D, WE_D] are asserted to execute commands on memory array B, C and D respectively. These signals are considered valid only if the respective CS pin is low during the active edge of the clock.

- CKEN_A, CKEN_B, CKEN_C, CKEN_D
  CKEN_A, CKEN_B, CKEN_C and CKEN_D are used to drive memory arrays A, B, C and D respectively. CKEN input suspends data (i.e. read data remains valid and write data is inhibited) during an active read or write. The GF9320 activates CKEN_A and CKEN_B signals during field/frame write cycle to drop pixels. CKEN_C and CKEN_D are activated during field/frame read cycle to hold pixel values. These signals are considered valid only if the respective CS pin is low during the active edge of the clock.

- CS_A[3:0], CS_B[3:0], CS_C[3:0], CS_D[3:0]
  The CS_A[3:0] signals from the GF9320 allows selection of individual or multiple SDRAMs within the memory array A. The appropriate SDRAM(s) is selected when the respective CS_A[3:0] pin is active low on the rising edge of clock. CS_B[3:0], CS_C[3:0] and CS_D[3:0] select SDRAMs within memory arrays B, C and D respectively.

- DATAEN_AB, DATAEN_CD
  These signals are driven by the GF9320 only during startup to prevent data contention. When sampled high, it places the data bus buffers within the SDRAM in a high impedance state. After successful initialization, DATAEN_AB and DATAEN_CD stay low until the next power-up reset. DATAEN_AB is shared by memories in banks A and B, while DATAEN_CD is shared by memories in banks C and D.

- CK_A, CK_B, CK_C, CK_D
  CK_A, CK_B, CK_C and CK_D are clock signals, which drive the SDRAMs clock pins in memory array A, B, C and D respectively.

7. OUTPUT PROCESSOR

A block diagram of the output processor is shown in Figure 43. The output processor consists of three major functions:

1. Colour difference over-sample
2. Matrix conversion
3. Output format

The colour difference over-sample function is necessary for colour matrix conversion and to provide a 4:4:4 output. The colour difference over-sample block also performs colour background insertion and horizontal edge shaping. Horizontal edge shaping is done to eliminate overshoot on edges when the scaled output does not fill the entire output raster. That is, when OUT_HSTART is greater that 0 for left edge shaping and when OUT_HSTOP is less than OUT_HLEN_ACT for right edge shaping. A programmable flat matte colour background is inserted into the output non-live video. Note that the colour background is inserted prior to the matrix conversion. This means that the downloaded background colour is in the input colour space coordinates.

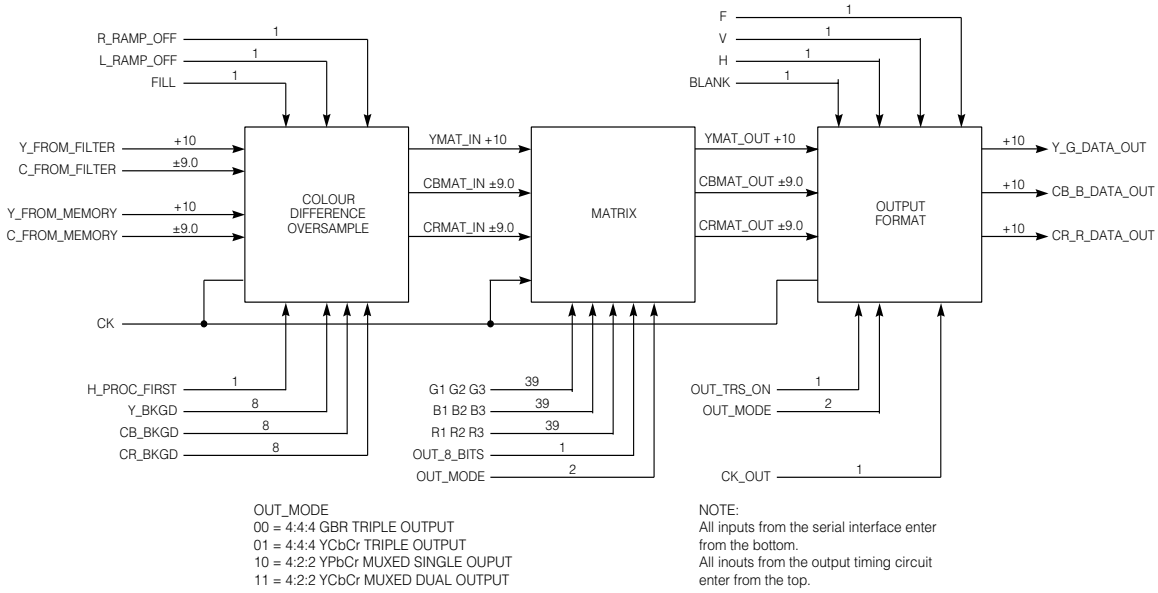


Fig. 43 Output Processor Block Diagram

The matrix block performs the following operations:

$$YMAT_{OUT} = \frac{G1 \cdot (YMAT_{IN} - 64) + G2 \cdot CBMAT_{IN} + G3 \cdot CRMAT_{IN}}{1024} + 64$$

$$PBMAT_{OUT} = \frac{B1 \cdot (YMAT_{IN} - 64) + B2 \cdot CBMAT_{IN} + B3 \cdot CRMAT_{IN}}{1024} + C_{OFFSET}$$

$$PRMAT_{OUT} = \frac{R1 \cdot (YMAT_{IN} - 64) + R2 \cdot CBMAT_{IN} + BR3 \cdot CRMAT_{IN}}{1024} + C_{OFFSET}$$

where $YMAT_{IN}$, $CBMAT_{IN}$ and $CRMAT_{IN}$ are the inputs to the matrix; $YMAT_{OUT}$, $CBMAT_{OUT}$ and $CRMAT_{OUT}$ are the outputs of the matrix; and G1, G2, G3, B1, B2, B3, R1, R2 and R3 are the matrix coefficients; C_{OFFSET} is given by

$$C_{OFFSET} = \begin{cases} 512 & OUT\_MODE = 0 \\ 64 & otherwise \end{cases}$$

and 1024 is the gain of the matrix.

The matrix coefficients provide +6dB of range for gain adjustments. The C_b and C_r components at the input to the matrix are in 2's complement format. The B and R components at the output of the matrix are unsigned in GBR output mode (OUT_MODE=0) and are offset binary in YC_bC_r output mode (OUT_MODE=1, 2 or 3). The matrix coefficients are completely programmable and are downloaded as described in the Section 3.

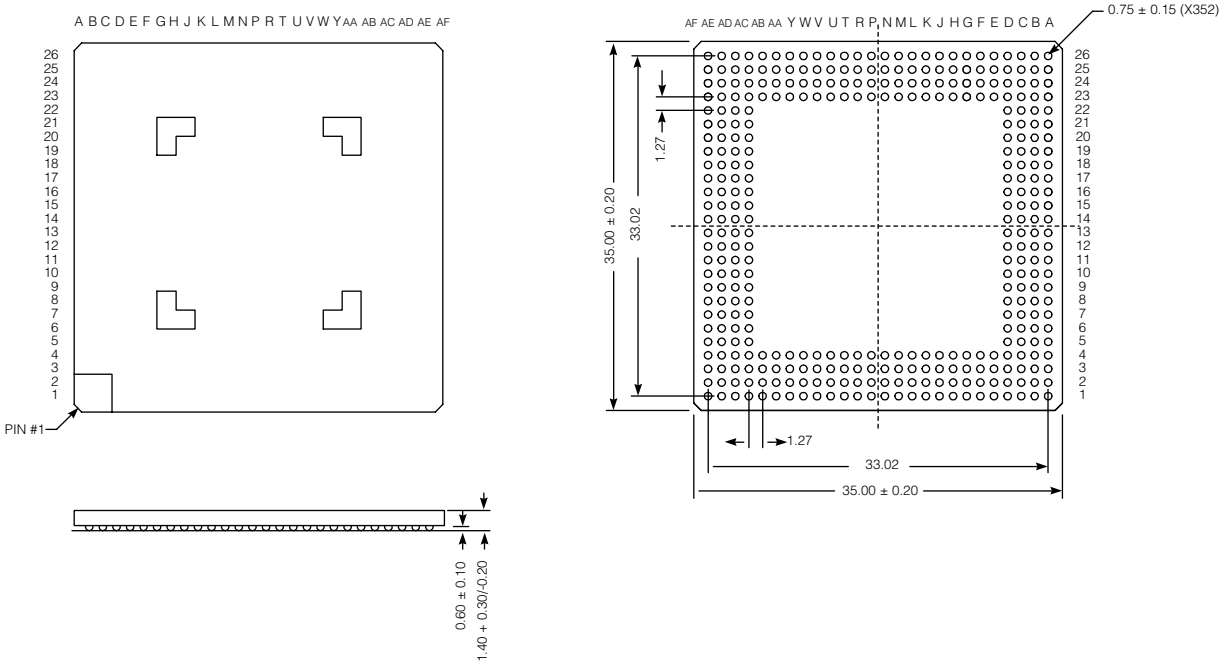
The output format block formats the data into one, two or three channels according to the OUT_MODE parameter and inserts the output format TRS. If TRS is enabled, the data is clipped to 4 and 1019 for 10-bits or 1 and 254 for 8-bits.

8. OUTPUT TIMING CONTROL

The output timing and control block determines the output video data timing. This block contains horizontal and vertical counters based on the output format parameters. The output timing is adjusted relative to the reference by using the LINE_ADV and H_POS parameters. The output reference is either the input TRS (if OUT_REF = 0) or the OUT_FRST pin on the GF9320 (if OUT_REF = 1). This provides for internal or external lock capability. The LINE_ADV parameter advances the output video data by LINE_ADV output lines. The H_POS parameter delays the output video data by H_POS samples. The range of H_POS is one output line or OUT_HLEN_TOT samples.

Only limited ranges of input/output timing relationships are available by using the GF9320. In general, there are 2 fields/frames of delay through the GF9320. It is not possible for the GF9320 to have an output timing relationship such that the last active output line occurs after the SDRAM field/frame switch point.

9. PACKAGE DIMENSIONS



DOCUMENT IDENTIFICATION
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